Impact of Positive Sequence Admittance and Negative Sequence Conductance of D-Statcom to Compensate Variations in Voltage Levels in Distributed Generation Systems

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ABSTRACT

Voltage fluctuations resulting from variable output power of renewable energy sources are strictly challenging power quality in distributed-generation systems. This paper presents a control method for distributed static synchronous compensator (D-STATCOM) to alleviate variation of both positive- and negative-sequence voltages. The D-STATCOM simultaneously operates as fundamental positive-sequence admittance and fundamental negative-sequence conductance to restore the positive sequence voltage to the nominal value as well as reduce the negative-sequence voltage to an allowable level. Both admittance and conductance are dynamically tuned to improve voltage regulation performances in response to load changes and power variation of renewable sources. A proportional–resonant current regulator with selectively harmonic compensation is realized to control the fundamental current of the D-STATCOM as well as reduce the harmonic current, which could be an advantage in practical applications due to high voltage distortion in low-voltage micro grids. Voltage-regulation performances are discussed for different D-STATCOM locations as well as different D-STATCOM currents. Computer simulations and laboratory tests validate effectiveness.

Keywords: *Distributed STATCOM (D-STATCOM), micro grid, voltage fluctuations, voltage imbalance*

I. INTRODUCTION

High penetration level of renewable energy sources and distributed generation (DG) plants faces new challenges in the operation of transmission and distribution networks .The growing installed power from DG plants has led to a change in the requirements for ancillary services, particularly during grid faults. Among these new services, voltage control in wind plants, photovoltaic parks and other large-scale power plants is gaining increasing attention due to its capability to improve grid efficiency, safety and reliability in a distributed manner. A voltage sag is a perturbation in the grid voltages characterized by a short-time reduction in the magnitude of one or several phases. The effects of such disturbances are important in terms of economic losses, malfunction of devices connected to the grid and in extreme cases, blackouts. To alleviate the adverse effects of grid faults, grid codes from the network system operators dictate the behavior of DG plants. The D-STATCOM simultaneously operates as fundamental positive-sequence admittance and fundamental negative-sequence conductance to restore the positive sequence voltage to the nominal value as well as reduce the negative-sequence voltage to an allowable level [1]. The evolution of these codes for DG during grid faults started with low-voltage ride-through, which demands withstanding Voltage sags.

Increasing the use of RESs could help relieve network congestion, reduce system losses, and defer infrastructure investments. These issues have received much attention recently, and numerous projects have

been commissioned to demonstrate and evaluate functionality of microgrids by worldwide research organizations, for example, Consortium for Electric Reliability Technology Solutions [3] and New Energy and Industrial Technology Development Organization [4].Conventionally, voltage fluctuations in the power system mainly result from impedance of transmission lines, loading types, and uneven distribution of single-phase loads. The scenarios become much severer in the low-voltage microgrid system due to reverse power flow contributed by distributed generations (DGs) in either three- or single- phase connection. As the penetration level of DG sources was increased, reactive power injection was included in grid codes to support the grid voltage and to reduce the possibility of voltage collapse. The next generation of grid codes could require negative sequence current injection and voltage support control in steady-state and transient. The aim is to regulate the point of common coupling (PCC) voltage to a safety range, preventing damage in the equipment while improving voltage support services.

Voltage fluctuations cause system losses, capacity reduction, transformer overloading, and motor overheating, and even results in output limitation of DGs, nuisance tripping of protected devices, and malfunction of sensitive equipment. According to IEEE Std 1547.2-2008 [6], voltage fluctuations are limited to ±5% as RESs are paralleled to low-voltage systems. Voltage imbalance measured by %Unbalance or %VUF kept below 2.0%–3.0% is acceptable for both manufactures and utility, where %Unbalance and %VUF are defined as the percentage of maximum deviation from the average value and the ratio of the negative-sequence voltage to the positive sequence voltage, respectively [7]. Therefore, voltage regulation is absolutely needed to allow more DGs to join grid connected operation. Voltage regulation in the power system could be realized by using an on-load tap changer (OLTC) or a static VAR compensator (SVC) at substations, and a step voltage regulator or a switched capacitor on feeders. With the help of the so-called optimal or intelligent control on all devices, the voltage profile could be improved on a real-time base [8], [9].

In this paper the proposed D-STATCOM realizes positive sequence admittance and negative-sequence conductance to regulate positive-sequence voltage as well as suppress negative-sequence voltage. Both positive-sequence admittance and negative-sequence conductance are dynamically adjusted according to positive-sequence voltage deviation and imbalanced-voltage percentage. Therefore, voltage quality can be maintained at an allowable level in case of variation of DGs or loads. A proportional–resonant current regulator with selective harmonic compensation is implemented to control the fundamental current of the D-STATCOM as well as reduce harmonic current due to high voltage distortion in low-voltage networks.

II. PRINCIPLE OF OPERATION

The proposed Topology is shown in Fig 1. Fig. 2 shows the D-STATCOM circuit implemented by a conventional three-phase voltage source inverter and connected to the distribution line by a step-up transformer with Simulink model of the STATCOM. The proposed D-STATCOM operates as fundamental positive-sequence admittance and fundamental negative-sequence conductance as given
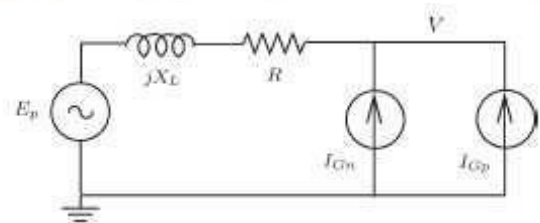

Fig 1: Thevenin's Equivalent Circuit.

$$i^* = Y_p^* \cdot E_f^{+\prime} + G_n^* \cdot E_f^-$$

where i^* is the reference current of the D-STATCOM, $E+1f$ is the quadrature fundamental positive-sequence voltage, and $E-f$ is the fundamental negative-sequence voltage. The fundamental positive-sequence admittance Y^*p and the fundamental negative sequence conductance G^*n are defined as variable control gains to accomplish regulating positive-sequence voltage and suppressing imbalanced voltage. The control algorithm will be discussed in detail, followed by Phasor analysis of the proposed method.
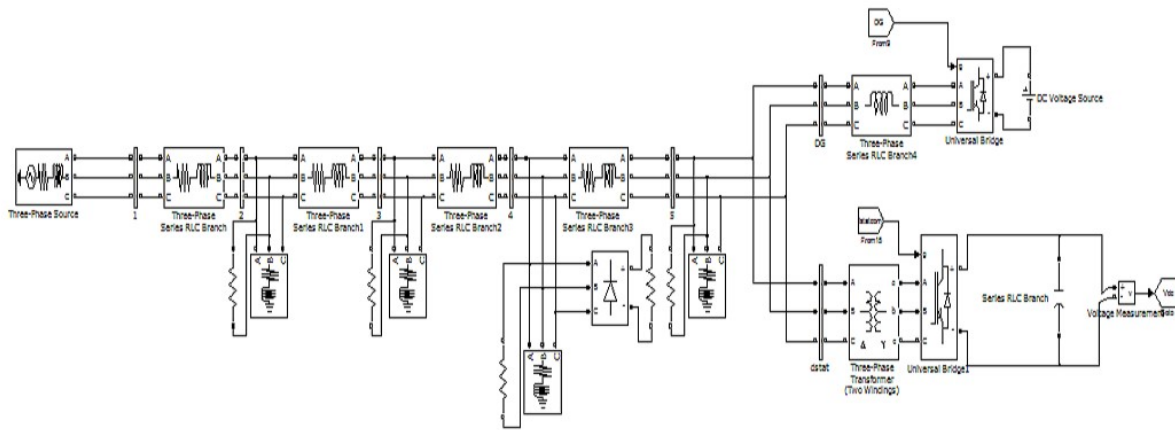
Fig 2: Simulink model of proposed D-STATCOM

The control is realized by using the so-called synchronous reference frame (SRF) transformation, as shown in Fig. 3. The positive-sequence voltage Vector E+eqdis obtained by using a low-pass filter (LPF) to filter out ripple components addition to the LPF, a band-rejected filter tuned at the second-order harmonic frequency is needed to determine the negative-sequence voltage Vector Eqd–e . By applying reverse transformation, the quadrature fundamental positive-sequence voltage E+¹ f and the negative sequence voltage E−f in the three-phase system are available, where E+f lags the fundamental positive-sequence voltage by 90∘. The positive-sequence current command I∗+f and the negative-sequence current command i∗−f are equal to E+¹ f, multiplied by Y ∗pand E − f, and multiplied by G∗n, respectively. Thus, the current command i∗ is generated as given below. A dc voltage control is also designed to assure proper operation of the D-STATCOM. Proportional–integral (PI) regulator is realized to produce a fundamental current in phase with the positive-sequence voltage to maintain the dc voltage Vdc at the reference value V∗dc.
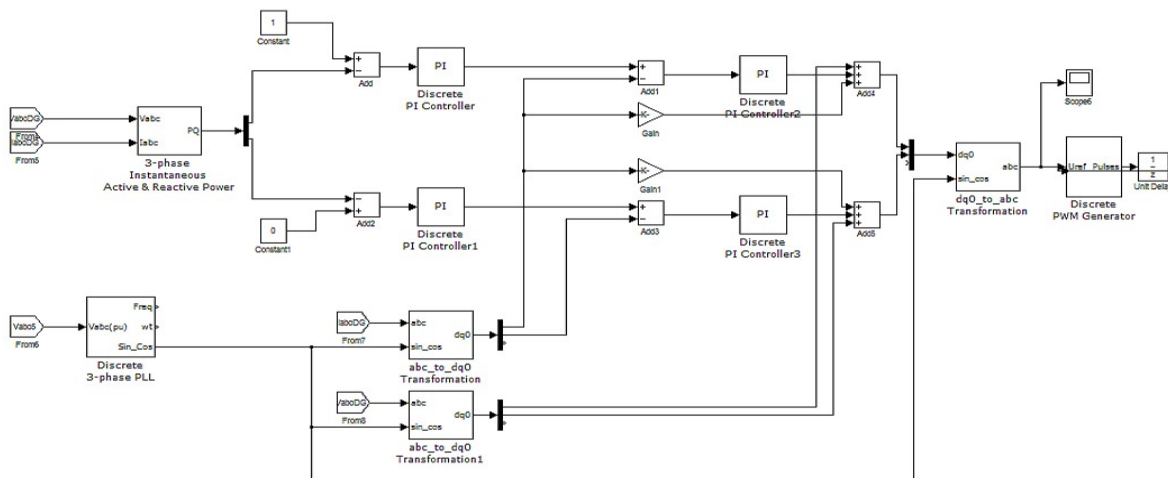

Fig 3: Generation of Reference Current

Phasor Analysis:

In this, D-STATCOM operation will be discussed based on Phasor analysis Fig 5 & Fig. 6. Thevenin equivalent circuit with the proposed D-STATCOM compensating positive-sequence current ICp as well as negative-sequence current ICn is shown in Fig. 4 Before the D-STATCOM starts operation, positive sequence voltage is swelled up, as shown in the red vectors of Fig. 5.
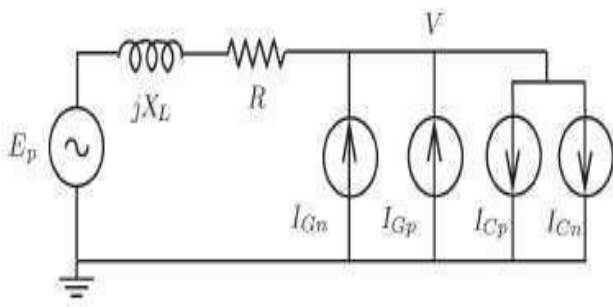
Fig 4: Thévenin equivalent circuit with the D-STATCOM

$$i^* = Y_p^* \cdot E_f^{+\prime} + G_n^* \cdot E_f^-$$

D-STATCOM compensating positive-sequence current ICp and negative-sequence current ICn. $|Vp|$ is obviously larger than $|Ep|$. This results from the voltage drop VGp on line impedane $Z = R + jXL$ when IGp is injected into the grid. On the other hand, the negative sequence current IGn flowing on the line impedance Z causes the negative-sequence voltage drop Vn, as shown in the red vectors of Fig. 6. When the D-STATCOM draws $ICp = -jY^* p \cdot Vp$, the blue vectors of Fig. 10 show that $|Vp|$ could be restored to the nominal value (the dashed line) by VCp due to ICp being 90θ lagging with respect to Vp. In addition, phase leading of Vp after compensation is dependent on the line impedance Z and Real power injection IGp. Similarly, the D-STATCOM performs negative-sequence conductance Gn, reciprocal of resistance, to provide low impedance for negative-sequence current, thus reducing negative-sequence voltage.
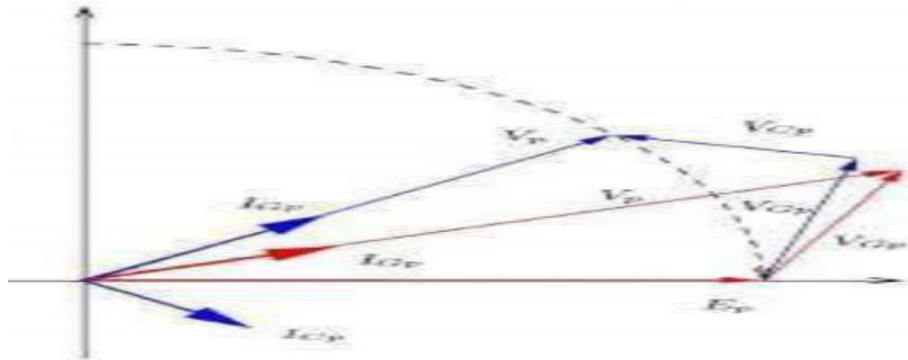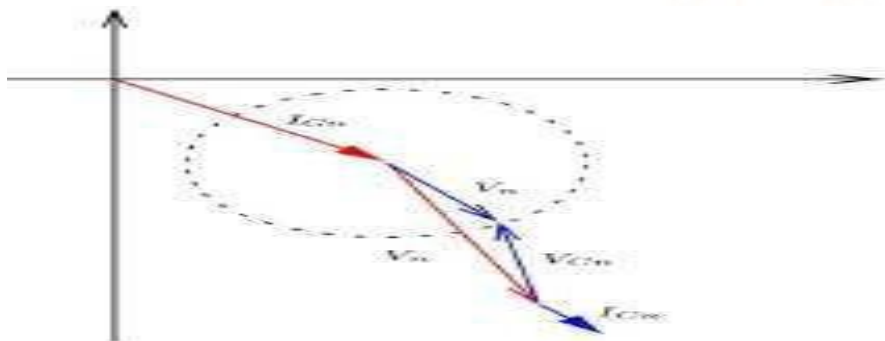

Fig 5: Phasor diagram of positive sequence

Fig 6: Phasor diagram of Negative sequence

As shown in the blue vectors of Fig. 6, the D-STATCOM draws

$ICn = G^*n.Vn$ (1)

to mitigate negative-sequence voltage by

$VCn = -ICn \cdot Z$ (2)

Accordingly, $|Vn|$ could be maintained at an acceptable value by variable $G\ n$. The acceptable value is represented by a dotted circle. As a consequence, we conclude that positive sequence voltage could be restored

by introducing an active admittance (or inductance) and that negative-sequence voltage could be suppressed by emulating an active conductance.

Current Control:

Based on the current command i , the measured current i, and the measured voltage E, the current regulator shown in
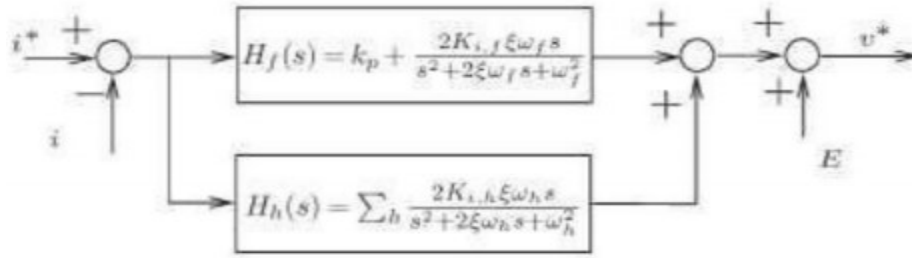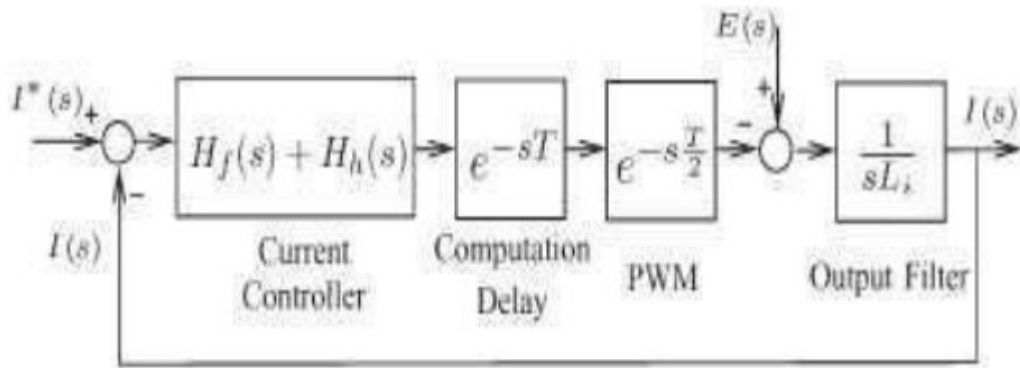

Fig 7: Current control
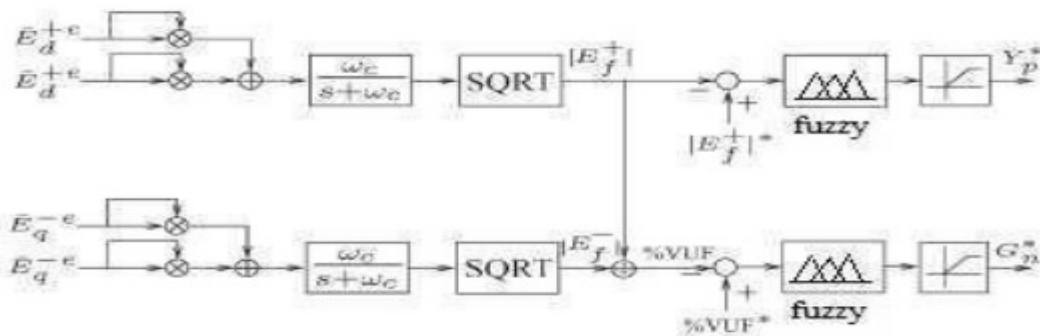

Fig 8: Current-loop block diagram

Fig 9: Tuning control of $Y*p$ and $G*n$

$$H_f(s) = k_p + \frac{2K_{i,f}\xi\omega_f s}{s^2 + 2\xi\omega_f s + \omega_f^2}$$

$$H_h(s) = \sum_h \frac{2K_{i,h}\xi\omega_h s}{s^2 + 2\xi\omega_h s + \omega_h^2}$$

$$H_f(s) = k_p + \frac{2K_{i,f}\xi\omega_f s}{s^2 + 2\xi\omega_f s + \omega_f^2}$$

$$H_h(s) = \sum_h \frac{2K_{i,h}\xi\omega_h s}{s^2 + 2\xi\omega_h s + \omega_h^2}$$

Fig. 7 produces the voltage command $v*$ for space vector pulsewidth modulation (PWM) control of the inverter. The transfer functions $H_f(s)$ and $H_h(s)$ are defined. where k_p represents a proportional gain; ω_f and $K_{i,f}$ are the fundamental frequency and its integral gain, respectively; and ω_h and $K_{i,h}$ represent the harmonic frequency and its integral gain, respectively. The current regulation is tuned with damping ratio ξ to introduce a narrow gain peak centered at the fundamental frequency for fundamental current tracking and also to produce various narrow gain peaks at the harmonic Frequencies to reduce current distortion. The current-loop lock diagram is shown in Fig. 8, in which digital signal processing delay and PWM delay are considered. T represents a sampling period. Accordingly, current-tracking capability and current loop stability can be simply evaluated by using Bode plots of open and closed-loop transfer functions. Further discussions on current control are provided in the simulation section.

Tuning Control:

Fig. 9 shows the tuning control with fuzzy controller of both $Y*p$ and $G*n$. $|E+|$ and $f|E-|$ are f defined as above. They can be approximately calculated by using LPFs and SQRT operation, where LPFs are designed with cutoff frequency $\omega c = 10$ Hz to filter out ripple components in the calculation. Then, a Fuzzy controller is realized to generate $Y*p$ to maintain $|E+f|$ at the nominal value $|E+f|*$. Similarly, imbalanced voltage could be suppressed and maintained at an allowable level by controlling $G*n$. In this paper, we adopt %VUF (percentage of voltage imbalance factor) to assess the level of imbalanced voltage. It is defined as the ratio of the negative-sequence voltage to the positive-sequence voltage.

$$\left|E_f^+\right| = \sqrt{\frac{\int_t^{t+T}(E_q^{+e}(t)^2 + E_d^{+e}(t)^2)}{T}dt}$$

$$\left|E_f^-\right| = \sqrt{\frac{\int_t^{t+T}(E_q^{-e}(t)^2 + E_d^{-e}(t)^2)}{T}dt}$$

$$\%VUF = \frac{\left|E_f^-\right|}{\left|E_f^+\right|} \cdot 100\%.$$

Basically, there are three control loops in the proposed method. The bandwidth of the current control loop is the highest one, which is dependent on the switching frequency of the inverter. The tuning loops of both admittance and conductance are to generate the current commands to improve power quality, so their bandwidths are lower than that of the current loop. On the other hand, the voltage on the dc capacitor will fluctuate due to inverter losses and conductance for suppressing imbalanced voltage. The lower the dc capacitance, the larger fluctuation will happen. Generally, due to large capacitance, the bandwidth of dc voltage control is lowest in the system.

IV. SIMULATION RESULTS

The proposed D-STATCOM is successfully implemented in MATLAB/SIMULINK environment as shown in Fig. 2. The simulation results are verified to illustrate voltage fluctuations and effectiveness of

the proposed D-STATCOM in a radial line rated at 23 kV and 100 MV · Since the grid voltage at the end of a radial line is most sensitive to injection of both real and reactive powers based on load flow analysis, the D-STATCOM is proposed to be installed at the end of the line.

The inverter-based DG is assumed to be installed at the end of the bus, and also all single-phase loads are connected between phases A and B to generate severe voltage variation as well as voltage imbalance. The power of the DG is controlled by a Fuzzy and PI controllers in the synchronous Reference Frame to produce the current command. Similar to the current control of the D-STATCOM, resonant current control is realized to regulate the output current of the DG.

I. Steady-State Operation

Before the D-STATCOM starts operation, Fig. 15 shows that bus voltages are significantly swelled and imbalanced due to the DG and single-phase loads. Voltage fluctuation is Setting worse toward the end of the line. When the D-STATCOM is initiated with compensation of the positive-sequence voltage only $(G*n = 0)$, $|E+f|$ on each bus could be restored to the nominal value. At this time, the D-STATCOM is operated at $Y*p = 0.37$ p.u. with rms currents ia = ib = ic = 0.37 p.u.. However, Fig. 16 shows that voltage fluctuation is still significant due to imbalanced voltage. After imbalance suppression is activated, Fig. 17 shows that bus voltages are clearly recovered from fluctuation. Table V illustrates that both $|E+f|$ and %VUF could be maintained below the presetting level on all buses. Current-tracking capability is assured by a resonant gain at the fundamental frequency. Various resonant gains at the 5th, 7th, 11th, and 13th frequencies are introduced to reduce harmonic current. The phase margin of the designed current loop approaches $70*$. D-STATCOM currents are almost maintained as sinusoidal waveforms. This could confirm the functionality of harmonic reduction because the nonlinear load at Bus 4 results in severely distorted line voltages. (THDa = 1.5%, THDb = 1.25%, and THDc = 1.85%).
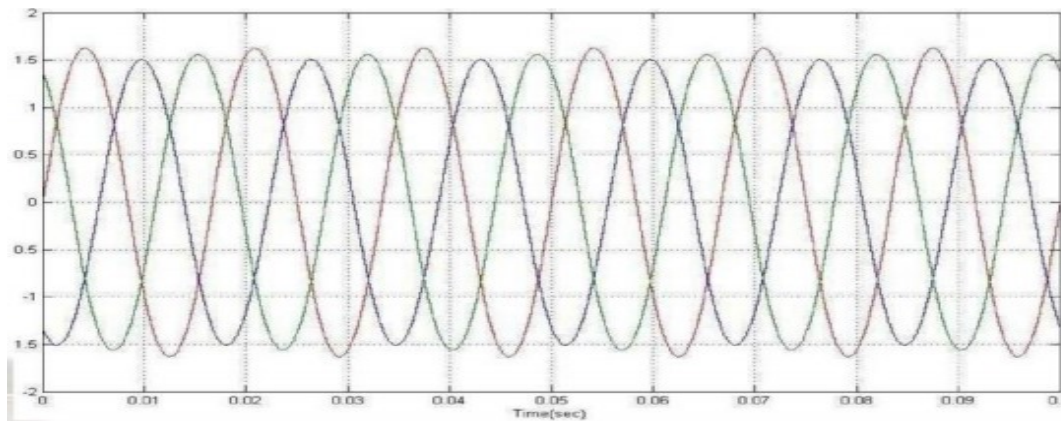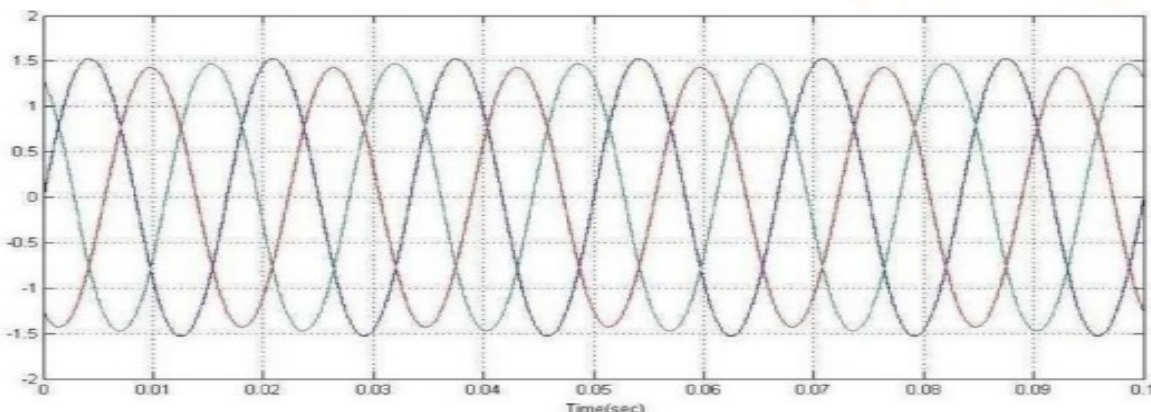

Fig 15: D-STATCOM off

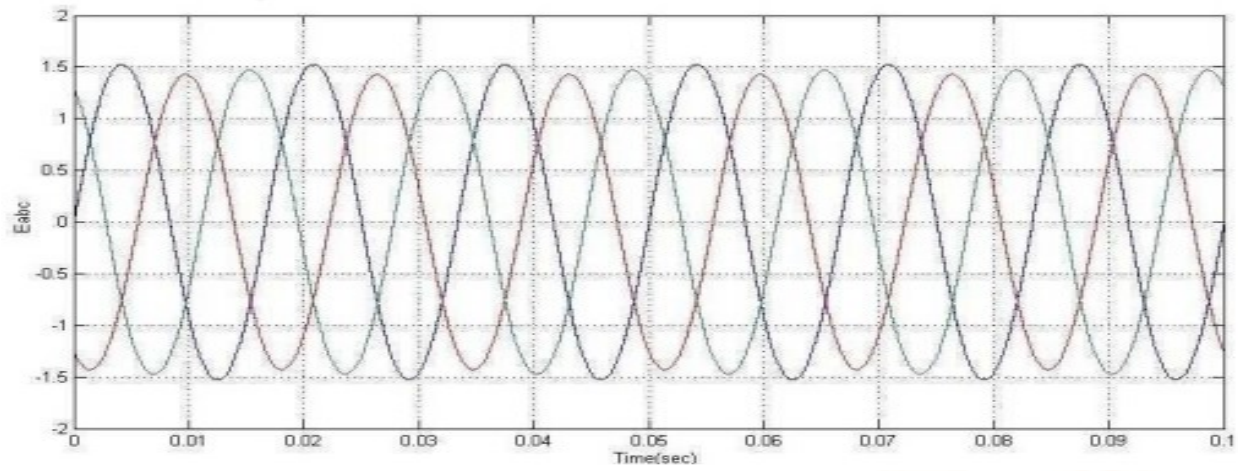

Fig 16: D-STATCOM on, but $G*n = 0$
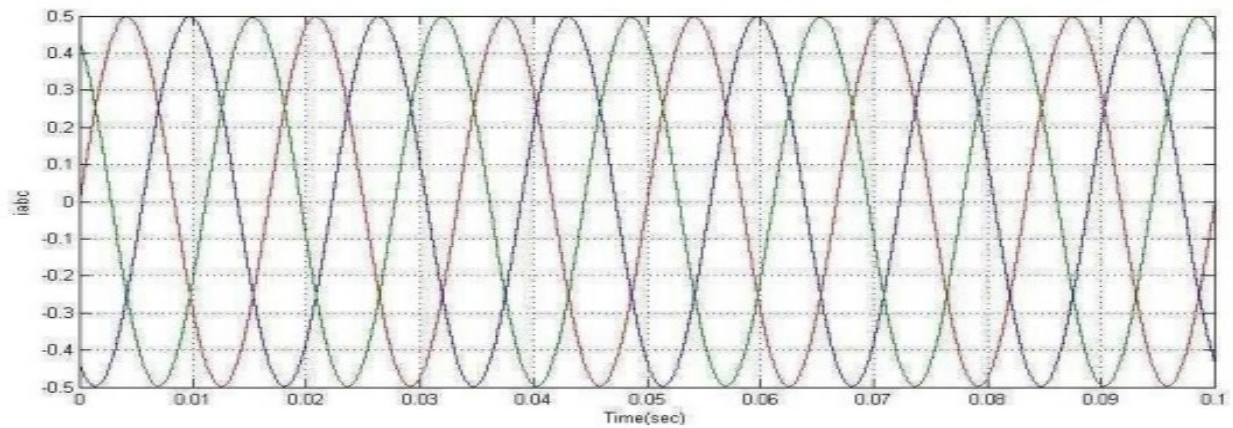
Fig 17: D-STATCOM on

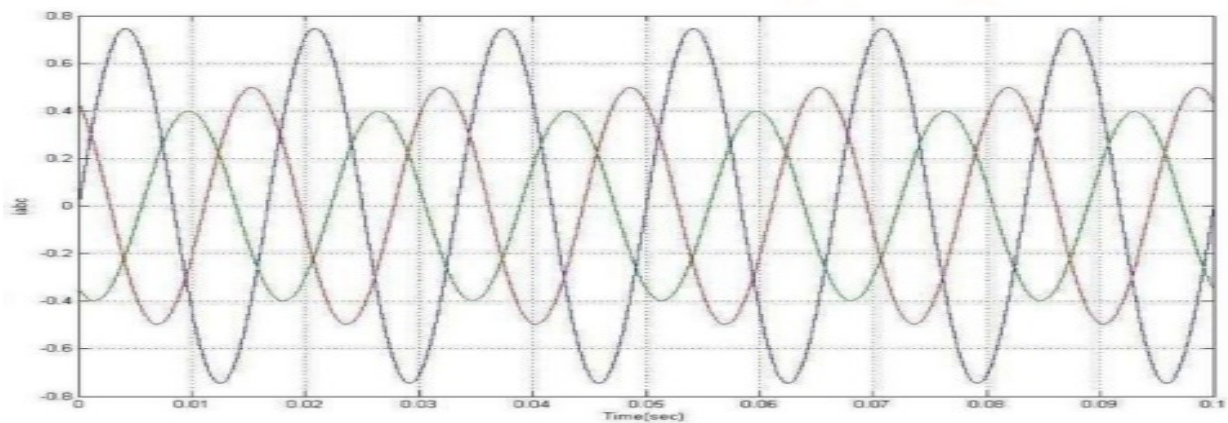**Fig 18: D-STATCOM on, but $G*n = 0$.**

Fig 19: D-STATCOM on

II.   Transient Operation

The transient performances of the D-STATCOM is shown in Fig. 20, 21, When three-phase loads at Buses 3 and 4 are turned off at t = 4 and 6 s, respectively, |E+ f| is increased. Thanks to the tuning control, $Y*p$ is correspondingly increased to maintain $|E+_f|$ at 1.0 p.u. In contrast, tuning off the single-phase load at t = 7 s reduces the imbalanced voltage in Fig. 21 so $G*n$ is decreased to keep %VUF at 4%, as shown in Fig. 24. At t =

8 s, the output power of the DG decreases from 0.9 to 0.75 p.u. Since the swelled voltage becomes slighter, $Y*p$ and the required reactive power of the D-STATCOM are reduced accordingly. More interestingly, with the DG being turned off at t = 9 s, |E+f | becomes lower than 1.0 p.u. In this situation, the D-STATCOM is operated with minus $Y*p$ to supply reactive current for increasing fundamental voltage. Instead of an inductor, the D-STATCOM currently behaves as a capacitor. Therefore, voltage regulation could be accomplished by dynamically tuning $Y*p$ and $G*n$ of the D-STATCOM.
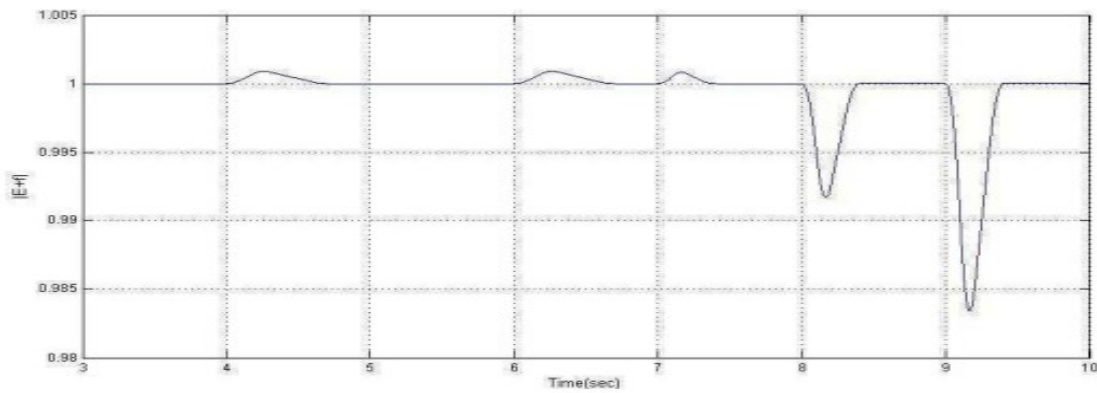

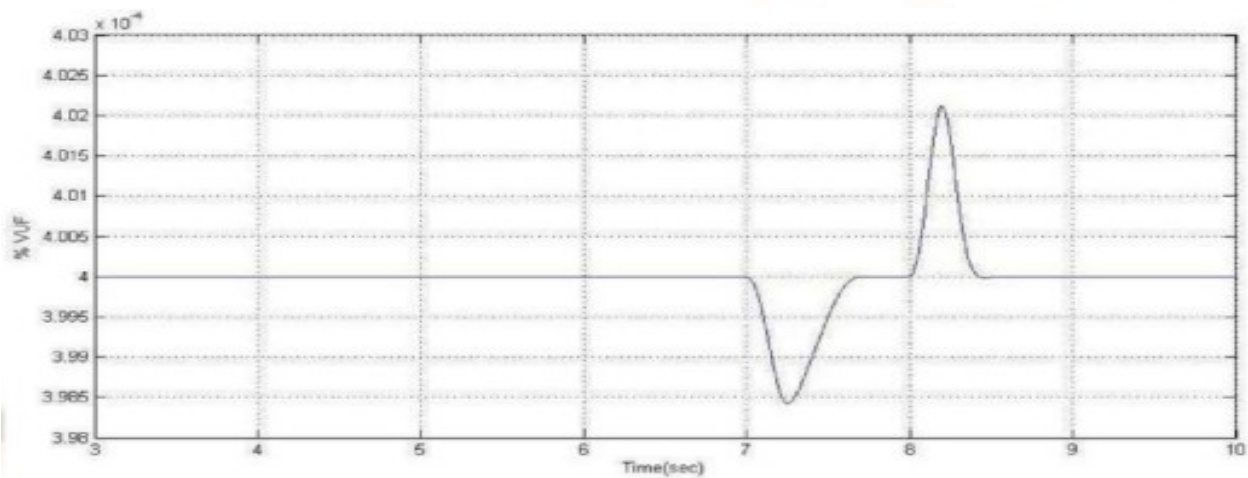
Fig 20: Voltage in transient |E+f|
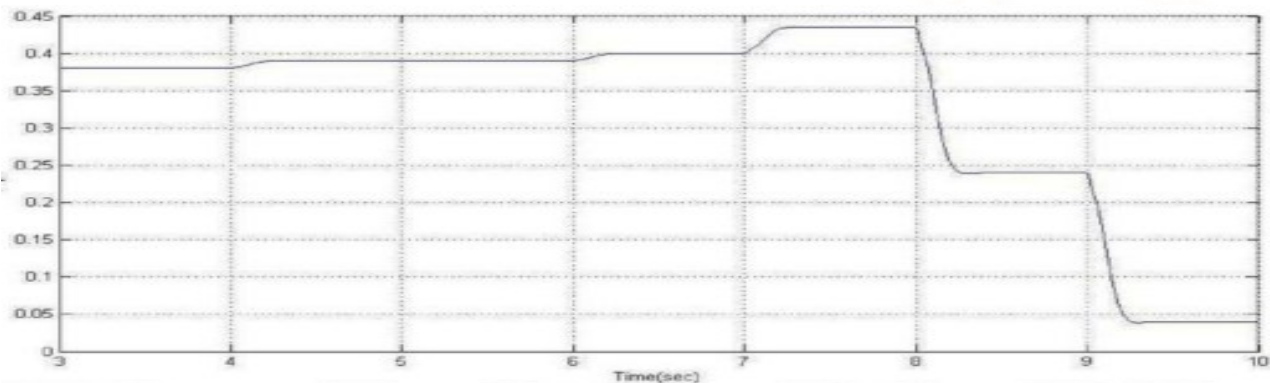

Fig 21: Voltage in transient % VUF

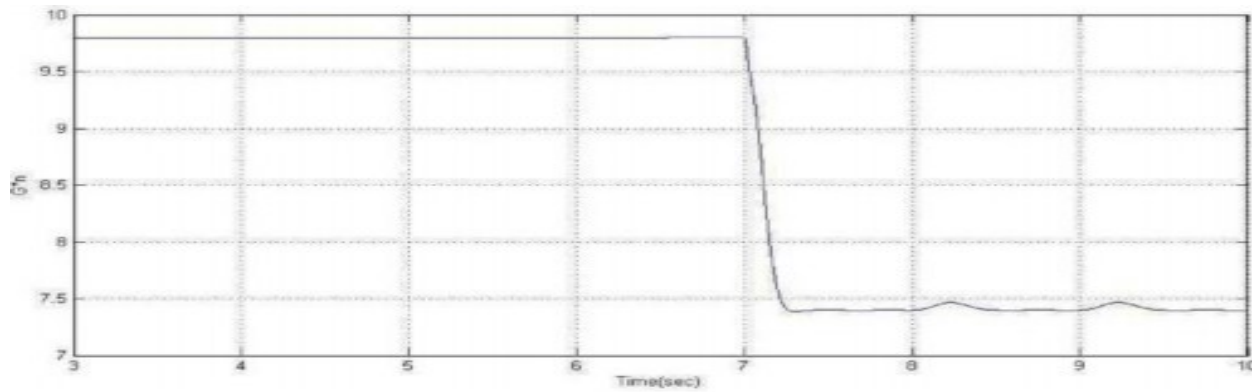**Fig 22: D-statcom commands in transient Y*p**

Fig 23: D-statcom commands in transient G*n

III.   *Large R/L Ratio*

In low-voltage systems, the feeder with high R/L ratio is very common. Here, we evaluate D-STATCOM performances in cases where the R/L ratio is increased by two and five times, respectively. As seen both |E+f| and %VUF are obviously increased, and this situation is growing worse with the increase of the R/L ratio.

After the D-STATCOM is in operation, |E+ | fis restored to the nominal value throughout the feeder, and %VUF is also improved. However, the imbalanced voltages on Buses 3 and bus 4 are still higher than 4%. This is because the feeder with high R/L ratio will limit the damping capability of the D-STATCOM at a distant location.

V. CONCLUSION

The proposed control strategy of the D-STATCOM to alleviate voltage fluctuations in high-level penetration of DG systems is simulated together with positive-sequence admittance to recover the positive-sequence voltage and negative sequence conductance is developed to enhance imbalanced voltage. A versatile fuzzy controller is designed with a tuning control is designed to dynamically adjust admittance as well as conductance commands to maintain both positive and negative-sequence voltages at an allowable level in response to power variation of DGs or loads. Extended discussions on the relationship between the D-STATCOM current and its voltage regulation have been presented. The D-STATCOM is controlled by separately adjusting admittance and conductance, and the compromise between the D-STATCOM rating and the required improvement on power quality can be accomplished.

The voltage-regulation performances of the D-STATCOM deployed at different locations have also been investigated. The termination–installation D-STATCOM is the best option to suppress voltage fluctuations. By using fuzzy controller voltage sag, voltage swells and low harmonic distortion can be achieved for the power quality improvement.

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