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Razor Based Low-Power Multiplier with Variable Latency Design

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Abstract: ***Digital multipliers are the most critical part of the digital systems. The overall performance of the Digital system depends on the speed of the multipliers. Due to Aging effects like negative bias temperature instability in pMOS transistor when it is under negative bias, increases the threshold voltage of the transistor hence the speed of the multiplier reduces, a similar positive bias temperature instability effect occurs in nMOS transistor, when it is under positive bias. Hence it is required to design a reliable low power high performance multiplier. In this paper we propose a Razor based low power multiplier with variable latency design. In this multiplier the performance degradation due to the aging effect can be minimized using Adaptive Hold Logic. This logic is applied to column and row bypassing multipliers.***

Keywords: Adaptive Hold Logic, Column bypassing multiplier, Razor flip-flop, Row bypassing multiplier, Variable latency design**.**

1. Introduction

Digital multipliers are the most critical arithmetic units in many of the digital applications such as Fourier transform, digital filtering, discrete cosine transforms and image processing units. The performance of these applications depends on the speed of the multipliers. If the speed of these multipliers is very low then the throughput of the circuits will be reduced. Furthermore, negative bias temperature instability effect (NBTI) occurs when pMOS transistor is under negative bias i.e. (Vgs = $-V$dd). In this situation, the interaction between the inversion layer holes and the hydrogen-passivated Si atoms breaks the Si–H bond generated during the oxidation process, generating H and H2 molecules. When these molecules diffuse away, interface traps are formed. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (Vth), hence reducing the circuit switching speed. When this biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect. However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and Vth is increased in long term. Hence, it is important to design a reliable high performance multiplier. Similarly the corresponding effect on nMOS transistor is positive bias temperature instability (PBTI), which occurs when nMOS transistor is under positive bias. Compared with the NBTI effect, the PBTI effect is much smaller on oxide/polygate transistors, and therefore is usually ignored.

Generally traditional circuits use their critical path delay as overall clock cycle in order to perform the correct operations. In most of the cases, path delay is shorter than critical path delay as the overall cycle period will result in significant time waste. Thus the variable latency design was proposed to reduce the timing wasting occurring in traditional circuit.

Variable latency design was divided in to two stages.

1) Shorter paths. 2) Longer paths.

In this variable latency design the entire critical path delay of the circuit is divided in to two paths as shorter paths and longer paths. When the average latency of the circuit is less than the critical delay then the shorter paths are activated which are executed in one clock cycle. If the total latency of the circuit is more than the critical path delay then the longer paths are activated which are executed using two clock cycles. These research designs were able to reduce the timing wastes occurring in very long instruction word processor.

Razor is an approach for digital VLSI systems based on dynamic detection and correction in the speed path failures of the digital systems. This approach is used to tune supply voltage by monitoring error rate during the system operation. This error detection provides monitoring of system delay and accounts for global and local delay variations and also helps the circuit not to suffer from voltage scaling disparities. The timing violations in the circuit were detected by using the Razor flip- flop. These flip-flops were used to detect the timing requirements for the multipliers to produce their outputs and generate the error signal which can be used as the input signal to the Adaptive hold logic. This adaptive hold logic decides whether the operations can be completed in one cycle or it requires more cycles. This logic can be applied to column and row bypassing multiplier. The performance degradation due to the aging effects are reduced by using the adaptive hold logic and also errors in the circuits are determined with Razor flip-flops.

A.Paper contribution

In this paper the Aging aware reliable multipliers has been proposed with adaptive hold logic based on the variable latency design. This AHL can decide whether the input pattern requires one clock cycle or more than one cycle. In section 2 we introduced the background of column-bypassing multiplier and row-bypassing multiplier and variable latency design. Section 3 details variable latency multiplier based on column and row bypassing multipliers. In section 4 simulation results are presented. Sections 5 conclusions are

done.

2. Preliminaries

2.1. Column By-passing multiplier

The Normal AM is fast parallel multiplier which consists of (n-1) full adder FA cells as shown in Fig 1. Each cell has two outputs, sum bit which goes down and the carry bit which goes diagonally to the next FA stage. Column bypassing multiplier is the modification of the normal array multiplier. In this multiplier the operations of the full adders are skipped based on the number of zero bits in input bits of the multiplicand.

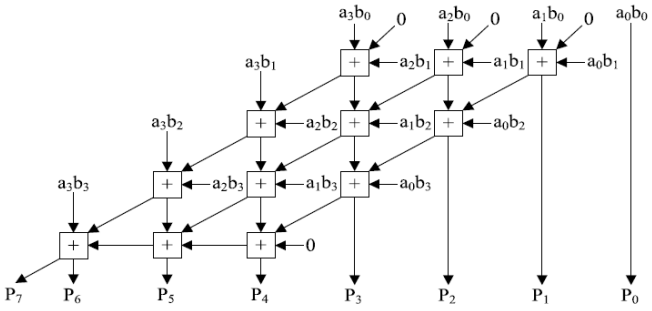

Figure 1: 4 x 4 Normal AM.

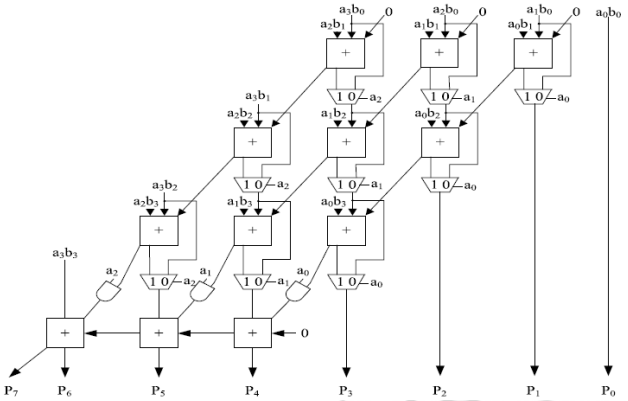

Figure 2: 4 x 4 Column bypassing multiplier.

Generally the FA's in AM are always active regardless of the inputs hence consumes more power but in column by-passing multipliers the corresponding FA operation is skipped whenever multiplicand bit is zero. Fig 2 shows a 4 x 4 column bypassing multiplier. Suppose if the inputs are 1100 * 1101, it can be seen that there are two zero bits in the multiplicand hence the FA's in the first and second diagonals have two of the three input bits as zero, hence the output of the FA will be the third bit which is the partial product a_ib_i. This bit will be directly bypassed to next stage by using the multiplier. The inputs to the FA's are blocked by using the tri-state gates based on the selector line a_i. Multiplexer uses the same bit as select line and bypasses the sum bit or the partial product bit a_ib_i. In this way the FA's operations are skipped to reduce the power consumption of the multiplier.

2.2. Row Bypassing Multiplier

A row bypassing multiplier is modification of normal array multiplier in which the operations of full adders are skipped based on the number of zero bits in the multiplier b_i. Fig 3 shows a 4 x 4 row bypassing multiplier.

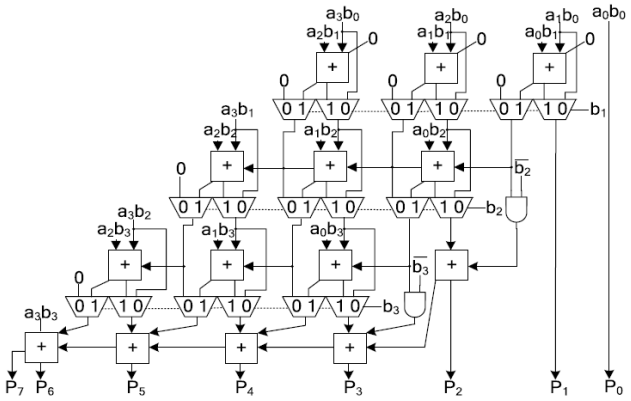

Figure 3: 4 x 4 row bypassing multiplier.

Suppose if the inputs to the multiplier are 1100 * 1001, two inputs to the FA's in the first and the second rows are 0, the multiplexers selects the partial product bit a_ib_i and bypasses it to the next stage and one more multiplexer bypasses the carry bit by selecting 0 bit initially. The tri-state gates blocks the inputs to the FA's in the first row and again in the second row. FA's operations are skipped, hence no switching activity occurs in the first and second rows of FA, and power requirements can be reduced. FA's in the third row are active since the third bit is nonzero.

2.3. Variable Latency Design

The variable latency model is proposed to minimize the timing waste occurring in the circuits which uses critical path delay as the execution cycle period. In this model we divide the critical paths in to shorter and longer paths. Shorter paths uses one clock cycle and longer path uses two clock cycle periods. Consider a 8-bit variable latency ripple carry adder as shown in Fig 4. A8-A1, B8-B1 are two 8-bit inputs, and S8-S1 are outputs. Suppose delay for each FA is one then the total delay for the adder is 8. Through simulation it is found that possibility of carry propagation delay longer than 5 is low, hence period is set to 5.

We will divide the carry propagation path in to two paths by considering the hold logic as shown in Fig 4. The function of hold logic is (A4 XOR B4)(A5 XOR B5). If the hold logic output is 0 either fourth or fifth bit doesn't produce carry, hence operation can be completed in 1 cycle period with delay less than 5. If the hold logic output is 1 means the operation requires two cycles with delay more than 5, since the hold logic notifies whether the operations require once cycle or two cycles to complete.

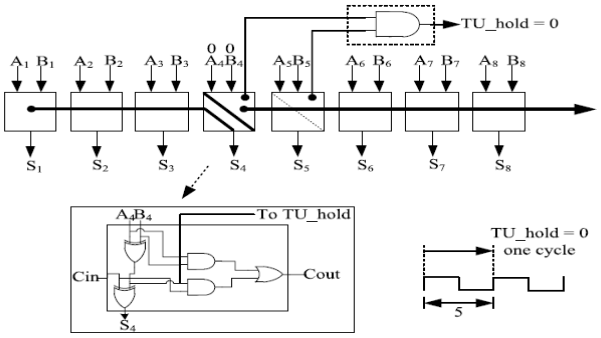

Figure 4: 8-bit RCA with hold logic circuit.

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3. Proposed Razor Based Aging Aware Multiplier

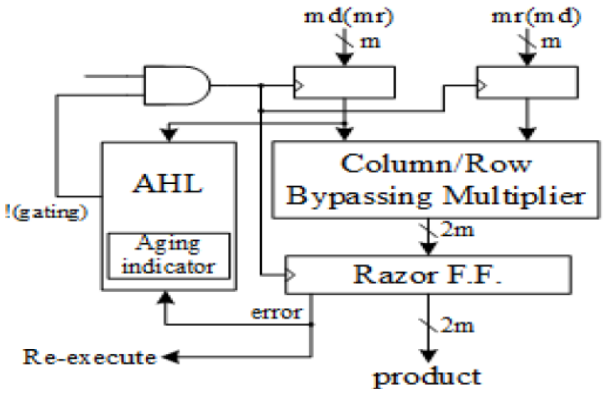

Figure 5: Proposed architecture.

Fig 5 shows the proposed architecture of multiplier with the adaptive hold logic. Two aging aware multipliers can be implemented using column and row bypassing multipliers. The input bits of the multiplicand and multipliers are sensed for number of zeroes and the decisions are done by the AHL circuit whether operations require one cycle or two cycle.

3.1. Razor Flip-Flop

A 1-bit Razor flip-flop is as shown in the Fig 6. Razor flip-flop is used to determine the timing violations caused by the multipliers. It consists of main flip-flop a shadow latch and XOR gate. The mail flip-flop catches the executed result from the combinational circuit with normal clock cycle and shadow latch catches the same result with a delayed clock cycle the XOR gate compares the both bits and generates the error signal.

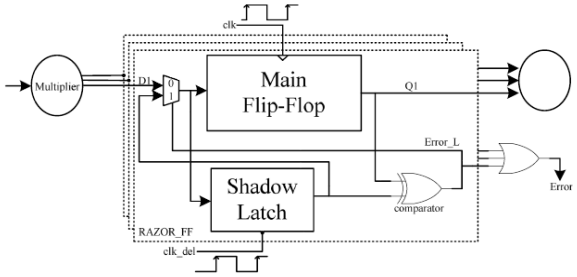

Figure 6: Razor flip-flop

If error occurs flip-flop will set the error signal to 1, which notifies AHL circuit to re-execute. Hence we use Razor flip-flop to detect the timing violations caused in the multiplier operations and decides whether the operation requires one cycle or two cycles by generating an error sign to AHL circuit.

3.2. Adaptive Hold Logic

Adaptive hold logic is the key component of the aging aware multiplier. Fig 6 shows the details of AHL circuit. It consists of aging indicator, judging blocks, mux and D flip-flop. Aging indicator in AHL circuit is implemented by counter which counts the number of errors during the operation and increments the counter whenever error occurs and resets to zero at the end of the operations.

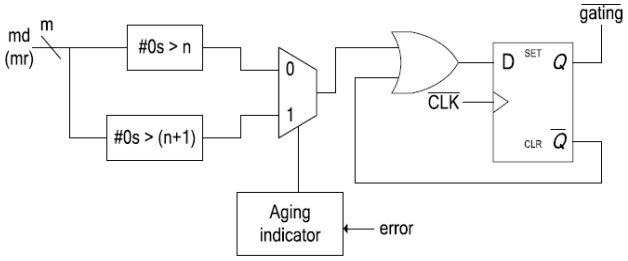

Figure 7: Adaptive Hold Logic.

The two decision making blocks are use to count the number of zeroes in the input bits of the multiplicand (md) in column bypassing multiplier and number of zero bits of multiplier (mr) in row bypassing multiplier. The first judging block gives output 1 if number of zeroes in md(mr)bit is larger than n (where n is positive number for 4-bit multiplier we consider it n as 2) and second judging block will output 1 if the number of zeroes in md(mr) are larger than n+1. These judging blocks are implemented to decide whether the input pattern requires one or two cycles. The multiplexer selects on of either result based on the aging indicator output, then OR operation is performed for output of multiplexer and Qb, which is given as input to the D flip-flop. When pattern requires one cycle multiplier outputs 1, hence the gating signal will become 1, hence the input of the flip-flop will latch the new data. When multiplexer output is 0 means the input pattern requires two cycles hence the OR gate will output 0 to D flip-flop. Therefore !gating signal will be 0 which disables the clock signals of input flip-flops of the multiplier in the next cycle.

4. Simulation Results

The proposed aging aware multipliers are implemented in verilog-HDL using Xilinx ISE 14.7v tools. The results are simulated for different input vectors using Xilinx ISim Simulator.

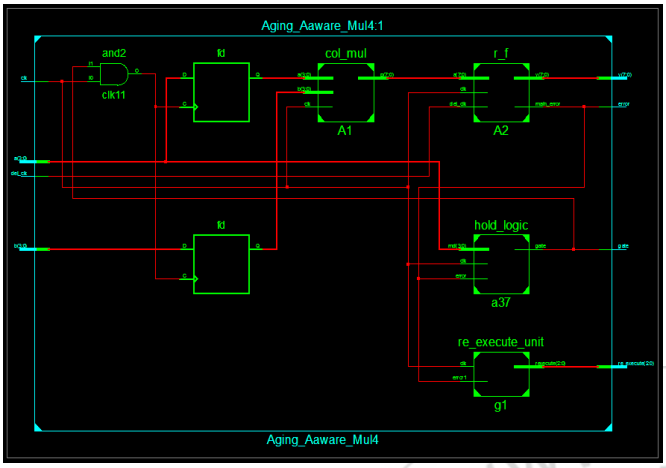

Figure 8: RTL Schematic.

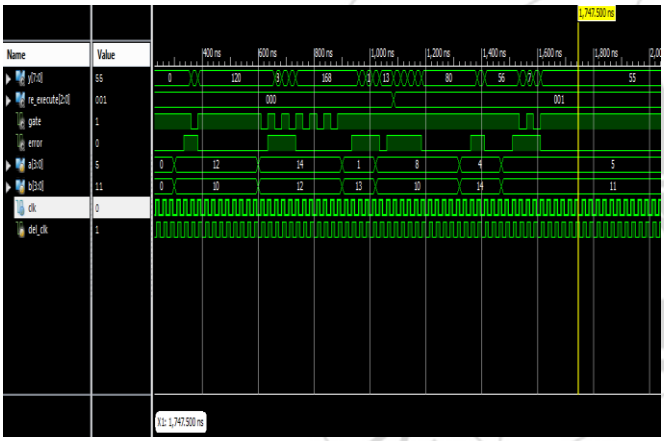

Figure 9: Simulation waveforms

5. Conclusion

In this the AHL circuit is proposed which decides whether the operations require one cycle or two cycles based on the number of zeroes in the input bits. The Razor flip-flops detect the number of errors and generate the error signal and acknowledge the AHL circuit to re-execute the operation. By using the AHL the timing violations due to aging effects can be avoided and overcome the performance degradation of the multiplier.

This variable latency design is used with the column by-passing multiplier and row bypassing passing multiplier to minimize the power requirements to the multiplier and the speed of operations can be achieved.

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