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# Implementation of Low Power Circuit Analysis with Applications of Test Vectors

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**Abstract:** An advanced approach to design a fault coverage test pattern generator by utilizing linear feedback shift register called Bit Swap-LFSR. This could perform fault analysis and also minimize the power utilization at circuit level during tests, by generating three intermediate patterns between random patterns by decreasing the hardware components usage. The main purpose of having intermediate patterns is to minimize the transitional processing at initial inputs; this could minimize the switching activities at circuit under test. By this the power consumption is decreased without any lose or damage in the hardware components. This experiment results by efficient multipliers circuits in proposed system, with and without fault confirm of fault coverage when the circuit has been tested.

**Keywords:** LFSR, Low Power Test Pattern Generation, BIST, ATE.

## I. INTRODUCTION

The most complex areas in VLSI are performance, cost, power dissipation is because of shift i.e. this ability consumed testing, because of short current flow and charging of load space, dependability and power. The demand for movable computing devices and communication systems are increasing quickly. The applications need low power dissipation VLSI circuits. This ability dissipation throughout take a look at mode is two hundredth over in traditional mode, hence the necessary side to optimize power throughout testing. The Power dissipation may be a difficult in the applications for today's System-on-Chips (SoCs) style and take a look at the ability dissipation [11]in CMOS technology is either static or dynamic. Static power dissipation is primarily because of the outpouring currents and contribution to the overall power dissipation is extremely tiny. [1]

A. Automatic Test Equipment (ATE):
Automatic Test Equipment (ATE) is that the instrumentation utilized in external take a looking to use test patterns to the CUT, to investigate the responses from the CUT, and to mark the CUT nearly as good or unhealthy in keeping with the analyzed responses. External testing ATE has a serious disadvantage, since the ATE (control unit and memory) is extraordinarily costly and value is expected to grow within the future because the range of chip pins will increase. There will be some value of increasing switching activity and eventually power dissipation of the circuit. The dominant consider the ability dissipation is that the dynamic power that is consumed once the circuit nodes switch from zero to one.
The most recent advances in semiconductor technology have led to transistor scaling of transistor dimensions, allowing a large number of devices to be fabricated on a single chip. The high integration has made power consumption. The power dissipation of a system in test mode is more than in normal mode. The extra power (average or peak) can cause problems such as instantaneous power surge causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of the product yield and lifetime.
BIST perform self-testing Associate in reducing dependence on an external ATE. BIST may be a Design-for-Testability (DFT) technique makes the electrical testing of a chip easier, faster, more economical and fewer expensive. It is the necessary factor to settle on the correct LFSR design for achieving acceptable fault coverage and consume less power. Each design consumes totally different power for same polynomial.

B. Applications of LFSR:
Pattern generator, Low power testing, Data compression, and Pseudo Random Bit Sequences (PRBS). Parameters embody the take a look at power, take a look at length (test application time), take a look at fault coverage, and take a look at hardware space overhead. Large and complicated chips need a large quantity of take a look at knowledge and dissipate a major quantity of power throughout take a look at that greatly will increase the system value.

## II.TESTING PHENOMENA ON LOW POWER TECHNOLOGY

Various authors explained about the concepts to cover with power problems during testing. Existing low-power testing scheme is divided into the following two categories.

(A) Low - Power Testing Techniques at external for External Testing
(B) Low - Power Testing Techniques at internal for Internal Testing

A. External Testing techniques based on low power:
The category contains various methods adopted to minimize the power consumption during external testing by ATE and depending on the number of transitions in test

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data set.[3] offer a heuristic method to produce a test sequences which create worst-case power droop by increasing the high- and low-frequency effects using a dynamically restrict to version of the classical D-algorithm for test generation.

A novel scan chain division algorithm [4] analyzes the signal dependencies and creates the circuit partitions such that both shift and capture power can be reduced when using the existing ATPG flows.[5] presents a low capture power ATPG and a power-aware test compaction method. This ATPG lowers the growth of test pattern count compared to the detection number. The peak power becomes less as the detection number increases. The test compaction algorithm further reduces the number of test patterns as well as the standard capture power.

This concept is to identify an input control pattern such that, by applying that pattern to the primary inputs of the circuit during the scan operation, the switching activity in the combinational part can be minimized or even eliminated. The basic concept of input control technique is to subset of scan cells is selected to give maximum reduction in test power within a given area constraint.

An alternate formulation of the problem is to deal with maximum permitted and allowed to test power and area overhead as constraints and attains a test power that is within these limits using the minimum number of gated scan cells, thereby leading to least impact in area overhead. The area overhead is guessable and closely corresponds to the average power reduction.

These examinations have greatly explored larger levels at the test vector reordering techniques to reduce the switching power. Hamming distance based reordering is described in survey paper.[6]

According to the references Vector compaction and data compression based on a static compaction technique to minimize the scan vector power dissipation. Carefully selecting the merging order of test cube pairs during static compaction reduces both average and peak power for the final conventional static compaction techniques that randomly merge test cubes.

Chandra and Chakrabarty on low power testing concepts propose a novel technique using test data compression for testing that reduces both test data volume and scan power dissipation.[7]

B .Internal testing techniques based on low power:

Various authors reported on techniques to cover-up with power problems during BIST. Several techniques have been reported to handle the low power BIST. The technique offer one consists of a distributed BIST control scheme that to make easier to understand BIST architecture for complex ICs, particularly during higher levels of test activity. The approach can schedule the execution of every BIST element to keep the power dissipation under mentioned limits. The technique decrease average power and avoids temperature-related problems but increase in test time.[8]

A BIST strategy called dual-speed LFSR is proposed and to reduce the circuit's during all switching activities. This concept utilizes two different-speed LFSRs to control those inputs that have transition densities. The low power test pattern generator is based on cellular automata, reduces the usage of test power in combinational circuits while gaining high fault coverage. Test time and area overhead remain genuine. Another low-power test pattern generator based on a modified LFSR is proposed.[9] The scheme decreases the power in CUT in general and clock tree in particular.

Initially consider the problem of low-power BIST for data path architecture built around multiplier-accumulator pairs. This technique offers two alternative architectures depending on low energy or low power dissipation. The authors based on both modified binary counters, operating as Gray counters, produces only one transition at a time. These architectures can achieve important energy and average power savings compared to conventional pseudorandom BIST.

The disadvantage of these techniques is circuit-dependent, suggests that non-detecting subsequences must be determined for each circuit test sequence. Other authors propose two other low-power approaches for scan-based BIST. Zhang, Roy, and Bhawmik propose modifying the LFSR by adding weight sets to tune the pseudorandom vector's signal probabilities and thereby decrease energy consumption and increase fault coverage.[6]

A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed [12]. In this technique, an LFSR generates almost similar probable random patterns. The technique produces random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the standard power. Girard et al. cope the problem of energy minimization during test application for BIST enabled circuits.

The main constraint is reducing energy consumption without modifying the stuck-at fault coverage. In this work, the authors first analyze the impact of an LFSR"s polynomial and seed selection on the circuit's switching activity during test application. They determine that the polynomial selection does not influence energy consumption; the LFSR"s seed selection is a more important parameter. Therefore, the authors propose a method based on a simulated- annealing algorithm to select LFSR's seed and provide the lowest energy consumption.

This architecture applied the most minimum number of test vectors needed to attain the required fault coverage and minimize the power. Many low-power techniques have been proposed for full scan and scan-based BIST architecture. The architecture proposed in changed the needed scan-path structure such that CUT inputs remain unchanged during a shift operation.[10]

A test pattern generator for scan-based BIST was proposed and that decrease the number of transitions that occur at scan inputs at the scan shift operation. Authors are proposed by a pseudorandom BIST scheme to reduce the switching activity in the scan chains. The activity and correlation in CUT is controlled by limiting the scan shifts to a portion of the scan chain structure using scan chain disable control.[13][14]

BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to Perform self-testing, i.e., testing of their own operation

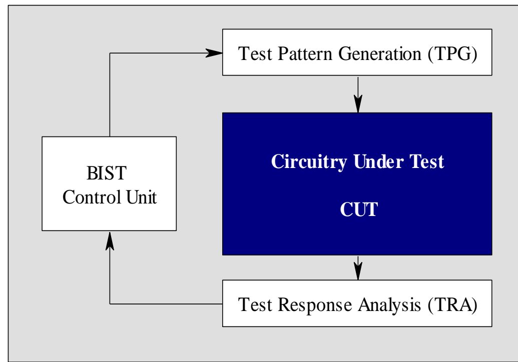


Fig. 1 BIST Implementation

(functionally, parametrically, or both) using their own Circuits, thereby reducing dependence on an external ATE.[15][16]

## III.IMPLEMENTATION OF BIST TECHNIQUE

A typical Built In Self Test(BIST) architecture consists of Test Pattern Generator (TPG) is generally implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR),Circuit Under Test (CUT) and BIST control unit as shown in fig.1.

A.CUT:

It is a part of the circuit test in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.

B.MISR:

It is designed for signature analysis, which is a technique for data compacting or reduction. MISR efficiently map different input streams to different signatures with every small probability of alias.

C.TRA:

It will check the output of MISR & verify with the input of LFSR & give the result as error or not.

D.TPG:

It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.[15]

E.BIST Control Unit

Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.

In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output. Test vectors applied to a CUT at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The result in more switching's and power dissipation in test mode.[11]

## IV. IMPLEMENTATION OF ALGORITHM FOR LOW POWER LFSR

In the simulation environment, the outputs of the flip-flops are loaded with the seed vector. The feedback taps are selected pertinent to the characteristic polynomial $x^8 + x + 1$. Only 2 inputs pins, namely test enable and clock are required to activate the generation of the pattern as well as simulation of the design circuit. It is also noteworthy here that the intermediate vectors in addition to aiding in reducing the number of transitions can also empirically assist in detecting faults just as good as the conventional LFSR patterns. Description of the technique to produce low power pattern for BIST The following is a description of a low power test pattern generation technique as depicted in the 9-bit LFSR based schematic in Figure. Verilog based test bench as shown in Appendix B is used in assigning the initial output states (0100 1011) of the 9-bit LFSR. The feedback taps are designed for maximal length LFSR generating all zeros and all one's as well.

A. Algorithm steps

The first step is to generate T1, the first vector by enabling (clocking) the first 4-bits of the LFSR and disabling (not clocking) the last 4 bits. This Shifts the first 4 bits to the right by one bit. The feedback bits of the LFSR are the outputs of the 8th and the first flip-flop. The output of the $8^{th}$ flip-flop is 1 and the output of the first flip-flop is 0. The exclusive-or of the $8^{th}$ -flip-flop (logic 1 in this case) and the first flip-flop (logic 0 in this case) is input (1 EXOR 0 = 1 into the first D flip-flop. The new pattern in the first four bits of the LFSR is 1010. Note that the shaded register is clocked along with the first 4 bits of the LFSR. So the input of the shaded flip-flop is the output of the $4^{th}$ flip-flop which in this case is 0. Also note that prior to the first clock, the input of the shaded register was the seed value of the $4^{th}$ flip-flop at the output of the $4^{th}$ flip-flop which in this case is 0. So after the first clock this value of 0 will now appear at the output of the shaded flip-flop. In other words the value of the $4^{th}$ output is stored in this shaded register and is used in the next few steps. The first 4 shifted bits of the LFSR and the last 4 un-shifted bits (i.e. the seed value) are propagated as T1 (1010 1011) to the final outputs. Next few steps involve generating the 3 intermediate patterns from T1. These patterns are defined as Ta, Tb and Tc shown in below flow.

Ta is generated by maintaining (disabling the clock to the first 4 bits) the first four bits of the LFSR outputs (as is from T1) as the final first four low power outputs 1010. Note that the clock to the last four bits of the LFSR is also disabled. The last four bits however are the outputs from the injector circuits. The injector circuit compares the next value (the input of the D-flip-flop) with the current value (the output of the D-flip-flop). According to T1, the outputs (current values) of the last 4 bits of the LFSR are 1011. The next values are the values at the inputs of the D-flip-flops which in this case are 0101.

Compare the current values (1011) bit by bit with the next values (0101). If the values bit by bit are not the same then use the random generator feedback R (in this case is logic 1) as the bit value as shown in the schematic above. If however both values bit by bit are the same then propagate that bit value to output as opposed to the R bit. This bit by bit comparison gives us the last four bits of Ta to be 1111. Therefore Ta = 1010 1111. Next step is to generate Tb. Shift the last 4 flip-flops to the right one bit but do not shift the first 4 flip-flops to the right.

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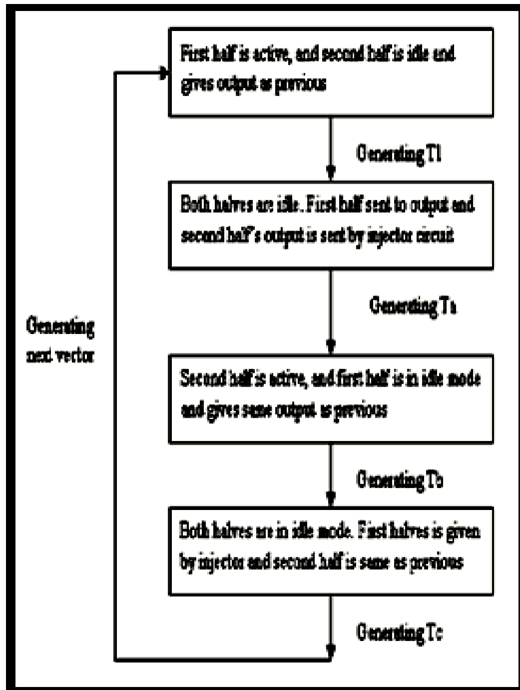


FIG2. Algorithm Steps for LP-LFSR

The clock to the first 4 bits plus the shaded flipflop is disabled. The clock to the last 4 bits is enabled. Propagate the outputs of the flip-flops of the entire LFSR as opposed to the outputs of the injection circuit to the outputs (low power). The injection circuits are disabled. As in Ta, maintain the first four LFSR outputs (1010) as the low power outputs. Again from Ta, the inputs of the last four D flip-flops from the previous step (generating Ta) are 0101. Also note that the output of the shaded register is 0 from the previous step (generating Ta). Therefore the input of the $5^{th}$ flip-flop is a 0. The outputs of the last 4 flip-flops are 0101 resulting in Tb = 1010 0101.

The $3^{rd}$ intermediate vector Tc is generated via disabling the clock to the entire LFSR. Propagate the first 4 outputs from the injection circuit as the first 4 low power outputs and maintain the last 4 low power outputs the same as Tb. Generating injection circuit outputs for Tc is conceptually the same as explained above in generating Ta. Current values (the outputs of the flip-flops) of the first four flip-flops are compared with the next values (the inputs of the flip-flops) of the flip-flops.

The feedback from the $8^{th}$ flip-flop is 1 (please see generating Tb). Therefore the logical feed forward value of R is 1. The feedback value from the first flip-flop is also 1 as per the current values above. The exclusive or of two ones is a 0. Therefore the input to the first flip-flop is a 0 which is also the next state of the first flip-flop. Hence the next values are 0 for the first flip-flop and 101 for the $2^{nd}$, $3^{rd}$ and $4^{th}$ flip-flop respectively. The latter values are 0101. The first four outputs from the injection circuit are 1111. The last 4 outputs are the same as Tb which are 0101 resulting in the $3^{rd}$ and final intermediate vector Tc = 1111 0101. Generating T2 is quite similar to generating T1. As in Tc the outputs of the last four LFSR flops are 0101. The outputs of the first 4 flip-flops of the LFSR are the current values which are 1010. Therefore the seed vector for generating T2 is 1010 0101. Shift the first four bits of the LFSR plus the shaded flip-flop. Do not clock the last four flip-flops. Propagate the outputs of the entire LFSR to the final low power outputs. The output of the $8^{th}$ flip-flop from the previous step (generating Tc) is a 1 and the output of the first flip-flop from the previous step (generating Tc) is also a 1. The exclusive or of the output of the $8^{th}$ flip-flop and the first flip-flop is 0. Therefore the input to the first flip-flop will be a 0. The inputs to the $2^{nd}$, $3^{rd}$, $4^{th}$ and the shaded flip-flops are 1010. These are also the current values from the previous step (generating Tc). Shifting the first four flip-flops of the LFSR to the right by one bit results in 0101 as the outputs of the first four flip-flops. Therefore T2 generated is 0101 0101.

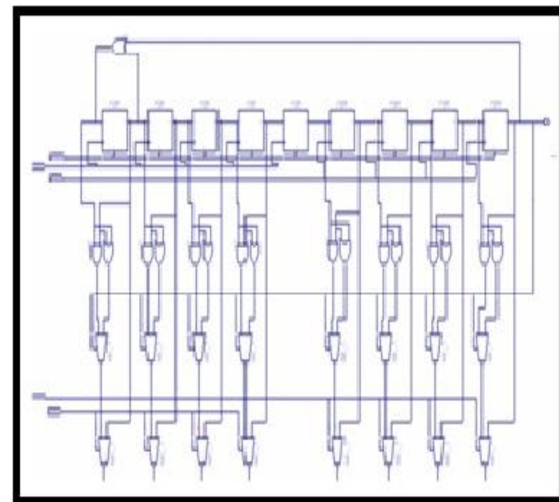

FIG3.Lowpower (LP) LFSR Architecture

In chip the power consumed by the chip under test is a measure of the switching activity of the logic inside the chip which depends largely on the randomness of the applied input stimulus. The existing technologies reduced correlation between the successive vectors of the applied stimulus into the CUT can result in much higher power consumption by the device. The increased power may be responsible for cost, reliability, performance verification, autonomy and technology related problems. The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR.

## V.RESULTS

A. Simulation

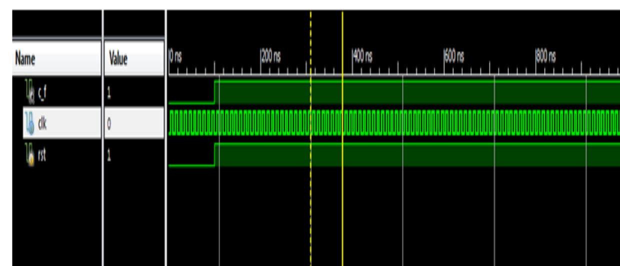


FIG4.Verification under LP-TPG'S

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B. Synthesis

1) Device Utilization Summary:

Selected device is spartan 3e 3s 500efg320-5

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 18 | 4656 | 0% |
| Number of Slice Flip Flops | 27 | 9312 | 0% |
| Number of 4 input LUTs | 24 | 9312 | 0% |
| Number of bonded IOBs | 3 | 232 | 1% |
| Number of MULT18X18SIOs | 1 | 20 | 5% |
| Number of GCLKs | 1 | 24 | 4% |

Fig4.Design utilization summary report

TABLE I POWER CALCULATIONS

| **Total device power** | 76mw |
|---|---|
| **Total LUT's of selected device** | 9312 |
| **Total LUT'S generated for top_propose module** | 25 |
| **Power generated for top_propose module** | 0.2mw [(25*76)/9312] |

TABLE II PERFORMANCE CALCULATIONS

| EVALUATED PARAMETER | GENERATED VALUE |
|---|---|
| **TOTAL DELAY FOR PROPOSED MODULE** | 6.319ns (4.887ns logic, 1.432ns route) (77.3% logic, 22.7route) |

## VI.CONCLUSION

The proposed approach shows the concept of reducing the transitions in the test pattern generated. The transition is reduced by increasing the correlation between the successive bits. The simulation results shows that how the patterns are generated for the applied seed vector. The power reports shows that the proposed low power LFSR consumes less power during testing by taking the CUT(**Verified multiplier**) and better performance by reducing the delay parameter.

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