Symmetrically Modified Laddered H-Bridge Multilevel Inverter with Reduced Configurational Parameters

Shyam D, Premkumar K, Thamizhselvan T, Nazar Ali A, Vishnu Priya M

Abstract: *Multilevel Inverters are incorporated in this modern world for medium and high-level applications for its adaptability to improve power quality problems. Its necessity is growing big in developing newer techniques and topologies for efficient implementation of DC to AC conversion system. Developing the MLI using less active switching components, less switching losses on active devices and improvement of number of voltage levels is always a tough task. A step forward to solve this problem is to modify the existing H-bridge multilevel inverter to produce Symmetrically Modified Laddered H-Bridge Multi-level Inverter (SMLHB -MLI). Comparative analysis has been carried out with other reputed existing MLI topologies to find out the performance and reduces complexity problem in inverter based on reduced switching methods in inverter side, reduction of active switching components and power diodes.*

Keywords: Multilevel inverter (MLI), Pulse Width Modulation (PWM), Symmetrically Modified Laddered H-Bridge (SMLHB), Neutral Point Clamped (NPC), Total Harmonic Distortion (THD)

I. INTRODUCTION

Generation of inverter technology provides solution to achieve higher power applications by connecting series semiconductor switches with many DC sources. The structural behaviour of multilevel inverter produces laddered network (staircase) at the output voltage [1][2]. Basically, Inverters are classified based on its structure, which is usually represented as symmetrical type structure and asymmetrical type structure [3]. Both these inverters are efficient in their own ways by improving the quality of the inverter output voltage [4]. Firstly, it provides a brief analysis on the functional parts of the inverter which is to be analysed carefully and then trying different switching strategy to produce harmonic free system. To better understand the operational principles of the inverter, basic knowledge of what type of system is need to be known. Both symmetrical and asymmetrical type inverters focus on reducing the number of input DC sources rather than reducing the power switches to the system. This brings complexity in the circuits which in turn brings the cost of the inverter to be high [5].

Multilevel inverter (MLI) proffer for high power capabilities, duly resulting in the reduction of level of harmonics and the commutation losses [6][7]. MLIs are used in variety of industrial and power related applications such as industrial motor drives, electrical motors, interfaced for renewable sources using solar/wind, active rectifiers, filters, static compensators and uninterruptible power supply (UPS) The main disadvantage is to bring down their complexity by increasing number of power devices and passive components, and rather complex control circuitry. This presents the features like output voltage boosting capability accompanied with capacitor voltage balancing problem [6]-[8].

Conventional multilevel inverters (MLI) are classified based on Neutral point-clamped MLI (NPC), Flying capacitor MLI, and Cascaded multilevel inverter. When compared to Neutral point clamped MLI and Flying capacitor MLI, Cascaded H-bridge MLI uses a smaller number of components to achieve same number of voltage levels and optimized layout circuit because each level shares the same structure and doesn't require extra clamping diodes or capacitors [5]-[9].

The major setback of Multilevel inverter is to bring down the switching losses, conduction losses, Total Harmonic Distortion (THD) and Harmonics which is added to the system. The primary concern is to reduce harmonics and THD analysis which is present in different multilevel inverter topology. This is incorporated to suppress the harmonics produced by the inverter at its output level [10]-[12]. The major reason for increase in switching losses and harmonics in the system is due to increase in switching components. The cascaded MLI is effective in reduction of selective harmonics which is why it is used in fuel cell applications and battery stored power devices [13]. Research focus has turned towards the improvement on inverter side and few results from various research paper have focused on the improvement of number of levels. As the number of levels in the inverter increases, the combined output waveform has a greater number of output steps [14]-[17]. Harmonic distortions are reduced with increase in steps. Smoothness of the waveform is proportional with increase in voltage level the waveform but the complexity of circuit increases with increase in components [18][19][20].

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Various developments in the inverter technology have taken place during a course of time. It might be on the topological side, battery size or different modulation techniques used. Despite of its growth, little concern on the inverter side looks to be harmonics [21][22]. It would create detrimental effect on switching components in both electrical as well as mechanical parts. This also determines the life span of the inverter [23].

Different modulation techniques such as Selective Harmonic Elimination PWM (SHE-PWM), Multi-carrier sinusoidal pulse width modulation (MC-SPWM) and other referenced technique [24]-[28] has been initiated to Hybrid multi-level inverter with new topology in sequence to reduce the THD level with minimum number of switches possible. This would bring down the cost and reduces the switching losses considerably [29][30].

The scope of developing new techniques and topologies in inverter is in rise among researchers [31]-[33]. Multilevel inverter is one among them which is widely used in high power applications. Researchers focus on the switching losses and stresses produced during switching as a result of attaining higher output voltage [34]-[40]. There are significant improvements in symmetrical configuration which provides a smaller number of DC sources added to the system. The drawback in both symmetrical and Asymmetrical configuration is the cascade connection which is added which has the greatest number of switches added to it. In proposed system, A modified ladder network pattern of symmetrical multilevel inverter is implemented with reduced number of active switches, DC sources and power diodes.

II. PROPOSED SYMMETRICALLY MODIFIED LADDERED H-BRIDGE MULTI-LEVEL INVERTER (SMLHB -MLI)

The proposed Symmetrically Modified Laddered H-Bridge MLI (SMLHB -MLI) is a hybrid combination of H-bridge comprising of 2 DC sources (V_1, V_2), 4 capacitors, 9 unidirectional switches (S_1, S_2, S_3…. S_9) and 12 freewheeling diodes connected across each switching sequence. Always bi-directional switching should be provided with almost care because it is a "converted unidirectional switching". That is Bi-directional switch (S_5) is converted to unidirectional switches in the SMLHB topology. Due to structural implementation of closed loop of the switching sequence, active mode switches present in the system should not be turned ON at the same time, otherwise different values of voltage (random) would appear across the load. The value of capacitors (C1, C2, C3, C4) would be identical to each other and also acts as a voltage divider. Important instruction to be followed while designing the hardware is to provide same capacitor value and that too from same manufacturer is better. The rating of the capacitor voltage must match with the minimum requirement of the DC source connected with the system.

For efficient implementation of the Voltage division rule across each capacitor, A large value of resistance (ceramic resistor usually in Mega Ohm) should be connected across each capacitor in parallel to produce same voltage across them.

Design of multilevel inverter (MLI) need to be done to incorporate renewable sources of energy such as solar, wind, hybrid methods to provide constant voltage to the system during peak time and off-peak time. Rooftop with green building will bring down pollution level and adapt few techniques. Selection of each component has to be handled carefully because these are one-time investment which should not be changed/modified continuously. For every modification or changes, its cost would increase. So, handling and selection process of each component is the most difficult part of the system.
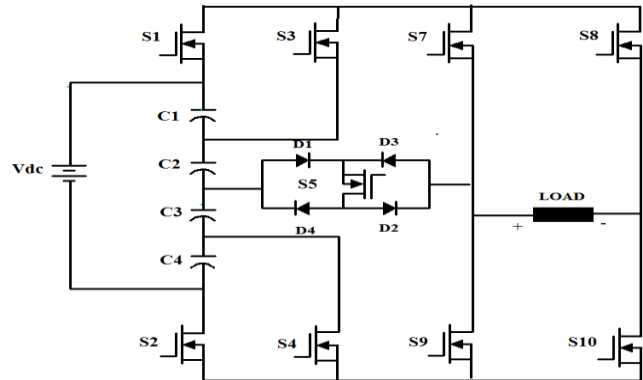

Fig. 1 Configuration of SMLHB MLI topology

Table I Modes of switching of *SMLHB* MLI

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	Output
1	1	1	0	0	0	1	0	0	1	+4
2	0	1	1	0	0	1	0	0	1	+3
3	0	1	0	0	1	0	0	0	1	+2
4	0	0	0	1	1	0	0	0	1	+1
5	0	0	0	0	0	1	1	0	0	0
6	0	0	1	0	1	0	1	0	0	-1
7	1	0	0	0	1	0	1	0	0	-2
8	1	0	0	1	0	0	1	1	0	-3
9	1	1	0	0	0	1	1	1	0	-4

As the proposed system is based on symmetrical level of implementation, the DC sources should be same value and identical in nature ($V_{dc} = V_1 = V_2$). The maximum operating voltage which is generated at the output side of the SMLHB -MLI topology is shown below in Eq. (1):

$$Voperating\ (max) = n\left(\frac{Vdc}{2} + \frac{Vdc}{2}\right) \qquad (1)$$

In order to reach the appropriate level in the symmetrical configuration, proper choosing of the magnitude level of DC source is required.

In order to provide proper switching of the SMLHB -MLI to produce 9 level output voltage: $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, $+4V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$.

The maximum number of voltage level can be attained by switching certain switches from S_1 to S_9 to operate in different mode condition which is described in Table 1. The converted unidirectional switch S_5 must be switched properly based on the direction of load current. The configuration and schematic diagram of different switching modes for the proposed SMLHB MLI is illustrated in *Fig. 1* and *Fig. 2*.

Mode 1: $V_0 = +V_{dc}$

Mode 2: $V_0 = +2V_{dc}$

Mode 3: $V_0 = +3V_{dc}$

Mode 4: $V_0 = +4V_{dc}$

Mode 6: $V_0 = -V_{dc}$

Mode 7: $V_0 = -2V_{dc}$

Mode 8: $V_0 = -3V_{dc}$
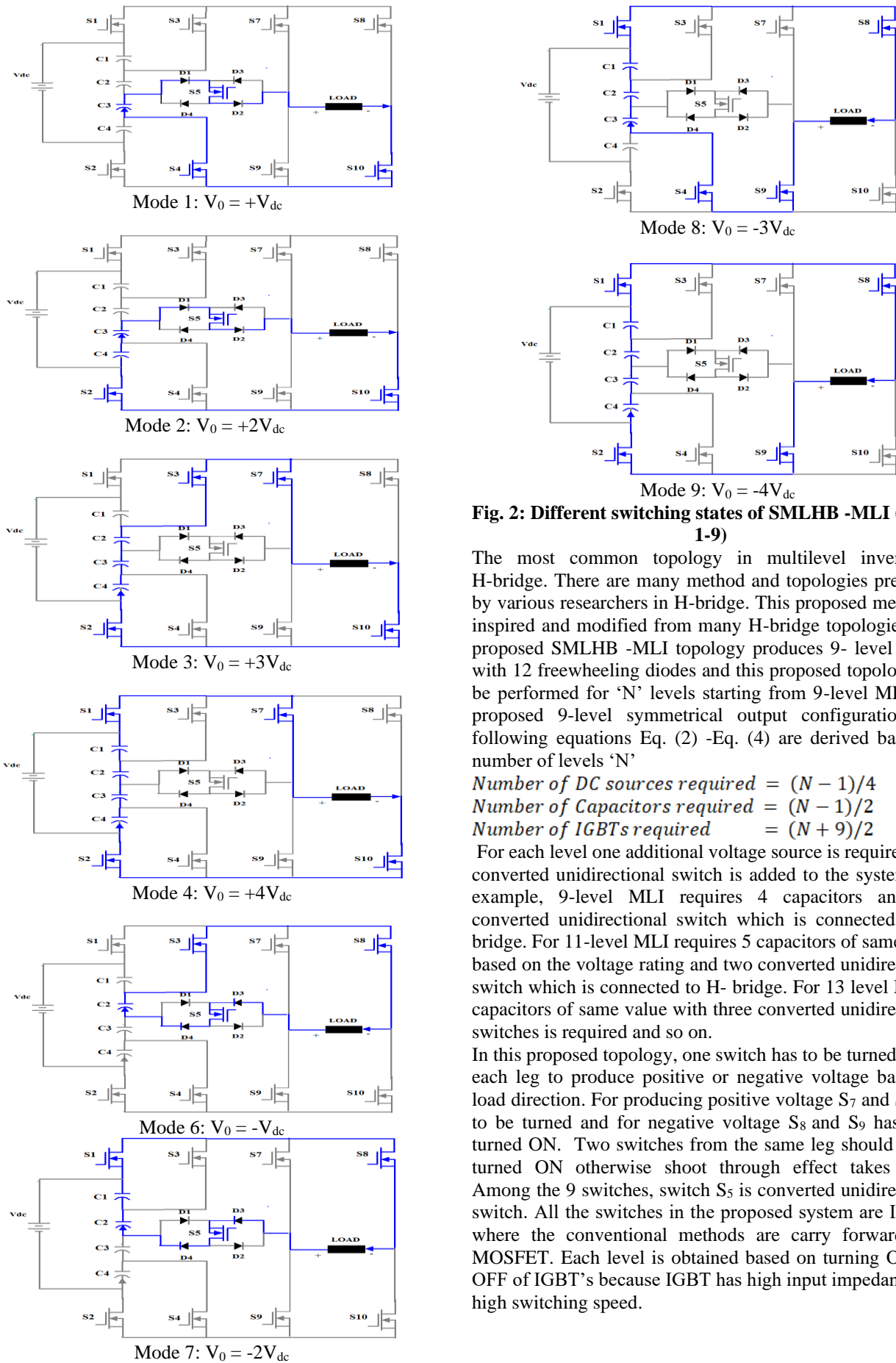

Mode 9: $V_0 = -4V_{dc}$

Fig. 2: Different switching states of SMLHB -MLI (Mode 1-9)

The most common topology in multilevel inverter is H-bridge. There are many method and topologies presented by various researchers in H-bridge. This proposed method is inspired and modified from many H-bridge topologies. The proposed SMLHB -MLI topology produces 9- level output with 12 freewheeling diodes and this proposed topology can be performed for 'N' levels starting from 9-level MLI. For proposed 9-level symmetrical output configuration, the following equations Eq. (2) -Eq. (4) are derived based on number of levels 'N'

$$Number\ of\ DC\ sources\ required = (N-1)/4 \qquad (2)$$
$$Number\ of\ Capacitors\ required = (N-1)/2 \qquad (3)$$
$$Number\ of\ IGBTs\ required = (N+9)/2 \qquad (4)$$

For each level one additional voltage source is required with converted unidirectional switch is added to the system. For example, 9-level MLI requires 4 capacitors and one converted unidirectional switch which is connected to H-bridge. For 11-level MLI requires 5 capacitors of same value based on the voltage rating and two converted unidirectional switch which is connected to H- bridge. For 13 level MLI, 6 capacitors of same value with three converted unidirectional switches is required and so on.

In this proposed topology, one switch has to be turned ON in each leg to produce positive or negative voltage based on load direction. For producing positive voltage S_7 and S_{10} has to be turned and for negative voltage S_8 and S_9 has to be turned ON. Two switches from the same leg should not be turned ON otherwise shoot through effect takes place. Among the 9 switches, switch S_5 is converted unidirectional switch. All the switches in the proposed system are IGBT's where the conventional methods are carry forwarded in MOSFET. Each level is obtained based on turning ON and OFF of IGBT's because IGBT has high input impedance and high switching speed.
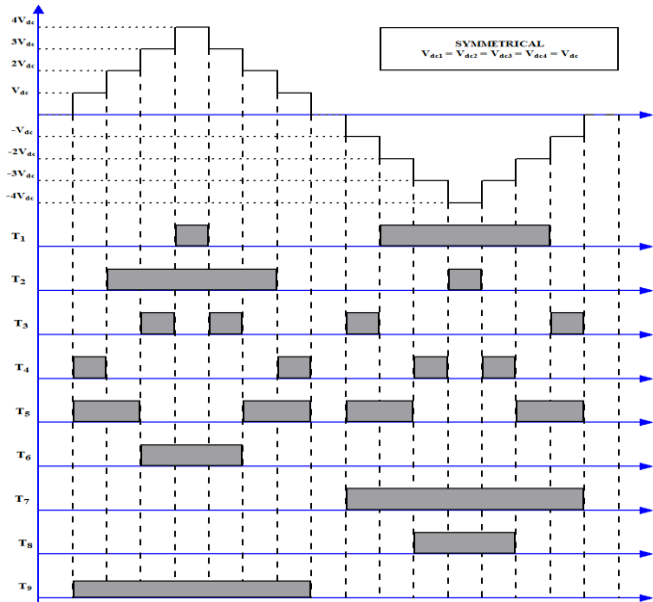
Fig. 3 Staircase output voltage waveform of SMLHB MLI

In the positive mode, S_{10} switch is always ON and in the negative mode, S_8 will be always ON. For producing $+V_{dc}$ (Mode IV), S_1, S_7, S_{10} and S_2 switches has to turn ON. For producing $+2V_{dc}$ (Mode III), S_3, S_7, S_{10} and S_2 switches is turned ON. For producing $-V_{dc}$ (Mode VI), S_1, S_8, S_9 and S_2 switches has to be turned ON.

III. SIMULATION RESULTS OF SMLHB -MLI

The proposed topology 9-Level SMLHB -MLI are simulated in MATLAB 2015a/Simulink model for resistive load which is shown in Fig. 4. The simulation results for the proposed system is carried for bo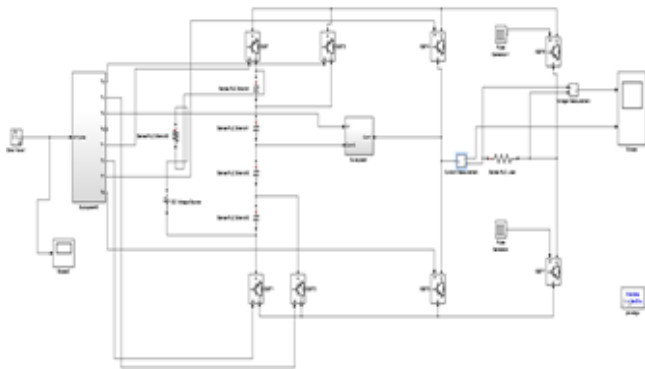th R and RL load. Among various modulation techniques, Multicarrier alternative phase opposition disposition (APOD) PWM technique is commonly used in single phase inverter system. This PWM scheme is used in SMLHB MLI system for the generation of gating signals. There are two major categories in multi-carrier based PWM techniques. They are based on phase shifted PWM technique and the other is level shifted PWM technique. Level based PWM technique is used for switching gates pulses for the circuit which is based on number of levels.

The selection of the symmetrical configuration uses identical value of DC sources ($V_1 = V_2 = 100V$). Therefore, the total DC voltage value is 200V. The Reference frequency is set as 50 Hz and carrier frequency used for both R and RL load is 4000 Hz. The primary focus of the proposed SMLHB -MLI topology is to find out the percentage of THD present in the system. In order to reduce the THD value, reduction of switching components is necessary. Table II shows the comparative analysis of different conventional topologies compared with the proposed topology based on the number of components used. The simulation results of unfiltered Output voltage and THD for resistive load [R= 50 Ω] is analyzed using Fast Fourier Transform (FFT) window in MATLAB simulation for 9-level SMLHB which is shown in Fig. 4 and Fig. 5. The simulated THD value obtained from resistive load of the SMLHB topology is 17.38%. The RMS voltage (V_{rms}) is 183.9V for resistive load. When the system is connected to RL load of value R= 50 Ω and L= 100 mH. The simulated THD value obtained from resistive- inductive load of the SMLHB topology is 5.17%. The results produced in the proposed system doesn't have any filter added to it.
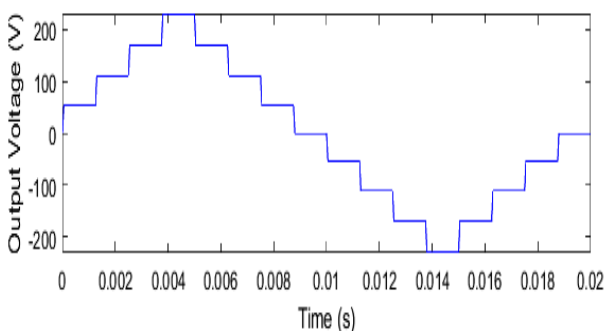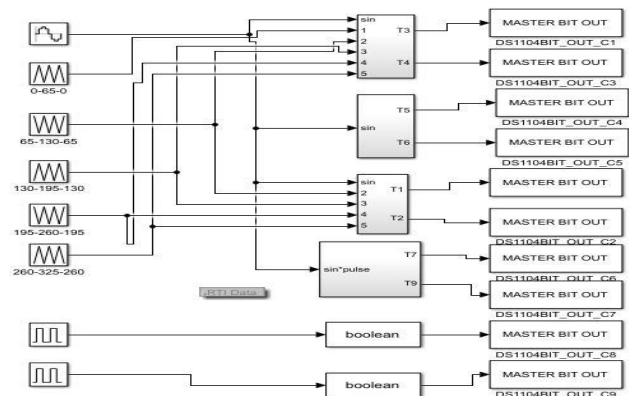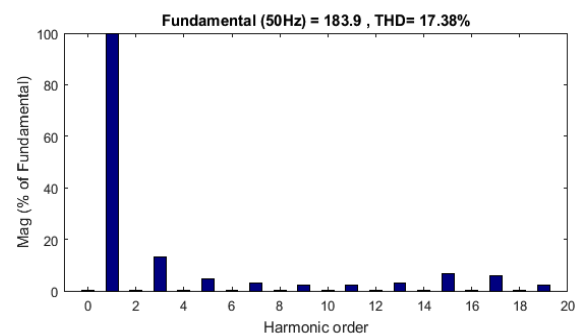

Fig. 4. Simulation results for SMLHB -MLI Simulation Circuit

Fig. 5. 9- Level simulated output voltage and corresponding THD using resistive load

In order to eliminate harmonics in the system, better design of filter is required. There are many filters with eliminates harmonics such as L, C and LC filters. Usually LC filter is preferred for single phase inverters because L and LCL performance adds complexity which in turn increases the cost.

The secondary focus is to reduce the losses in the system. These losses are caused by two major components. One is conduction losses and the other is switching losses. These losses play a vital role in deciding the efficiency of the inverter. Conduction losses are nothing but operational losses in the switches such as IGBTs/MOSFETs and the presence of freewheeling diodes present in the conduction path. Switching losses are produced due to turning ON and turning OFF of the switches (IGBTs/MOSFETs). In order to show the feasibility in reduction of losses in the proposed system, the following values $R_{switch} = 0.3\Omega$, $R_{diode} = 0.15\ \Omega$, $V_{switch} = 2V$, $V_{diode} = 0.9V$, $\beta = 1$, and ton = toff = 1µs were taken to find out the conduction losses and switching losses in the system.

$$Total\ loss\ (P_{loss}) = (P_{cond}) + (P_{SW}) \qquad (5)$$
$$(P_{loss}) = (P_{Switch}(t) + P_{diode}(t)\ ) + (P_{turn-on} + P_{turn-off}) \quad (6)$$

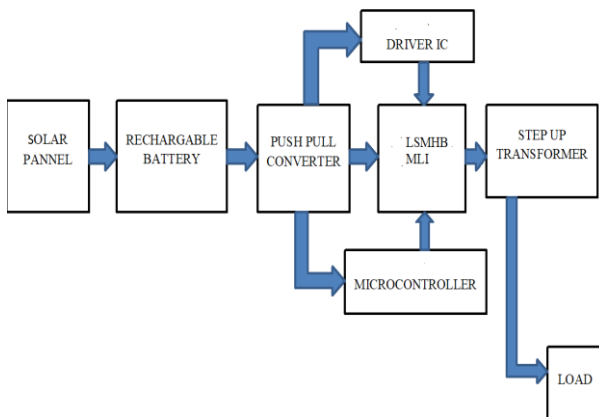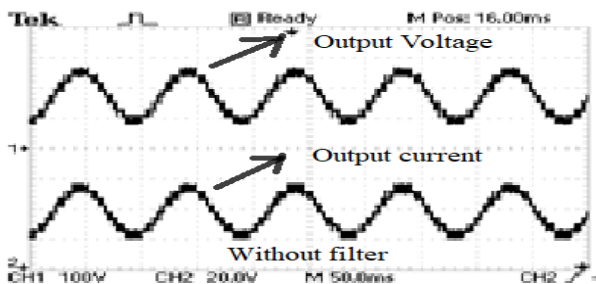Total power loss needs to be minimised in order to get maximum efficiency of the inverter.

The efficiency of the proposed SMLHB-MLI after using Multi-carrier PWM technique is 98.7%. This can be improved by using better implementation of different PWM techniques.
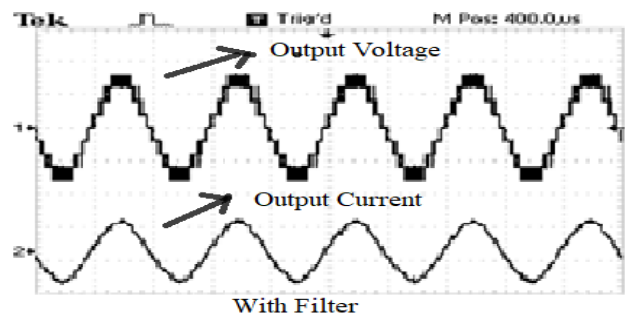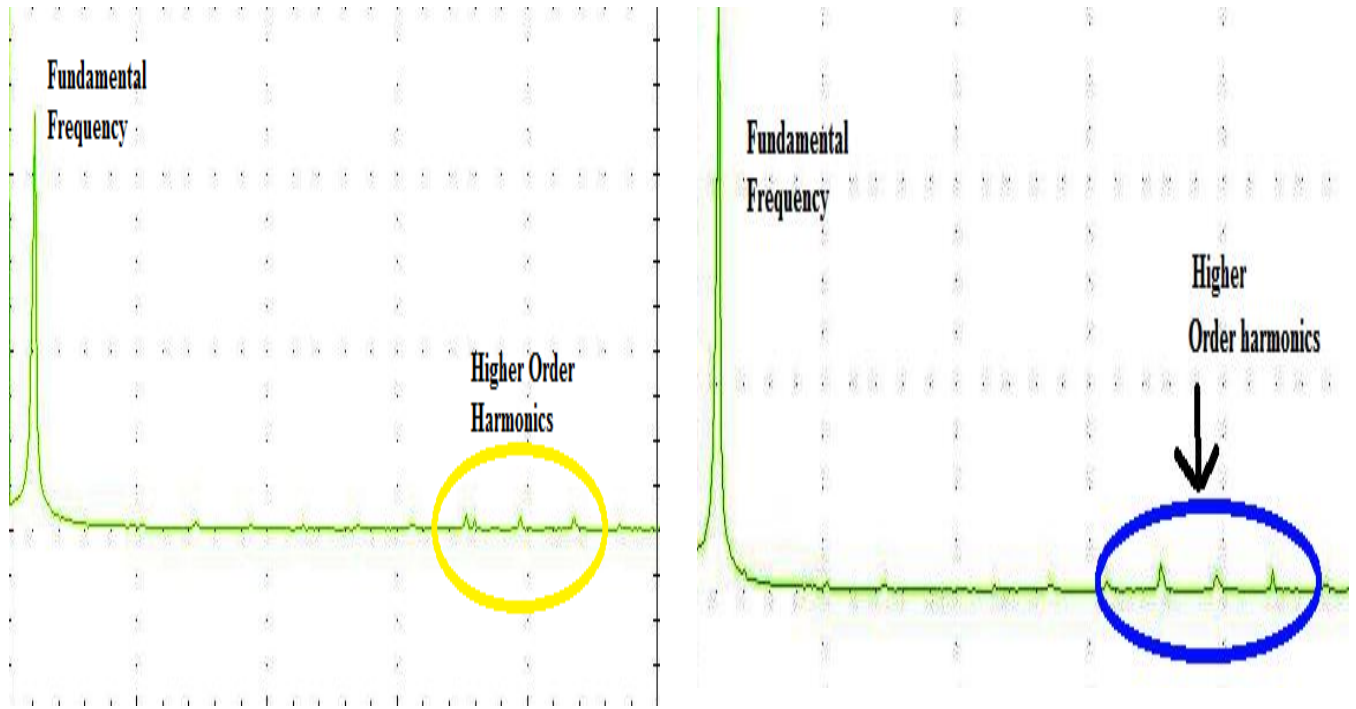
IV. EXPERIMENTAL RESULTS OF SMLHB -MLI

The proposed SMLHB -MLI system has been simulated for R and RL load. Simulation results has to be verified and tested in hardware also in order to prove its feasibility in both simulation and hardware. The hardware implementation of the proposed system is done using C2000 real time control MCU interfaced with MATLAB platform. The hardware implementation is done for 9- level multilevel inverter which is controlled by C2000 microcontroller.

Based on the experimental analysis for 9- level inverter, various factors need to calculated to find the better solution for inverter analysis. This system is performed for modulation index M of 0.9 for both R load. The values of R load are 50 Ω taken from the simulation results. The peak voltage from the hardware results is 200 V and the RMS voltage of magnitude is 164.2V. Fig. 6 shows the hardware configuration of SMLHB MLI. Fig. 7 indicates the output voltage and current waveform and its corresponding THD analysis is performed for R load for unity power factor without filter and with filter circuit.

Fig. 6. Hardware configuration and implementation of SMLHB MLI

(a) Without filter

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(b) With filter

Fig. 7. Hardware results for output end and THD for R load (without and with filter)

Table- II: Comparative analysis of different conventional topologies with SMLHB -MLI

Inverter Type	Flying Capacitor [12]	Neutral Point Clamped (NPC) [3]	Reverse Voltage Topology	Cascaded H-bridge	Switch Ladder Modified (SLMHB) [10]	Proposed Topology (*SMLHB*)
MOSFETs/IGBTs	6 (N-1)	6 (N-1)	3((N-1) +4)	6 (N-1)	(N-1)/2	(N+9)/2
Diode across MOSFETs/ IGBTs	6 (N-1)	6 (N-1)	3((N-1) +4)	6 (N-1)	(N+11)/2	(N-1)
Clamping diodes	0	3 (N-1) (N-2)	0	0	0	0
Isolated DC sources	(N-1)	(N-1)	(N-1)/2	3(N-1)/2	(N+3)/10	(N-1)/4
Flying Capacitors	3/2 (N-1) (N-2)	0	0	0	0	0
Total Number of Components	½(N-1) (3N+20)	(N-1) (3N+7)	(13N+35)/2	27(N-1) /2	11(N+54/11)/10	(7N+13)/4

V. CONCLUSION

This paper focuses on the basic analysis of Symmetrically Modified Laddered H-Bridge Multi-level Inverter (*SMLHB -MLI)* and their modes of operation are presented. The proposed system is used to generate output voltage based on number of levels with minimum number of switches and power electronic components used. Comparative analysis for various existing topologies were compared with the proposed system based on the number of DC sources, active switches and gate driver circuits. Lesser the switching frequency, lesser is the switching losses. This can be achieved by using Multi-carrier PWM technique as the novel method which is suitable for single phase inverter applications. The Simulation results and experimental results of the proposed Symmetrically Modified Laddered H-Bridge MLI has been carried and matched with results to prove its feasibility.

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