Research Article

Device Performance of Double-Gate Schottky-Barrier Graphene Nanoribbon Field-Effect Transistors with Physical Scaling

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Moore's law is approaching its limit due to various challenges, especially the size limit of the transistors. The International Roadmap for Devices and Systems (IRDS), the successor of International Technology Roadmap for Semiconductors (ITRS), has included 2D materials as an alternative approach for the More-than-Moore nanoelectronic applications. Among the 2D materials, graphene nanoribbons (GNRs) have been widely used as the alternative channel materials of field-effect transistors (FETs). In this paper, the impacts of physical scaling on the device performance of double-gate Schottky-barrier GNR FETs (DG-SB-GNRFETs) are investigated by using NanoTCAD ViDES simulation tool based on the tight-binding Hamiltonian and self-consistent solutions of 3D Poisson and Schrödinger equations with open boundary conditions within the nonequilibrium Green's function formalism. The extracted device performance parameters include the subthreshold swing and on-to-off current ratio. The results suggest that the performances of DG-SB-GNRFETs are strongly dependent on their physical parameters, especially the widths of the GNRs.

1. Introduction

Over the last few decades, the continuous scaling of transistors, as described by Moore's law, has resulted in astonishing innovations, especially in the semiconductor industry. According to Moore's law, the number of transistors in an integrated circuit would be doubled every 2 years [1]. However, the scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS) technology is expected to face its fundamental limit as it enters the sub-10 nm scaling regime [2, 3]. To leverage these shortcomings, various innovations involving field-effect transistors (FETs), such as the tunnelling FETs (TFETs) [4], nanowire FETs (NWFETs) [5], multibridge-channel FETs (MBCFETs) [6], and two-dimensional (2D) FETs, have been actively developed and studied. Interestingly, 2D material-based FETs have been listed as the potential candidates for further transistor miniaturisation in the International Roadmap for Devices and Systems (IRDS) [7]. Among the potential 2D

material candidates, graphene has attracted outstanding research interests among researchers since its introduction by Novoselov et al. [8].

Graphene possesses unique electronic and mechanical properties, but its gapless properties inhibit its application in FETs for switching applications (which typically require a band gap value between 0.1 eV and 3.0 eV [9]). Nevertheless, the band gap of graphene can be engineered by simply limiting its width, inducing the lateral confinement within its finite width and producing graphene nanoribbons (GNRs) [10, 11]. Theoretical works show that Armchair GNRs (AGNRs) have energy gap values which are inversely proportional to their widths. These widths can be classified into three families: the $3p$ group (with semiconducting properties), the $3p + 1$ group (with semiconducting properties), and the $3p + 2$ group (with metallic properties) [12]. The bandgap of the channel materials of FETs are crucial in the design of nanoelectronic devices [13].

Graphene is a 2D monolayer of carbon atoms constructed in the form of 2D honeycomb lattice. As a potential candidate for More-than-Moore CMOS technology, graphene offers several advantages such as high mobility for electron transport, high carrier velocity for fast switching, monolayer thin body for optimum scaling, and excellent thermal conductivity [14]. The band gap tuning of gapless graphene can be achieved by tailoring it into GNRs, enabling its application as digital switching devices, namely the GNRFETs [15, 16]. Careful selection of physical parameters of GNRFETs must be performed because the device performances of GNRFETs are strongly dependent on their widths. Previous studies showed that the carefully designed GNRFETs can have comparable current-voltage (I–V) characteristics as compared to silicon-based FETs [17]. In addition to the band gaps of the channel materials, the metal contacts in FETs are also important. Upon connection with metal contacts, Schottky-barrier (SB) is formed at the intersections between the GNR channel material and the contact metals [18]. Therefore, studying merely the electron transport properties within the GNR-based FET channels is insufficient to predict the overall performance of the GNR FETs.

In this paper, the simulation of double-gate SB-GNRFETs (DG-SB-GNRFETs) is performed using Nano-TCAD ViDES simulation tool [15, 16, 19]. Figure 1 shows the schematic structure of the SB-GNR-FET used in this work. Subsequently, the effects of physical scaling to the device performance of DG-SB-GNRFETs are also investigated. The remaining sections of this paper are organised as follows: Section 2 shows the theoretical equations employed in the NanoTCAD ViDES simulation tool [15, 16]. Section 3 compiles the results and discussions of this work. Conclusion of this study is drawn in Section 4.

2. Simulation Procedures

The performance of GNRFETs can be evaluated by using different carrier transport models such as simplified semi-classical transport model or quantum transport model. However, simplified semiclassical transport model does not treat quantum tunnelling effect and electrostatic short channel effect, making it difficult to explore the behaviour of GNRFETs due to physical scaling [20]. The quantum-based transport simulation approach is more efficient and accurate than that of other method. The NanoTCAD ViDES simulation tool performs the calculations based on the tight-binding Hamiltonian and self-consistent solutions of 3-D Poisson and Schrödinger equations with open boundary conditions within the nonequilibrium Green's function formalism [15, 16]. Non-equilibrium Green's function formalism (NEGF) formalism provides the atomistic description of the channel material, producing relatively accurate results in investigating the performance of GNRFETs in the sub-10 nm channel length regime [21]. Green's function [15, 16] can be expressed as follows:

$$G(E) = \left[EI - H - \sum_s - \sum_D \right]^{-1}, \tag{1}$$

where E is the energy, I the identity matrix, H is the Hamiltonian of GNR, and $\sum_s$ and $\sum_D$ are the self-energies of the source and drain. In this simulation tool, the transport is assumed to be completely ballistic and the type of graphene nanoribbon is armchair. This model assumes that the chemical potential of reservoirs is aligned at the equilibrium with Fermi energy level of the GNR channel. Given that there are no fully confined state, the electrons and holes concentration equations [15, 16] are expressed as follows:

$$n(\overrightarrow{r}) = 2 \int_{Et}^{+\infty} dE \left[|\psi s(E, \overrightarrow{r})|^2 f(E - E_{FS}) + |\psi_D(E, \overrightarrow{r})|^2 f(E - E_{FD}) \right], \tag{2}$$

$$p(\overrightarrow{r}) = 2 \int_{-\infty}^{Et} dE \left\{ |\psi s(E, \overrightarrow{r})|^2 [1 - f(E - E_{FS})] + |\psi_D(E, \overrightarrow{r})|^2 [1 - f(E - E_{FD})] \right\}, \tag{3}$$

where $\overrightarrow{r}$ represents the coordinate of the carbon atoms, f is the Fermi–Dirac occupation factor, and $|\psi_S|^2$ and $|\psi_D|^2$ are the probability of the states injected by the source and drain, respectively. E_{FS} and E_{FD} are the Fermi energy levels at the source and drain, respectively. Following that, the output current of DG-SB-GNRFETs [15, 16] are then simulated by using the following formula:

$$I = \frac{2q}{h} \int_{-\infty}^{+\infty} dE T(E) [f(E - E_{FS}) - f(E - E_{FD})], \tag{4}$$

where $T(E)$ is the transmission coefficient, q is the electron charge, and h is Plank's constant. In addition, the widths of the AGNRs with N_A dimers of carbon atoms are calculated by using the following formula:

$$W = (N_A - 1) \frac{\sqrt{3}}{2} a_{c-c}, \tag{5}$$

where $a_{c-c} = 0.142$ nm is the carbon-carbon bond length. To better illustrate the model in this work, Figure 2 shows the 3D structure of the SB-GNR-FET.

3. Results and Discussion

In this work, the DG-SB-GNRFETs are simulated with the scaling physical parameter, including the channel length (L_C), the gate oxide thickness (t_{OX}), and width of GNRs (W). For all the simulations in this work, the temperature and dielectric constant are fixed to $T = 300K$ (ambient temperature) and $\varepsilon_r = 3.9$, respectively. Table 1 shows the values that are used in the simulation of DG-SB-GNRFETs, whereas the physical parameters are shown in Figure 1.
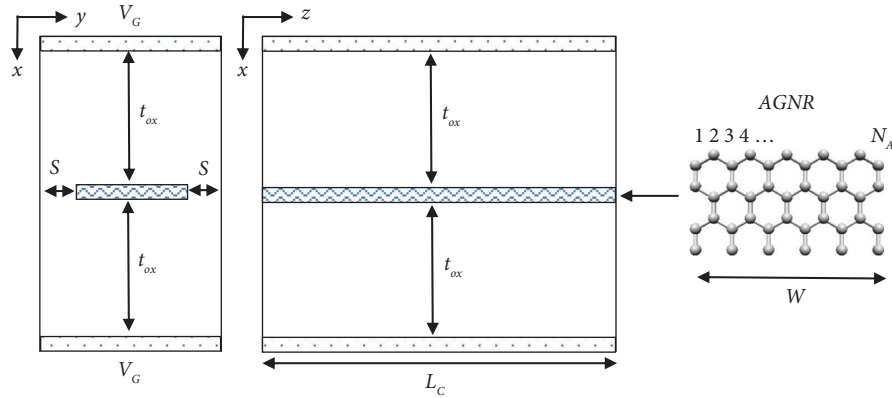
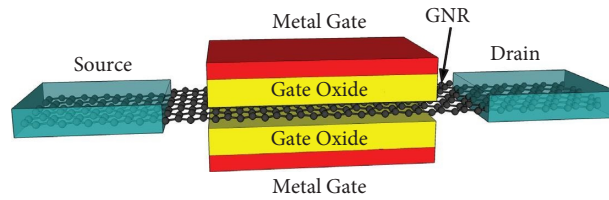FIGURE 1: Schematic structure of the SB-GNR-FET used in the simulation [19].

FIGURE 2: 3D structure of the SB-GNR-FET [19].

For simulation 1, the channel length (L_C) of DG-SB-GNRFETs is manipulated while fixing other physical parameters. For simulation 2 and simulation 3, the manipulated variables are the width of GNR channels (W) and gate oxide thickness (t_{OX}), respectively. All simulation results are analysed by extracting the on-to-off current (I_{ON}/I_{OFF}) ratio and subthreshold swing (SS) from I–V characteristics as shown in [22]. The I_{ON}/I_{OFF} ratio is one of the important parameter performances of this device that is related to the short channel effect and leakage current, whereas SS is an important measure of the performance for switching operation in FET devices. Figure 3 shows the I–V characteristics of DG-SB-GNRFETs with the width of $W = 0.98$ nm ($N_A = 9$), with their channel length scaled, at low ($V_D = 0.1V$) and high ($V_D = 0.3V$) drain voltages. Based on the I–V characteristics obtained, it is clearly shown that the I_{OFF} for $V_D = 0.3$ V is generally higher than that for $V_D = 0.1V$.

In Figure 3, the I–V characteristics do not show significant difference for different channel length. Theoretically, scaling down the channel length of transistor will be resulting the short channel effect on the transistor and therefore leading to current leakage. However, the I_{ON}/I_{OFF} ratio and SS do not show significant changes when the channel lengths of SB-GNR-FETs are scaled down from 14 nm to 7 nm, where only slight decimal points differences can be observed. This condition is observed due to the ballistic transport [23] assumption employed in the NanoTCAD ViDES simulation tool. Table 2 summarises the results of device performance of the SB-GNR-FETs with respect to channel length scaling. The device metrics summary clearly shows that the performances of SB-GNR-FETs are severely degraded at high drain biasing voltage. This

observation has also been observed in the previous study on SB-GNR-FETs [15]. Therefore, the subsequent simulations are carried out at low drain voltage, that is $V_d = 0.10$ V.

Figure 4 shows the I–V characteristics of SB-GNR-FETs with GNR width scaling. From the I–V characteristics in Figure 4, SB-GNR-FET with $W = 1.72$ nm has higher off-current compared to the SB-GNR-FET with $W = 0.98$ nm. This shows that the scaling of GNR width significantly affects the I_{ON}/I_{OFF} ratio due to the altered band gap values. In other words, increasing the GNR width reduces the band gap, and hence, increasing the tendency of band-to-band tunnelling and smaller Schottky-barrier height. Moreover, the SS of SB-GNR-FETs is also degraded significantly when the width is increased to $W = 1.35$ nm and $W = 1.72$ nm, while the SB-GNR-FET with $W = 0.98$ nm possesses SS value of 72 mV/dec, which is close to the ideal room temperature limit (SS = 60 mV/dec). Table 3 shows the summarised device metrics of SB-GNR-FETs with GNR width scaling.

Figure 5 shows the I–V characteristics of SB-GNR-FETs with three gate oxide thickness at 1 nm, 2 nm, and 3 nm. Table 4 lists the summarised device metrics of SB-GNR-FETs with gate oxide thickness scaling. Based on the gate oxide thickness scaling in Figure 5, it is shown that the oxide thicknesses of the SB-GNR-FETs have minimal impacts on their I–V characteristics. Although the SS and I_{ON}/I_{OFF} ratio are slightly degraded due to thicker gate oxide, the performances of the SB-GNR-FETs are still decent. This observation is most probably due to the excellent gate electrostatic control offered by the DG structure [24]. In summary, the results in this work imply that the widths of the GNR channels are the most significant physical parameter influencing the device performance of SB-GNR-

TABLE 1: Physical device structure of DG-SB-GNRFETs.

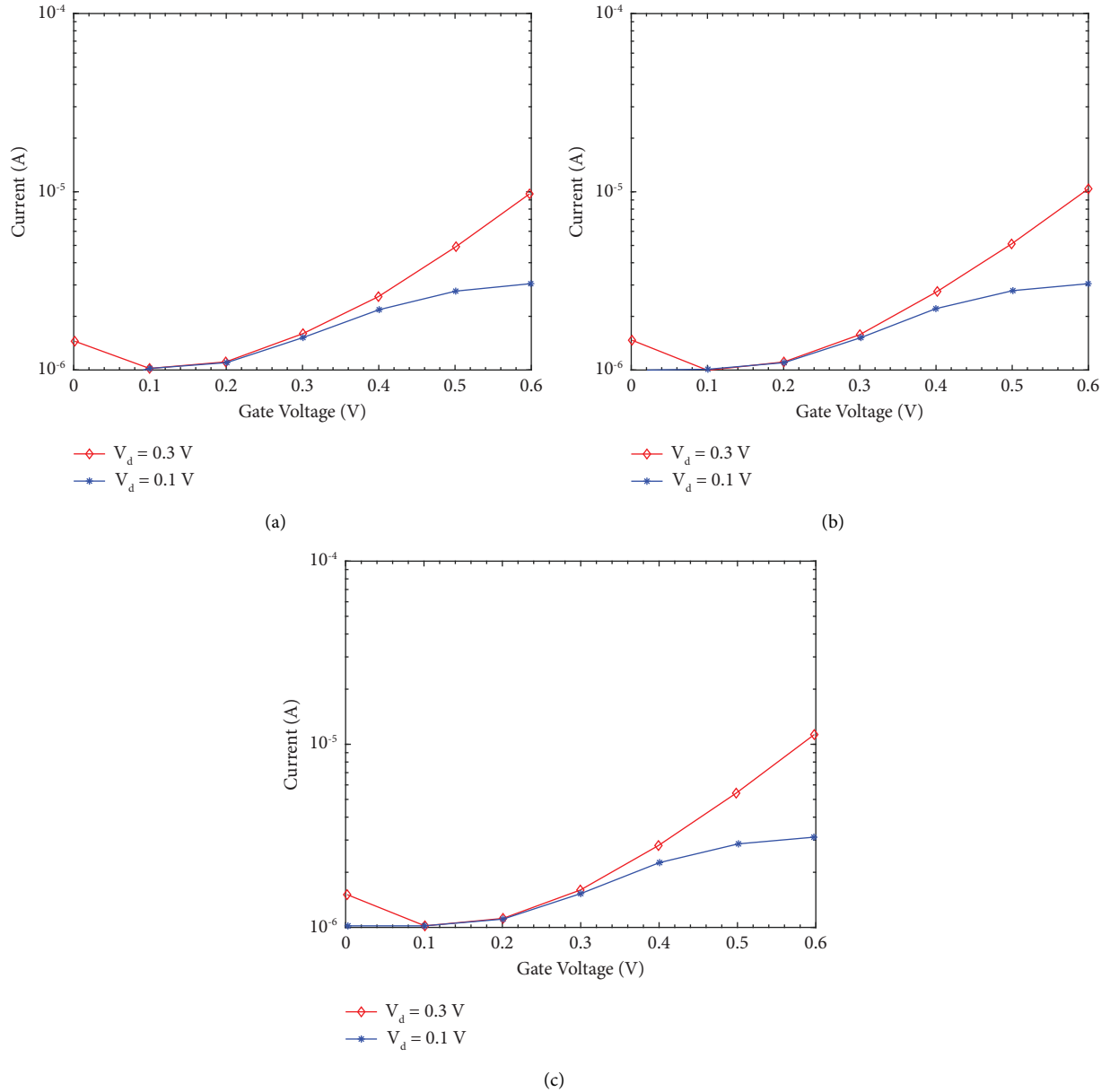| Physical parameters	Simulation 1	Simulation 2	Simulation 3
Channel length, L_C (nm)	7, 10, 14	10	10
Oxide thickness, t_{OX} (nm)	1.0	1.0	1.0, 2.0, 3.0
Dimers of carbon atoms, N_A	9	9, 12, 15	9
GNR width, W (nm)	0.98	0.98, 1.35, 1.72	0.98
Lateral space, S (nm)	1.0	1.0	1.0

(a)

(b)

(c)

FIGURE 3: I–V characteristics of SB-GNR-FETs with different channel lengths: (a) L_C = 7 nm, (b) L_C = 10 nm, and (c) L_C = 14 nm, simulated at low and high drain voltages.

Table 2: Device performance of SB-GNR-FETs with channel length scaling.

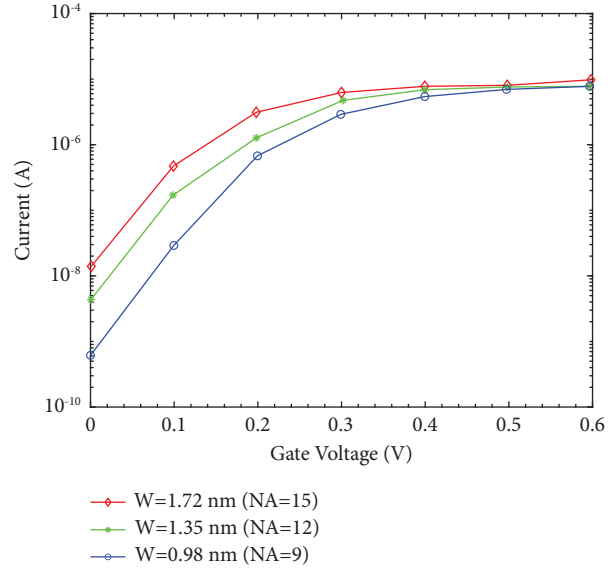| Device metrics	$V_d = 0.10$ V			$V_d = 0.30$ V		
	$L_C = 7$ nm	$L_C = 10$ nm	$L_C = 14$ nm	$L_C = 7$ nm	$L_C = 10$ nm	$L_C = 14$ nm
On-current, I_{ON} (A)	7.47×10^{-6}	7.52×10^{-6}	7.53×10^{-6}	1.52×10^{-5}	1.56×10^{-5}	1.61×10^{-5}
Off-current, I_{OFF} (A)	6.11×10^{-10}	6.11×10^{-10}	6.11×10^{-10}	2.55×10^{-6}	2.61×10^{-6}	2.67×10^{-6}
I_{ON}/I_{OFF} ratio	1.22×10^4	1.23×10^4	1.23×10^4	5.96×10^0	5.98×10^0	6.03×10^0
SS (mV/dec)	73.2	72.0	72.53	127.9	125.8	125.7

Figure 4: I–V characteristics of SB-GNR-FETs with GNR width scaling, simulated at $V_d = 0.1$ V.

Table 3: Device performance of SB-GNR-FETs with GNR width scaling.

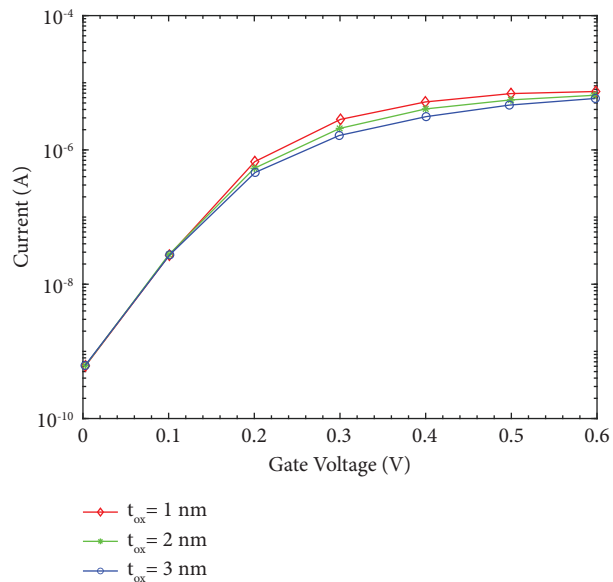| Device metrics	Width of GNR		
	$W = 0.98$ nm	$W = 1.35$ nm	$W = 1.72$ nm
On-current, I_{ON} (A)	7.52×10^{-6}	7.82×10^{-6}	9.47×10^{-6}
Off-current, I_{OFF} (A)	6.11×10^{-10}	4.25×10^{-9}	1.37×10^{-8}
I_{ON}/I_{OFF} ratio	1.23×10^4	1.84×10^3	6.92×10^2
SS (mV/dec)	72.0	114.1	123.2

Figure 5: I–V characteristics of SB-GNR-FETs with gate oxide thickness scaling, simulated at $V_d = 0.1$ V.

TABLE 4: Device performance of SB-GNR-FETs with gate oxide thickness scaling.

Device metrics	Gate oxide thickness		
	$t_{OX} = 1.0$ nm	$t_{OX} = 2.0$ nm	$t_{OX} = 3.0$ nm
On-current, I_{ON} (A)	7.52×10^{-6}	6.79×10^{-6}	6.06×10^{-6}
Off-current, I_{OFF} (A)	6.11×10^{-10}	6.11×10^{-10}	6.11×10^{-10}
I_{ON}/I_{OFF} ratio	1.23×10^{4}	1.11×10^{4}	0.99×10^{4}
SS (mV/dec)	72.0	76.4	80.6

FETs. In the future, this study can be extended by incorporating other band gap engineering techniques such as doping and defects [25].

4. Conclusion

In conclusion, the performances of SB-GNR-FETs with physical scaling are studied by using NanoTCAD ViDES tool. The performances of these devices are investigated by comparing the device metrics including the on-to-off current ratio and subthreshold swing. The results also show that DG structure can provide excellent gate control for GNR-based FETs. In addition, among the three physical scaling parameters investigated in this work, the widths of GNR channels are identified as the most vital design parameter that strongly affects the device performances of SB-GNR-FETs. The on-to-off current decreases and subthreshold swing increases when the width of SB-GNR-FET increases, causing its device performance to degrade. In summary, the physical parameters of SB-GNR-FETs must be carefully designed to achieve optimum performances for nano-electronic applications.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest.

Acknowledgments

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