PHYSICAL UNCLONABLE FUNCTIONS (PUF) FOR IOT DEVICES

Abdulaziz Al-Meer, Saif Al-Kuwari

Division of Information and Computing Technology, College of Science and Engineering Hamad Bin Khalifa University, Qatar Foundation, Doha-Qatar abal34183@hbku.edu.qa, smalkuwari@hbku.edu.qa

ABSTRACT

Physical Unclonable Function (PUF) has recently attracted interested from both industry and academia as a potential alternative approach to secure Internet of Things (IoT) devices from the more traditional computational based approach using conventional cryptography. PUF is promising solution for lightweight security, where the manufacturing fluctuation process of IC is used to improve the security of IoT as it provides low complexity design and preserves secrecy. It provides less cost of computational resources which prevent high power consumption and can be implemented in both Field Programmable Gate Arrays (FPGA) and Application-Specific Integrated Circuits (ASICs). In this survey we provide a comprehensive review of the state-of-the-art of PUF, its architectures, protocols and security for IoT.

Keywords Physical Unclonable Function · IoT security · hardware security · authentication · lightweight cryptography

1 Introduction

Preserving authenticity and confidentiality in IoT networks are major concerns for researchers and industries due to the increase reliance on these networks at many applications such as, sensors, monitoring and healthcare [1].

To address these concerns, PUF approaches have recently been proposed as a promising alternative to conventional cryptography, which is largely unsuitable to IoT network mainly because of its sheer computational requirement, which often degrade battery efficiency on the lightweight IoT devices.

Additionally, conventional cryptography is based on the hardness of solving some mathematical problems. However, advances in quantum computers may render such problems easy to solve [2][3][4].

Moreover, key distribution techniques used in conventional cryptography usually require a third party, which makes it impractical for IoT applications [5] as large-scale wireless network require keys to be frequently updated, and that will introduce high overhead on the network.

Finally, some conventional cryptography primitives such as, message authentication code (MAC), rely on the upper-layer mechanisms, which can be manipulated by adversaries e.g., spoofing attack.

On the other hand, PUF offers an alliterative solution for lightweight hardware security suitable for IoT networks. PUF is based on the fact that no two identical chips having the same characterization and going through the same production line will never share the same physical properties to inevitable manufacturing variation during the fabrication of the chips. [6]. PUF circuits exploit these features and utilize such variations to generate secret keys and authenticate IoT devices.

The rest of the survey is organized as following: section 2 provides a brief discussion on the fundamentals of PUF. Section 3 describes PUF performance evaluation and quality metrics. PUF authentication protocols are then introduced in section 4 followed by a thorough description of the popular architectures of PUF in section 5 with analysis of specific security requirements such as, strengths and weakness for each circuit design as well as performance evaluation comparison. In section 6, we discuss common PUF implementations, mainly focusing on FPGA implementation. Section 7 discuss threats and common attack against PUF. Finally, we conclude this paper in section 8 and discuss some potential future research directions.

1.1 Related work

Several survey were published on PUF considering both current PUF devices and emerging technologies. Babaei and Schiele [7] presented an overview of PUF for authenticating IoT devices and investigated the related challenges toward PUF exploitation. Similarly, the survey in [8] highlighted various silicon PUF, mainly on Ring Oscillator (RO) PUFs with related issues and challenges. Furthermore, Chang *et al.* [9] reviewed the improvement of PUF over past decade and demonstrate vulnerabilities of PUF. Halak *et al.* [10] presented an overview of PUF in term of principle and design challenges. A tutorial on PUF applications, error correction mechanism, PUF types and emerging technologies were presented in [11]. Moreover, the authors in [12] presented a review of the IoT network security challenges and investigate related attacks based on several IoT domains and discussed fuzzy extractors schemes for key extractions. In addition, Alkatheiri *et al.* [13] presented an experimental study of three designs in each of the two categories of PUFs: delay based and frequency variation PUFs. Table 1 provides a comparison between previous survey and ours.

1.2 Motivation

One of the attractive lightweight security solutions for IoT devices is PUF. Consequently, many researchers discussed and reviewed the emerging PUF technologies and their security challenges.

In addition, several PUF architectures have been proposed in the recent years. However, to the best to our knowledge, there is no comprehensive review of PUF that discusses important aspects of PUF, such as the recent PUF implementations, quality evaluations and security perspective for common and recent attack for different PUF architectures. This has motivated us to write this survey and provide such recent review for this rather important and emerging technology.

1.3 Our contributions

Our contributions of this survey are as following:

- We investigate the essential performance evaluation and quality metrics of different PUF category and design.
- We introduce recent PUF authentication protocols and compare them for lightweight devices, while showing how they mitigate common attack.
- We discuss different PUF architectures suitable for IoT applications, specially PUF designs implemented on FPGAs, which is becoming an attractive development platform.
- We investigate the most common threats and attack on PUF and discussed multiple assumptions and scenario.
- Finally, we discuss some open problems, identity gaps and make recommendations and directions for future work.

$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$					-		
	Ref.	PUF Applications	PUF evaluation	PUF protocol	PUF Architectures	PUF implementation	PUF Threats and attack
$ \begin{bmatrix} 8 \\ 14 \end{bmatrix} \checkmark \qquad x \qquad \checkmark \qquad \checkmark \qquad \checkmark \qquad x \qquad \checkmark \qquad \checkmark \qquad x \qquad \checkmark \qquad \checkmark$	[11]	\checkmark	х	\checkmark	\checkmark	Х	\checkmark
	[8]	\checkmark	х	\checkmark	\checkmark	Х	\checkmark
	[14]	х	\checkmark	х	\checkmark	\checkmark	х
	[10]	\checkmark	х	\checkmark	х	Х	х
	[9]	\checkmark	х	\checkmark	\checkmark	Х	\checkmark
	[13]	Х	\checkmark	х	\checkmark	\checkmark	х
	[7]	\checkmark	х	\checkmark	\checkmark	Х	\checkmark
This work \checkmark \checkmark \checkmark \checkmark \checkmark \checkmark \checkmark	[12]	\checkmark	Х	Х	\checkmark	Х	\checkmark
	This work	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark

Table 1: Previous Survey Comparison and contributions

2 **PUF fundamentals**

2.1 Definitions

The inherent unclonability of the PUF cannot be controlled as it is based on multiple random parameters that are generated during the manufacturing process. When the binary sequence applied to PUF system, it will react with corresponding response. That is, no two Integrated Circuits (IC) provide an identical response R for the same challenge C and this combination is called challenge-response pair (CRP). The PUF system contains uncontrollable random

components, so when the challenge C applied to the PUF system it will react with these components in a way to produce unpredictable and random response R.

These random components and the inability to control the manufacturing process make the PUF system unpredictable, unique, and more important, Physically Unclonable[15].

PUF system is considered physically disordered with the structural information as following:

- The related information of the PUF system could be extracted in a reliable way through measurement when different challenge C applied to the system to generate identical response R.
- Due to the large possible combination of challenges C, the corresponding response R cannot be predictable within restricted time.
- It is very hard and almost impossible to model, computationally and numerically determine and predict the challenge-response pair (CRP) based on the available information and current pairs.
- The PUF system cannot be cloned and reproduced due to the variation of the manufacturing process.

The physical characteristics of the PUF circuits can vary in term of: signals transmission speed, frequency oscillation, and the initial random state of the memory elements. These characteristics can be exploited to Physical Layer Security (PLS).

2.2 PUF Applications

The main goal of PUF is to ensure communication security and prevent possible attack. There are several applications of PUF that can be utilized for identification, confidentiality and to authenticate. Below we list some popular PUF application, each of which may prefer some PUF designs over others based on their requirements:

- *True Random number sequence generator*: usually used to generate keys for encryption in communication and digital signatures and create password to protect the system[16].
- *Malware detection*: Malware detection is one of the most time-consuming processes in hardware security. However, PUF can efficiently detect differences between original devices and malware injected device by examining the corresponding challenge-response pairs [17]. That is, when a chip is injected with malware, it will inevitably changes the power distribution of the device and that will deviate the response of the chip.
- *Detection of degraded hardware performance*: The performance of the chip can be degraded due to natural aging and time, as a result PUF challenge-response pair can detect such devices specially with the critical applications such as, aviation, military, and healthcare.
- *Hand weapon authentication*: Utilizing embedded PUF device to authenticate, secure the authorized users of a weapon. For instance, if the weapons are lost, no one other than its original owner will be able to use it [18].
- *Self-destruction electronics*: self-destruction is commonly required in the military and defense applications, such as when a devices is left in the battlefield [19]. In this case, PUF can inspect self-destruction signals, and only executes self-destruction if it passes authentication.

PUF has been widely used to provide essential security services, such as authentication and secret key generations, specially at constrained environments, such as IoT, where power consumption and security need to be balanced. In most applications, the main function of the PUF is to authenticate IoT devices as well as store the secret keys. The basic operation of PUF based security is to get a random choice of challenges bits to the PUF circuit and produce unpredictable and random response. Moreover, the manufacturing process variations of the PUF circuit has a unique silicon fingerprint, which provides a unique challenge-response pair (CRP) for each IoT devices even with the same input challenge bits [7]. Figure 1 illustrate the general operation of PUF where k-input bits represent the challenges and m-output bits provide the unique responses.



Figure 1: General operation of PUF

Several security criteria should be considered to achieve high secrecy. First, the response bits need to be correlated to the specific challenge's bits and is reproducible for the same challenge, despite any environmental factors, such as temperature and voltage. Second, the uniqueness of the CRP pairs should be verified by applying same challenges to different PUF circuit that must generate different responses. Third, the challenge k-bits need to be large enough to limits the searchable and predictable computational of the eavesdropper.

2.3 PUF categories

Several types of PUFs have been proposed, the authors in [20] categorized PUF as: memory-based PUFs, which exploit the initial binary sequences of memory when it is powered on, and delay-based PUFs, which use delay variations between propagation signals of the circuit. However, more commonly, other authors classified PUFs into three types: weak, strong, and controlled PUFs [21], each with it is own security properties and applications.

2.3.1 Strong PUFs

Strong PUF provides exponential growth in term of the number of CRPs pairs due to the large size of the circuits. However, while it would be impossible to efficiently recount all the CRPs pairs for large CRPs pairs, strong PUF is generally stable under environmental conditions changes. Strong PUF is also considered unpredictable, since CRPs contains multiple combination, and unclonable, where response can be readable without any additional information from the internal design of PUF. Strong PUF can be used for authentication and key establishment [6][21].

2.3.2 Weak PUFs

Weak PUF can be utilized for key generations and digital fingerprinting. However, it accepts limited number of CRPs and is increasingly linear. Compared to strong PUF, weak PUFs provide constant response under environmental conditions, utilize small number of CRPs pairs, and provides responses that are both unclonable and unpredictable.

2.3.3 Controlled PUFs

The controlled PUF use strong PUF as main block and adds a control logic to control challenges from being freely applied to the PUF circuit while preventing immediate readout of the responses. Therefore, the control logic can be utilized to hinder machine learning attack [22].

3 PUF performance evaluation

In this section, we discuss PUF performance evaluation and quality metrics that need to be considered while designing PUF circuits to achieve high security and prevent major attacks.

A comprehensive study of PUF performance to evaluate the security can be found in [23]. The first commercial performance evaluation based PUF-embedded for radio frequency identification (RFID) tags in [24] and the PUF performance evaluation by delay statistics presented in [25].

There are four essential parameters to evaluate on a PUF circuit, namely: uniformity, uniqueness, reliability, and bit-aliasing.

• Uniformity: the probability that the 0s and 1s are uniformly distributed in PUF's response R. Uniformity reflects the randomness of the response bit, and is calculated as the percentage of Hamming Weight (HW) of the response bit as shown equation in (1).

$$Uniformity = \frac{1}{n} \sum_{l=1}^{n} r_{i,l} \times 100\%$$
(1)

Where $r_{i,l}$ is the l - th bit of the response *n*-bit from a chip *i*.

• Uniqueness: The ability of PUF to distinguish a specific IC from other IC of the same structure when the same challenge C is applied to the PUF circuit. Technically, it is defined as Inter-device (Hamming Distance) between d different devices and the ideal value of uniqueness supposed to be 50%. If the two chip i and j $(i \neq j)$ have the responses R_i and R_j for the same challenge C, the average inter-device can be calculated as:

$$Uniqueness = \frac{2}{d(d+1)} \sum_{i=1}^{d-1} \sum_{j=i+1}^{d} \frac{HD(R_i R_j)}{n} \times 100\%$$
(2)

• *Reliability*: The PUF design must be able to reproduce the same response bit R to the same challenge C under fluctuation of the environmental conditions, such as supply voltage and temperature. The reliability of PUF can be estimated as an average intra-device (HD) and indicate the unreliable or noisy responses bits:

$$HD_{intra} = \frac{1}{s} \sum_{t=1}^{s} \frac{HD(R_i R'_{i,t})}{n} \times 100\%$$
(3)

Where R_i for the chip *i* measured at the normal operation condition and R'_i extracted at different supply voltage and temperature. $R'_{i,t}$ is the *t*-th sample of R'_i . The total of *n*-bit response obtained for *s* group. In other word, the reliability is reflecting the stability of PUF and it is measured with both equations (3)(4):

$$Reliability = 100\% - HD_{intra} \tag{4}$$

• *Bit-aliasing*: Bit-aliasing indicates the similarity of PUFs responses. When bit-aliasing occurs, different IC may produce identical response. The bit-aliasing of the *l*-th bit of an *n*-bit response is the average hamming wight of the *l*-th bit across several *k* devices. The ideal value is 50% and it is defined as:

$$Bit-aliasing = \frac{1}{k} \sum_{i=1}^{k} r_{i,l}$$
(5)

where k is the number of PUF devices and $r_{i,l}$ is the l-th bit of the response n-bit response.

4 PUF authentication protocols and key generation

In this section, we describe how PUFs circuit can be used to authenticate low cost devices, such as IoT devices and Radio-frequency identification (RFID), without resorting to conventional cryptography to maintain an acceptable low power consumption and reduce the overhead circuit area.

Authentication in PUF can be performed in two phases as shown in figure 2: the enrollment and verification phase. In the *enrollment* phase, the PUF circuit is directly connected to the server to receive the challenge bits, then the PUF provides the response bits to be stored and used later in the verification phase by the server. In the *verification* phase, since the PUF chip is implemented into IoT devices to be authenticated by the server, the server sends the original challenges bits that has been utilized in the enrollment phase and the IoT device reply with the generated responses bits. If the generated responses bits match any entry in the original (stored) CRPs table, the IoT devices is authenticated. Additionally, the response bits for PUF circuit can be used to extract secret key to ensure confidentiality when exchanging data [7]. Also, the challenges must never be reused to prevent man-in-the-middle attack and consequently predict the CRPs.



Figure 2: Authentication in PUF

In fact, authentication in PUF can be done in plaintext. The authors in [16] proposed key generation protocol using PUF circuits to be implemented with conventional cryptographic primitives (e.g., RSA). The key generation operation proceeds in two steps. First, the error correction code (ECC) consisting of initialization and regeneration to ensure that PUF circuit generates the same keys under variation of environmental conditions or fluctuations of power supply and temperature. Second, key generation is executed to transform the PUF output into keys.

Moreover, the PUF based lightweight protocol proposed in [26] authenticates IoT devices during an establish WiFi connection. It was shown that this protocol overcomes the security issues against several WiFi attack, such as, MAC

spoofing attack, invasive attack and evil twin attack by using only 3 CRPs to secure the connections [27]. A mutual authentication protocol based PUF was proposed in [28], which utilizes keys generated by PUF to authenticate IoT devices while using on the fly keys to avoid key storage. Furthermore, the authors in [29] introduced PUF based authentication protocol combined with exploiting wireless channel properties such as, Received Signal Strength Indicator (RSSI) to distinguish between legitimate and eavesdropper channels. Thus, data provenance is achieved in terms of confidence and data source e.g., locations and time. In addition, the authentication protocol based on continuously confirming the existence of device is proposed in [30]. This protocol was developed to detect the displacement of nodes through the link state changing using one CRP. Another work [31] proposed multi-factor authentication that depends on cryptographic primitive such as, hash functions and XOR gates with configurable PUF as the first factor and the second factor exploits channel characteristics such as, RSSI and Signal-to-Noise Ratio (SNR) as a fingerprint for the devices. Similar work [32] introduced two factor authentication protocol for Internet of Vehicles (IoV). This protocol relied on a combination of password and PUF to enhance the authentication mechanism, eliminate secret key storage in devices and ensure that the adversary cannot compromise the device even with the physical access. Table 2 illustrate the comparison between PUF authentication protocols.

|--|

Ref	Authentication method	Technique	Comments		
[16]	Authenticate individual ICs	PUF-based	Suitable for low-cost platform such as, RFIDs		
[26]	Wi-Fi authentication of IoT devices	PUF-based	Less resource and computation overhead using only 3 pairs of CRPs.		
[28]	Mutual Authentication Protocol	PUF-based	Used for real-time applications No need to store the generated keys		
[29]	Authentication privacy preservation	PUF-based and wireless link fingerprint	Mitigate against physical and cloning attacks. Low energy consumption compared to related protocols.		
[30]	Lightweight pairwise protocol	PUF-based	The protocol can detect nodes that have been removed or replaced		
[31]	Mutual multi-factor authentication	PUF-based and crypto- graphic method	Lower communication overhead. Three messages re- quired to achieve the authentication Fast to execute		
[32]	Two-factor authentication for IoV sys-	PUF-based and crypto-	There is no storage required of any secret data. They		
[32]	tem	graphic method	combine password with PUF (two-factor)		

5 PUF Architectures

In this section, we describe several PUF architectures suitable for IoT applications. We will also discuss the strengths, weakness, quality metrics and evaluation of common architectures as shown in table 3. The following criteria need to be taken into account when selecting a PUF architecture:

- 1. Robustness against different possible attack, such as machine learning attack and side channel attack [7].
- 2. Statistical properties and quality metrics such as:
 - Uniqueness: the ability of PUF circuit to generate a unique secret key when a challenges bit is provided.
 - *Reliability*: the ability of the PUF circuit to generate the same secret key under different environmental factors, e.g., temperature and voltages.
 - Randomness: the response bits generated from PUF circuit contain sufficient entropy.
- 3. The growth of the number of CRPs in strong and weak PUF need to be taken into account as it can lead to increased computational complexity, which, in turn, will consume power.
- 4. The PUF circuits need to be implemented easily in silicon chip.

5.1 Arbiter PUF

During manufacturing variations of multiplexers, different delay paths are formed, where one path is usually faster than others. Depending on the input challenges bits, each multiplexer will select the next path to be switched to, which provides multiple combinations of bit path selections. Arbiter PUF [33] operates by comparing two path delays as shown in figure 3 and generates a response bit '0' or '1' depending on the faster path being selected by the latch at the output.

Arbiter PUF is categorized as strong PUF. Moreover, to achieve practical statistic properties, all the delay-paths must have the same length. The arbiter PUF can be implemented in both Field Programmable Gate Arrays (FPGA) and application-specific integrated circuit (ASIC).



Figure 3: Arbiter PUF

In [34], a reconfigurable arbiter PUF presented with 4×4 switch block instead of the classical 2×2 . such that the 4×4 switch block can be reconfigured to increase the numbers of paths connection, which can be used for the applications that required regular keys generation. The authors in [35] proposed an energy efficient arbiter PUF using Current starved (CS) inverters at the back stage of each multiplexers. The proposed arbiter utilizes two RS latches and NAND gate instead of D flip-flop in classical arbiter to improve the propagation delay at the output phase. Therefore, the design alleviates effectiveness of fluctuating temperature at the output responses. Similarly, in [36], the authors demonstrated an energy efficient arbiter PUF that consists of 64 PUF cells using 45nm CMOS technology, each cell contains 8 switching elements which competes between different paths depend on challenge *C* values, 8 selecting modules, and an arbiter. The design achieves high uniqueness and consume low energy.

5.2 Ring Oscillator PUF

Ring Oscillator (RO) PUF [16] is based on the circuit oscillation between two voltage levels in specific frequency as shown in figure 4. By comparing two RO frequencies, the binary bits are generated based on incoming challenges bits. However, while the theoretical properties of RO PUF show that the oscillating frequencies must be the same, during the hardware manufacturing variations process it will inevitably cause some differences in the oscillation frequencies.



Figure 4: Ring Oscillator PUF

RO PUF is a strong PUF and can be implemented on FPGA. The main drawback of RO PUF is its sensitivity to the environment. To address this issue, the authors in [37] proposed configurable RO using only two hybrid logic gates, which is not only reliable under environment variation conditions, but also consumes less power and circuit area. The work in [38] further enhances the response entropy by adding configurable multiplexer with RO PUF circuit, which can

select from inputs challenges C based on proposed selection algorithm. The FinFET 20 nm technology based RO PUF proposed in [39] to overcome hardware overhead and power consumption of classical RO PUF, however they introduce frequency divider with flip-flop instead of counters, comparator to reduce power consumption.

5.3 SRAM PUF

One of the common PUF based on memory architecture is SRAM PUF [40] [41]. The main idea of SRAM PUF is to generate a response bit based on boot-up of SRAM cells, which are unpredictable; that is, when the SRAM is powered ON, the initial values of the single cells in the SRAM can be '0' or '1' randomly as they are considered noisy fingerprint. Furthermore, each SRAM has unique states during this boot-up period. Figure 5 illustrates SRAM PUF circuit.



Figure 5: SRAM PUF

However, SRAM PUF is weak PUF with limited number of CRPs and is mainly applicable for microcontrollers. Hence, more layers of security are required to thwart machine learning attacks. Additionally, SRAM PUF suffers from noise effects and requires error correction [7][40].

5.4 Hybrid PUF

Lightweight Hybrid PUF (LHPUF) [42] combines features of Arbiter PUF and RO PUFs to enhance the security as illusrated in figure 6. LHPUF consists of N to 1 multiplexers, two counters, NAND gate, NOT gate, and one arbiter circuit. The result of bit output response depends on the count of the number of '1's or '0's in the counter at the output. The authors in [42] implemented LH-PUF using FPGA (Xilinx) and it provides higher security performance as shown in table 3 compared to traditional arbiter PUF and RO PUF with less power consumption.

Another work [43] introduced FinFET based-PUF with two hybrid oscillator-arbiter PUF designs, which improved the power consumption and speed compared to traditional RO and arbiter PUF.

5.5 Optical PUF

The optical PUF was first proposed in [44][45] to demonstrate an inexpensive non-silicon system that consists of a token with the integrated three-dimensional micron scale glass as a physical system to generate 2400-bit unique key. The authors in [46] developed an optical PUF that can be implemented in Printed Circuit Board (PCB) by adding an imager and Light-emitting diodes (LED). These components are covered by polymer waveguide. However, the LED light is emitted and reflected by the waveguide to the imager to generate a unique number that can be used for authentication and key generation. Therefore, any invasive attack attempting to discover the unique key will destroy the waveguide coating, which damages the secret key. Rührmair et al [47] represent new image transformation that enhance the PUF entropy to measure the interference pattern through the optical PUF instead of detecting the reflection compared to the previous work in [44][45] with the same hardware cost.



Figure 6: LH-PUF

5.6 Memristor PUF

Memristor (refer to memory resistor) is first proposed in 1971 by Chua [48], which provides a relation between charge and flux. In 2008, HP labs [49] present a physical model of two-terminal device, which is based on switching process between two resistance states, such as high resistance state (HRS) (called OFF state, '0') and low resistance state (LRS) (called ON state, '1'). This state is changed when the voltage is applied to across terminals for specific period with two main operations: SET (that represent the change of state from HRS to LRS) and RESET (refer to transition from LRS to HRS). As a result, memristor is suitable for PUF due to the variability of the state and switching process. Also, it is used as True Random Generator [50]. Koeberl et al [51] proposed memristor PUF to exploits undefined logic state region based on memory functionality that depends on access time and applied voltage. Consequently, unpredictable sequence value is produced due to the utilization of the weak-write method. The authors in [52] present a single bit memristor PUF with two control signals that specify the writing and reading operation. On the other hand, the authors in [53] describe a multi bit memristor PUF as an entropy source based on the process variations of the write-time memristor cell. The Xbar memristive architecture [54] that consists of $N \times M$ size word-lines as a rows to receive the challenge bits N and bit-line as a columns to produce response bits M. The more Xbar rows size, the more randomness generated. An optimized and robust architecture based on memristive Xbar is presented in [55][56], which implements two memristive Xbar PUF utilizing two memristors devices and the logic circuit that processing the challenges and activate the PUFs.

5.7 Quantum PUF

Quantum PUF provides control on the unique parameters of the process variation that created the classical PUF. Škorić in [57] proposed quantum readout PUF (QR-PUF), which uses quantum state for both challenges and responses, usually to implement remote authentication protocols. By exploit the no-cloning theorem [58] of the quantum state, the adversary will be detected if they intercept the CRP. Another work [59] present quantum secure authentication (QSA), which rely on phase shaping of irradiate light pulse using spatial light modulator (SLM) and analyzer plane to detect the reflected response. The quantum confinement is described in [60] to provide a unique identifier for the devices by measuring the variation in resonant tunnelling diodes (RTD). A comprehensive study of the quantum PUF is presented in [61], which defines a quantum attack model and security parameters of the quantum PUF. The authors in [62] propose a quantum PUF to address the security issues of a workload scheduling algorithm threats for cloud-based quantum computers.

5.8 MRAM PUF

Magnetoresistive Random-Access Memory (MRAM) based PUF is proposed in [63] [64] to generate unique keys and provide authentication by exploit the variation geometric of the MRAM cell. The stream bits are stored in Magnetic

Tunnel Junction (MTJ) that consists of several layers. Due to the variation of the manufacturing process, the geometric of the cell vary in shape (rectangle or ellipse). Experimental evaluation of the MRAM PUF is presented in [65] with Thermally Assisted Switching MRAM (TAS-MRAM) method that are fabricated in dies. The experiment shows that TAS-MRAM consumes low power and high speed compared to SRAM. Furthermore, the authors in [66] proposed reconfigurable arbiter PUF based on hybrid Spin Transfer Torque (STT-MRAM/CMOS). The design employed the variation process of the transistors and MTJs connected in series with the control signals. The switch selection and pre-charge sense amplifier (PCSA) is used as an arbiter to determine the delays of the discharge current between paths. Therefore, the design provide sufficient entropy response and produce large and unpredictable CRPs compared to the silicon/classical arbiter PUF (section 5.1). The reliability enhancement/improvement of STT-MRAM PUF response is demonstrated in [67].

5.9 Carbon PUF

Carbon Nanotube Field Effect Transistor (CNTFET) based PUF is a promising technology to provide a unique signature with low power consumption. The first design of Carbon Nanotube PUF (CNPUF) is presented in [68], which is composed of pairs of CNTFET connected in series that share the same input voltage and response bits produced from comparing two stage currents. The simulation result in [68] shows that the CNPUF is reliable under temperature and voltage variation. The authors in [69] introduced CNTFET PUF cell, which compares the input voltage twice using two inverters and comparator. Similarily, the work in [70] demonstrated the fabrication of 400 CNTFET PUF device with same manufacturing process and evaluate their performance. The measurement show that the devices produce high quality metrics in term of uniformity and uniqueness. Ternary cycle operator based CNTFET PUF is proposed in [71] with two delays line using cycle operators.

5.10 Others PUFs

Several other PUF designs have been proposed to enhance the quality metrics, including:

- Glitch PUF[72]: exploits the glitch waveform variation of the logic gates.
- *Butterfly PUF*[73]: overcomes the initialization SRAM in some FPGAs making it suitable to be implemented on all FPGAs types.
- *Latch PUF*[74]: introduce a unique identification number (ID) for IC using cross-coupled NOR gates arrays, which improve the speed and power consumption.
- Digital PUF (D-PUF)[75]: improves the reliability of analog PUFs.
- Coin Flipping PUF (CF-PUF)[76]: exploits the convergence time of the bistable ring circuit.
- *Finite State Machine (PUF-FSM)*[77]: removes the need of error correction code (ECC) in Controlled PUF (section 2.3.3) and improve the security.
- Subthreshold current array PUF (SCA-PUF)[78]: exploits the I V characteristics of the two arrays of transistors and the response is produced based on the comparison between two output voltages.
- *Spin Orbit Torque (SOT) PUF*[79]: reconfigurable PUF based on Spin Orbit Torque (SOT) to stimulate the motion of the Domain Wall (DM).

6 PUF implementation

FPGA is widely used to simulate the design of PUF circuit due to flexibility, customizability and configurable logic gate as well as faster to be deployed in IoT devices. In this section, we discuss PUF implementation in FPGAs. We will cover only the architectures that are suitable for FPGA implementation. Table 3 summarizes the quality metrics and evaluation of designs in this section.

6.1 Arbiter PUF on FPGA

Many types of Arbiter FPGA PUFs has been proposed to improve the security of lightweight devices. The authors in [80] proposed 3-1 Double Arbiter PUF with 3 arbiter PUF and 1 bit response and new mode of operation for wires connection to arbiter which enhance uniqueness of output responses. The feedback Oriented XOR flip-flop based arbiter (FOXFF APUF) [81] for identification applications and provides a uniqueness improvement compared to FFAPUF [82] by adding delay elements, such as, feedback flip-flop to the design. Another work [83] introduced a combination of flip-flop and XOR gates based arbiter which enhance the uniqueness to 16% using families of FPGAs and consume

more resources compared to [82] design. Flip-Flop Based Arbiter PUF (FF-APUF) demonstrated in [84] provides sufficient entropy and reliability compared to conventional arbiter PUF, which is suited for FPGA implementation and can be utilized in authentication protocols for lightweight devices. Moreover, the authors in [85] introduced the new concept of bit self test (BST) based arbiter PUF by designing a detection circuit that produces reliability flag. BST depends on propagation delay between paths and fluctuations in temperature and voltages. Therefore, based on the reliability flag a robust responses generated, which is suitable for key generation and authentication.

6.2 RO PUF on FPGA

One of the alternative solution to conventional RO PUF is Transient effect ring oscillator (TERO-PUF) [86], which exploits oscillation of four 64-loop TERO cells; each cell consists of cross-coupled circuit of 2 AND gates and 2 inverters. The design thwarts electromagnetic attack [87], which analyses electromagnetic emanation and obtains information from RO circuit. However, the circuit utilizes more hardware resources. Furthermore, the authors in [88] introduce Phase Calibration Process (PCPUF) technique to precisely measure the frequency of 128 RO array, which improves the stability and reduces the bit error rate of responses. In addition, the authors in [89] demonstrated Galois ring oscillators (GARO-PUF) that compares different statistical parameters, such as, variability and location of implemented PUF in FPGA of oscillators instead of frequencies, so the design overcomes the systematic issues that produced by RO frequencies and correlations when RO PUF implemented in some physical locations in FPGA. The RO PUF based Lookup Table (LUT) FPGA introduced in [90] extracts more entropy by applying proposed method called Difference on Summed Difference (DSD) to obtain the differences between frequencies. The design achieved sufficient entropy with low area overhead. Moreover, the authors in [91] proposed two schemes: parallel and serial based RO PUF, and replace the counters with Linear feedback shift register (LFSR) to eliminate the linear behaviour in counters. However, the problem of linearity still appear in LFSR, so the scrambler circuit is also proposed to obliterate the correlation behaviour. Therefore, the design produces unpredictable output and consumes low area and power. In [92], a reconfigurable XOR gate based RO PUF is proposed, which produced larger CRP and enhance responses stability; reconfigurable XOR gate implemented in the RO circuit instead of inverter.

6.3 LFSR PUF on FPGA

Generally, Linear feedback shift register (LFSR) has been widely used as Random Number Generator (RNG) in cryptography, specially for lightweight devices with limited hardware resources. One of security concern associated with LFSR is its linearity and predictability. To address this, the authors in [93] proposed lightweight configurable Shift Register based PUF (SRPUF), with a non-linear function to improve the entropy and thwart machine learning attacks. Similarly, the work in [94] introduced LFSR-based strong PUF (L-PUF), which is a weak PUF at front-end of the circuit, such as Anderson PUF [95], combined with LFSR. Consequently, the authors in [96] proposed asynchronous LFSR based PUF (LFSR-PUF) that utilizes basic building block of the FPGA such as, LUTs and flip-flops, which exploits the variation process of LFSR circuit to produce random responses. Another work [97] proposed pseudo linear feedback shift register with multiple RO (PL-MRO) PUF, which utilizes logic gates instead of shift registers in LFSR to exploit the delay behaviour of the RO circuit. The PL-MRO PUF, produces sufficient entropy, high speed operation and low power consumption compared to conventional RO PUF.

6.4 Others PUF on FPGA

Several other PUF architectures have been proposed targeting FPGAs implementation and taking advantages of inherent FPGAs structures such as, LUT and flip-flops. For instance, the authors in [98] proposed an area efficient SR-Latch PUF with two methods of implementations that consist of 4 NAND gates with multiplexers to generate high entropy responses. In addition, the work in [99] introduced parallel scan design based PUF and exploits the delay difference between pairs of shift registers as chains through the SR-Latch arbiter to reduce the area overhead and improve the uniqueness. Consequently, a combination of weak PUF and pseudo Strong PUF (p-SPUF) were proposed in [100]. The weak PUF produces 1-bit response from the variation process of the logic gates, which feeds as an input to the LFSR. The design enhances the response randomness and can be well fitted in FPGAs due to low area cost. Furthermore, the dynamic reconfigurable PUF introduced in [101] based on 3 different logic circuit design stored in external memory, so the FPGA can be configured by the programming system (PS) that has an access to external memory to select between configurable logic. This technique improves the hardware overhead, provides large amount of CRPs and thwarts machine learning attack. Similar work [102] proposed transformer PUF based on reconfigurable properties of RO basic circuit such as, multiplexers which select between different paths and configurable XOR gates. As a result, transformer PUF improves hardware efficiency and reliability compared to conventional configurable RO. Moreover, a modified Anderson PUF with Low-density parity checker error correction (LDPC) is proposed in [103] to enhance the error bits in responses. The LDPC was utilized to provide reliability under environmental variations condition and high

uniformity. However, the design has less uniqueness which is not suitable for authentication applications. Another work [104] introduced optimization of Anderson PUF that utilized one configurable logic block (CLB) in FPGA with inherent XOR gates, which improves unpredictability of responses compared to conventional Anderson PUF.

7 Threat landscape and Security

In this section we discuss some attacks and threats on IoT devices based on PUF. We start by describing some possible attacks and assumption. Then we consider the following scenarios:

- Scenario 1: an adversary eavesdropping the communications channel between IoT devices.
- Scenario 2: an eavesdropper with physical access the devices.

In addition, the adversary can be active or passive; an active adversary can manipulate the operational temperature and power supply, while a passive adversary attempts to observe and intercept data in the communication channel. Ultimately, the physical access to the PUF chip is required for active attacks.

7.1 Brute-force

The attacker can try to clone the CRP table of the PUF circuit by enumerating all possible combination of challengeresponse pairs by repeatedly querying the PUF circuit. Clearly, this attack is very time consuming and will generate a huge CRP table requiring a considerable storage.

7.2 Invasive attack

This attack measures internal PUF properties, such as delays of the circuit, to predict the response for a particular challenge. Such measurement entails physically removing external packaging and chip metal layers. However, as any probing attempt will directly affect the wiring and routing of the circuit's delayed-paths, such actions will inevitably change the PUF chip characteristics or even destroy it [33]. This attack is both costly and impractical since the attacker needs specialized laboratory equipment while the IoT devices could be installed in protected or public areas.

7.3 Non-invasive attack

This attack attempts to intercept the communication channel between the device and the server without physical access to the internal components of the IoT device. In this case, the adversary intercept the authentication protocol that forms the challenge-response pairs and develop a machine learning models to predict them (see section 7.5). The Arbiter-PUF (section 5.1) is vulnerable to machine learning attack, which works by building a model that learns the correlation of known CRPs and predict the unknown CRPs. The authors in [108] introduced a defensive interface that improves the arbiter-PUF and similar design to resist the machine learning attack. Several designs have been proposed to overcome this vulnerability in the arbiter-PUF, such as XOR Arbiter PUF [16][109] and Feed-Forward Arbiter PUF [110] [105][111]. In addition, the authors in [112] evaluated various machine learning models such as, Logistic Regression (LR), Support Vector Machines (SVMs) and Evolution Strategies (ES) against Arbiter PUF. Moreover, the work in [113] demonstrated a a non-invasive attack against SRAM PUF based on chip correlation parameters, identical specification that sharing manufacturing process. The experiment showed that the adversary was able to guess approximately 45% of the CRPs for SRAM PUF.

7.4 Semi-invasive

This attack tries to access the PUF chip without destruction, so the adversary can apply multiple techniques, such as photonic emission analysis[114], to physically characterize the arbiter-PUF from the backside. In addition, other techniques, such as laser fault injection and optical contactless probing, have been demonstrated by [115] to predict the secret key from the PUF chip. Similarly, the authors in [87] proposed an electromagnetic analysis attack that identifies leakage frequencies of the Ring Oscillator PUF (section 5.2). However, these types of attacks still require specialized laboratory equipment.

7.5 Machine learning attack

Machine learning attack is the most popular and effective attacks on PUF. In this attack, the attacker intercepts the communication link between the device and the server without physical access to the internal components of the chip.

	PUF	Implementation	Uniqueness	Uniformity	Reliability	Hardware	Power
Ref	Architectures	Platform	(inter-chip)	HW	(intra-chip)	Overhead	Consumption
	Arenitectures	T hatform	HD	1177	HD	overnead	consumption
[105]	Arbiter PUF	TSMC 0.18 μm	23%		95.18% ^a , 96.26% ^b	1212µm×1212µm	137µW
[106]	Feed-Forward Arbiter	TSMC 0.18 μm	38%	—	90.16%		<u> </u>
[80]	3-1 DAPUF	Virtex-5	$\approx 50\%$	$\approx 50\%$	$\approx 88\%$	—	_
[81]	FOXFF APUF	Spartan-3, Virtex-6	42%, 44%	—	_	703 Slices	_
[83]	XOR FFAPUF	3 Types FPGAs	48% ^g	—	—	224 Slices ^g	—
[34]	Reconfigurable APUF	Simulation	50%	50%	_	4×4 switch blocks	—
[35]	CS-APUF	CMOS	46.8%	Pass NIST	99.2%	$3838 \ \mu m^2$	68.63µW
[84]	FF-APUF	Artix-7	41.53%	54%	97.10% ^a , 93.90% ^b	128 Slices	_
[85]	BST-APUF	Artix-7	49.1%	50.3%	$\approx 100\%$	150 Slices	_
[36]	Energy-Efficient APUF	CMOS	49.9%	50%	94.4% ^a ,97% ^b	$2168 \mu m^2$	6.63mW
[16]	RO PUF	Virtex-4	46.15%	—	99.52%	$16 \times 64 \text{ array}^{c}$	_
[86]	TERO-PUF	ALTERA DE1	48%	—	98.3%	416 ^r	—
[37]	Configurable RO	Artix-7	56.1%	50.36%	98.22 ^a , 99.56 ^b	$1128 \ \mu m^2$	119.4µW
[90]	RO based LUT	Kintex-7	49.15%	—	99.16%	8 ^s	_
[91]	Two schemes RO PUF	Spartan-7	46.4%	High entropy	99.68%	32 RO array (serial)	_
[92]	XOR-RO	Virtex-6	48.4%	Pass NIST	98.33%, 98.25% ^b	16 ^s	_
[94]	L-PUF	Alinx	49.66%	49.8%		210 ^s	_
[93]	SRPUF	Alinx	49.9%	49.8%	$\approx 100\%$	20,544 s	0.242W
[96]	LFSR-PUF	Spartan-3E	47.4%	_	95.8% ^a ,93.55% ^b	2 Slices	_
[97]	PL-MRO PUF	Artix-7	51.7%	High entropy	94.5%	_	$23.44 \mu W$
[95]	Anderson PUF	Virtex-5	47.9%		96.4%	2 Slices	
[98]	SR-Latch PUF	Spartan-3	49.2%	54.27%	80%	2 Slices	_
[99]	Scan chains PUF	Virtex-5	49.86%	Pass NIST	96%, 98% ^b	128 Slices	_
[100]	p-SPUF	Alinx	50.58%	49.6%	93.3% ^{ab}	12×32 slices	_
[102]	Transformer PUF	Artix-7	49.44%	_	98.12%	Efficient	_
[104]	Modified Anderson PUF	Spartan-6	50.89%	49.41%	91.25% ^a	348 Slices	_
[88]	PC-PUF	Kintex-7	50%	Pass NIST	$\approx 99\%$	365 Slices	_
[39]	FDRO-PUF	Simulation	49.98%	50.05%	99.5% ^{ab}	_	$264 \mu W$
[89]	GARO-PUF	Pynq Z2	39.1%	$\approx 50\%$	98.9%	7 LUT ^s	<u> </u>
[41]	SRAM PUF	FPGA	49.97%	—	88% ^a	4600 SRAM memory bits	_
[42]	LH-PUF	Spartan-3E, Spartan-6	38.28%	—	_	123 slices	$2500 \mu W$
[43]	Hybrid PUF	Simulation	50.9% ^p , 52% ^q	—	99.21%	—	285.5µW ⁹ , 320µW ^q
[45]	Optical PUF	Optical token	49.79%	—	25.25%	1cm×1cm×2.5mm ^d	_
[47]	Optical PUF	Optical token	50%	_	94%	$1 \text{cm} \times 1 \text{cm} \times 2.5 \text{ mm}^{d}$	_
[74]	Latch PUF	CMOS 0.130µm	50.55%	_	96.96% ^b 96.22% ^b	8×16 NOR-latch array	$0.162 \mu W$
[51]	Memristor PUF	Fabricated	High	$\approx 50\%$	_	150(1MB) ^e	_
[53]	Memristor PUF	Simulation	High	$\approx 50\%$	_		_
[54]	Memristor PUF	Simulation	≈50%	$\approx 50\%$	90%ª	Four ^f	$104 \mu W$
[55][56]	Memristor PUF	Simulation	50.1%	48.9%	97%, 95.5%	Two 32×2^{h}	· ·
[62]	Ouantum PUF	Cloud-based ⁱ	55%		96%	_	_
[63]	MRAM PUF	Fabricated	47%	_	99.9%	10×20 PUF array ^j	_
[65]	MRAMPUF	Fabricated[107]	49.8%		92.3%b	32×32 PUE array	
[66]	MRAMPUE	CMOS	~50%	Pass NIST ^k	99.76% ^{ab}	28nm	
[67]	MRAM PUE	CMOS	50.64%	50.02%	07.87% ab	$m \times n$ PUE array ¹	
[69]	Carbon PUE	Simulation	40.67%	50.0270	06 50% ab	$m \wedge m$ i Or allay	1.26.JW
[00]	Carbon PUE	Simulation	~49.07%	~50%	90.5% 06 67% a 80 / 10/b	$1.27 \mu m^{2n}$	1.20µ W
[09]	Carbon PUE	Entricated	~49%	~50%	90.07%, 80.41%	1.27μ III 500 µm DUE array	1550µ w
[70]	Carbon PUF	Simulation	49.1%	45.5%			7 26. W
[72]	Glitch PUF	Sporton 3A	41.5%	+0.770	03.4%		7.20µ w
[72]	Butterfly DUF	Virtex 5	~50%		93.4%	130 slices	
[75]	Digital DUE	Simulation	~50%	50%	~100%ab	$145.92 \times 80.32 \ \mu m^0$	
[79]	SCA DUE	CMOS	~50%	57 901-	00 007/ab	130nm	68rW
[70]	SOT DUE	Eshricated	~50%	J2.0%	99.9%	1.501111	0011W
[/9]	301 FUF	Fabricated	41.2%	40.0%	stable	$0 \times 0 \mu m$ (device size)	—

Table 3: Summery of PUF quality metrics and evaluation.

^a Temperature variation.
 ^b Voltage variation.
 ^c 16 × 64 array = 1024 ROs; One RO (contain 5 inverters and 1 AND gate).

^d Plastic token size.

e Memristor memory structure.

^f Different crossbar sizes (XORed Xbar) 4×2 , 8×2 , 16×2 , 32×2 .

g Spartan-6.

^h Memristive Xbar PUFs.

ⁱ IBM quantum hardware.

¹ IBM quantum hardware.
 ⁵ The array fabricated using standard electron beam lithography process.
 ^k National Institute of Standards and Technology, test results for 10K responses produced from PUF.
 ¹ MRAM Size (m×n cells), 4×128, 8×128, 16×128, 32×128.
 ^m Serial connection of Carbon Nanotube PUF Parallel-elements.
 ⁿ The layout sketched by CAD tool Electric.
 ^o Overall silicon area (chip dimension).
 ^p Power Optimized Hybrid Oscillator-arbiter design.
 ^g Snead Optimized Hybrid Oscillator-arbiter design.

⁴ Speed Optimized Hybrid Oscillator-arbiter desgin.
 ^r Logic Array Block.
 ⁸ Lookup Table.

Ref	PUF Architectures	ML models	Prediction Rate (%)	Training Time	CRPs	Bit Length
[112]	Arbiter PUF	LR ^a	95	0.01s	640	64
	Arbiter PUF	LR	79.05	0.0024s		
[116]		ES ^f	74.8	76.19s	400	64
[110]		Naive Bayes	84.30	0.0011s	400	
		AdaBoost	83.10	0.1167s		
[112]	RO PUF[16]	QS ^c	99		83,941	1024
[109]	XOR Arbiter PUF	NN ^d	50.40 ^e	—	24,000	64
[117]	FF XOR PUF	NN ^d	50		100,000	32
		LR	49.9			
[93]	SRPUF	ES ^f	50.20	—	500,000	64
		DL^g	50.28	54 min 30 s		
[102]	Transformer PUF	LR	60		2000	128
[102]		ES	60		2000	120
[66]	MRAM PUF	LR	65.12			
		SVM	64.53	—	10,000	15
		NN	62.7			
[118]	Multiplexer PUF ^h	NN	1.26		8.55×10^{5}	32
[56]	Memristor PUF	LR	50.5 ⁱ		5000	Xbar size 32×2
[30]		SVM	56.5 ⁱ			

Table 4: Summery of machine learning attack models for different PUF architectures

^a Logistic Regression.

^b Support Vector Machines.

^c Quick Sort.

^d Neural Network.

^e 8 XOR PUF.

^f Evolution Strategies.

^g Deep Learning methods.

^h 7 stages.

ⁱ With XORing.

The attacker then develops a machine learning models to predict the CRPs. Numerous research papers used these attacks against several designs, so designers can evaluate the security strength, weakness and how effectively the attacker can predict the CRPs.

The PUF circuit can be designed to maintain a limited number of challenges in a very short period for each authentication process. However, the challenge-response pair must never be reused to prevent any machine learning attack [21]. In fact, producing large number of pairs is usually required to prevent such prediction. In this case, the PUF circuit will be large and that will increase computational overhead. To address this issue, the authors in [119] proposed a reconfigurable design that increases the number of pairs without affecting the computational resources of the IoT.

The aforementioned attack scenarios need to be considered to develop a secure PUF circuit that can resist the machine learning attack and detect any possible invasive attack. Strong PUFs can be used with the secure authentication protocol to satisfy this security requirements. The authors in [120] introduced obfuscated challenge response protocol to prevent machine learning attack without conventional cryptography, which consists of PUF chip, random number generator and control block. Furthermore, the authors in [109] proposed a training model with Mutli-layer Perceptrons (MLP) as neural network to predict CRPs for XOR Arbiter PUF. The study shows that the accuracy of the prediction depends on the size of the XOR gates (i.e., when the XOR size increase the prediction accuracy percentage decreased). However, the authors believe that prediction rate below 80% can be considered secure as the authentication process relied on multiple response bits (approximately 64 bits). Similarly, the authors in [117] demonstrated a neural network attack against feed-forward XOR PUF with 50% prediction rate for multiple PUF stages. This shows that the proposed feed-forward XOR PUF is considered more secure compared to XOR PUF. Moreover, the authors in [93] introduced various attack models in their design of configurable LFSR PUF. They performed Logistic Regression (LR), Evolution Strategies (ES) and Neural Network. As a result, the prediction rate is approximately 50% of the proposed models. In [102], the authors implemented two models attack, LR and ES for 128 stages Transformer PUF with 8 XOR gates. The evaluation achieved 60% accuracy compared to classical RO PUF with 90% prediction rate. In addition, the authors in [121] developed two mathematical attack on previous PUF design, lightweight secure PUF [122] and composite PUF [123], which consists of multiple different PUF design stages that usually combine strong and weak PUFs. On the other hand, the authors in [66] applied SVM, LR and MPL modeling attack on their proposed Spin-transfer torque (STT)-MRAM reconfigurable Arbiter PUF. It was shown that the design reduces the prediction rate to 65.12% without utilizing XOR gates and 44.34% with XOR gates. Furthermore, the authors in [116] studied the various modeling attack such as, LR, ES, Naive Bayes and AdaBoost on Arbiter PUF with different cases in terms of number of training sets, efficiency of the machine learning algorithms and several number of Arbiter stages. The experiment show that LR and ES performed better for large data sets, while Naive Bayes and AdaBoost applied for small data sets. Additionally, the training time of Naive Bayes faster (0.0007s) compered to other models with the highest prediction rate as shown in table 4. Moreover, the multiplexers have been widely used in delay based PUFs for switching between paths. However, the authors in [118] evaluated multiple stages of multiplexer PUF based on Neural Network method to predict the generated responses and showed that the multiplexer PUF is vulnerable to the machine learning attack with high prediction rate. Consequently, the LR and SVM modelling attacks have been analyzed against memristive Xbar PUF in [56] under linear and nonlinear (e.g. XOR) architectures. The evaluation of LR based attack show that the XORing nonlinearity drop the prediction rate accuracy from 73% to 50.5%, which is near ideal, while exhibiting high resilience against such attack. Table 4 summarizes the common machine learning attack models and related PUFs with the accuracy of predicting CRPs table.

7.6 Side-Channel attack

The side-channel attack is one of the common and powerful technique used to breach a PUF circuit. This attack relied on the leakage information that can be occupied by the power dissipation during the key generation process. For instance, the adversary can exploit the relation between power dissipation and CRPs on the PUF and measure the correlation between two variables, such as, responses R and correlation coefficient r with the corresponding power dissipation P. Several works evaluated the side-channel attack in their proposed design. The authors in [66] evaluated the (STT)-MRAM reconfigurable Arbiter PUF by measuring the correlation between power consumption and 800 generated responses. It was shown that there are no correlation associated between the two variables and the design resist side-channel attacks. Furthermore, the authors in [124] proposed Cross-PUF attacks, which exploit the leakage power of the Latch in Arbiter PUF to train machine learning models, such as SVM, to predict responses. Therefore, the adversary targets one PUF as a references without recording CRPs to breach all PUFs that fabricated from the same Graphic Design System (GDS), which contains a database of circuit layout.

8 Conclusion and Outlook

In recent years, advances in PUF architectures provided a solution for solving and enhancing the security of IoT devices. In this paper, we provided an overview of PUF architectures to provide applicable security solutions for IoT environments due to the low computational complexity of PUF circuit design, less energy and improve the quality metrics such as, randomness, uniqueness and reliability. In addition, the PUF based authentication protocols has been discussed and common security concerns and effective attacks against PUF were reviewed.

More work is still needed to test different properties of PUF to evaluate their security strengths and weakness. The aforementioned techniques provide lightweight authentication for IoT without utilizing the traditional cryptography methods that can increase the power and the resources consumption, still without having to store secret keys in memory.

More investigations is need to design proper PUF architecture that prevent machine learning attack, which traditional cryptography methods such as Hash function are used to prevent in non PUF solutions. However, confidentiality and integrity based PUF for exchanging information between IoT devices is still not addressed by the PUF community, which makes it largely an open problem.

In practice, conventional confidentiality and integrity techniques have been utilized by the PUF authentication protocols, trading off circuit and computational complexity. Therefore, more research is needed to provide suitable and practical encryption and integrity mechanism that can be implemented in the lightweight applications with low energy consumption and more secure.

Acknowledgments

This work is partially funded by the G5797 "Developing Physical-Layer Security Schemes for Internet of Things Networks" project under the NATO's Science for Peace Programme.

References

- D. Wang, B. Bai, W. Zhao, and Z. Han. A survey of optimization approaches for wireless physical layer security. *IEEE Communications Surveys Tutorials*, 21(2):1878–1911, 2019.
- [2] J. Zhang, S. Rajendran, Z. Sun, R. Woods, and L. Hanzo. Physical layer security for the internet of things: Authentication and key generation. *IEEE Wireless Communications*, 26(5):92–98, 2019.
- [3] Mahdi Shakiba-Herfeh, Arsenia Chorti, and H. Vince Poor. Physical layer security: Authentication, integrity and confidentiality, 2020.
- [4] P.W. Shor. Algorithms for quantum computation: discrete logarithms and factoring. In *Proceedings 35th Annual Symposium on Foundations of Computer Science*, pages 124–134, 1994.
- [5] N. Xie, Z. Li, and H. Tan. A survey of physical-layer authentication in wireless communications. IEEE Communications Surveys Tutorials, 23(1):282–310, 2021.
- [6] Dimitrios Schinianakis. Lightweight security for the internet of things: A soft introduction to physical unclonable functions. *IEEE Potentials*, 38(2):21–28, 2019.
- [7] Armin Babaei and Gregor Schiele. Physical unclonable functions in the internet of things: State of the art and open challenges. *Sensors*, 19(14):3208, Jul 2019.
- [8] Ji-Liang Zhang, Gang Qu, Yong-Qiang Lv, and Qiang Zhou. A survey on silicon pufs and recent advances in ring oscillator pufs. *Journal of Computer Science and Technology*, 29(4):664–678, 2014.
- [9] Chip-Hong Chang, Yue Zheng, and Le Zhang. A retrospective and a look forward: Fifteen years of physical unclonable function advancement. *IEEE Circuits and Systems Magazine*, 17(3):32–62, 2017.
- [10] Basel Halak, Mark Zwolinski, and M. Syafiq Mispan. Overview of puf-based hardware security solutions for the internet of things. In 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), pages 1–4, 2016.
- [11] Charles Herder, Meng-Day Yu, Farinaz Koushanfar, and Srinivas Devadas. Physical unclonable functions and applications: A tutorial. *Proceedings of the IEEE*, 102(8):1126–1141, 2014.
- [12] Alireza Shamsoshoara, Ashwija Korenda, Fatemeh Afghah, and Sherali Zeadally. A survey on physical unclonable function (puf)-based security solutions for internet of things. *Computer Networks*, 183:107593, 2020.
- [13] Mohammed Saeed Alkatheiri, Yu Zhuang, Mikhail Korobkov, and Abdur Rashid Sangi. An experimental study of the state-of-the-art pufs implemented on fpgas. In 2017 IEEE Conference on Dependable and Secure Computing, pages 174–180, 2017.
- [14] Ilia A. Bautista Adames, Jayita Das, and Sanjukta Bhanja. Survey of emerging technology based physical unclonable functions. In 2016 International Great Lakes Symposium on VLSI (GLSVLSI), pages 317–322, 2016.
- [15] Chip-Hong Chang and Miodrag Potkonjak. Secure System Design and Trustable Computing. Springer International Publishing, 2016.
- [16] G. Edward Suh and Srinivas Devadas. Physical unclonable functions for device authentication and secret key generation. In 2007 44th ACM/IEEE Design Automation Conference, pages 9–14, 2007.
- [17] Mohammad Tehranipoor and Farinaz Koushanfar. A survey of hardware trojan taxonomy and detection. IEEE Design Test of Computers, 27(1):10–25, 2010.
- [18] armatix. Armatix ip1 limited edition set. http://www.armatix.us/iP1-Limited-Edition.804.0.html? &L=7, 2021. [Online; accessed 2021].
- [19] Jeremy Hsu. New u.s. military chip self destructs on command. https://spectrum.ieee.org/tech-talk/ computing/hardware/us-militarys-chip-self-destructs-on-command, 2015. [Online; accessed 2021].
- [20] Roel Maes and Ingrid Verbauwhede. Physically unclonable functions: A study on the state of the art and future research directions. *Information Security and Cryptography Towards Hardware-Intrinsic Security*, page 3–37, 2010.
- [21] Ulrich R Uhrmair, Frank Sehnke, Jan S Olter, Gideon Dror, Srinivas Devadas, and J Urgen Schmidhuber. Modeling attacks on physical unclonable functions. *Proceedings of the 17th ACM conference on Computer and communications security - CCS 10*, 2010.
- [22] B. Gassend, D. Clarke, M. van Dijk, and S. Devadas. Controlled physical random functions. In 18th Annual Computer Security Applications Conference, 2002. Proceedings., pages 149–160, 2002.

- [23] Abhranil Maiti, Vikash Gunreddy, and Patrick Schaumont. A systematic method to evaluate and compare the performance of physical unclonable functions. *IACR Cryptology ePrint Archive*, 2011:657, 01 2011.
- [24] Hyunho Kang, Yohei Hori, and Akashi Satoh. Performance evaluation of the first commercial puf-embedded rfid. In *The 1st IEEE Global Conference on Consumer Electronics 2012*, pages 5–8, 2012.
- [25] Zouha Cherif Jouini, Jean-Luc Danger, and Lilian Bossuet. Performance evaluation of physically unclonable function by delay statistics. In 2011 IEEE 9th International New Circuits and systems conference, pages 482–485, 2011.
- [26] Mahabub Hasan Mahalat, Shreya Saha, Anindan Mondal, and Bibhash Sen. A puf based light weight protocol for secure wifi authentication of iot devices. In 2018 8th International Symposium on Embedded Computing and System Design (ISED), pages 183–187, 2018.
- [27] Omar Nakhila and Cliff Zou. User-side wi-fi evil twin attack detection using random wireless channel monitoring. In *MILCOM 2016 - 2016 IEEE Military Communications Conference*, pages 1243–1248, 2016.
- [28] Krishna Prasad Satamraju and B. Malarkodi. A puf-based mutual authentication protocol for internet of things. In 2020 5th International Conference on Computing, Communication and Security (ICCCS), pages 1–6, 2020.
- [29] Muhammad Naveed Aman, Mohammed Haroon Basheer, and Biplab Sikdar. Data provenance for iot with light weight authentication and privacy preservation. *IEEE Internet of Things Journal*, 6(6):10441–10457, 2019.
- [30] Konstantinos Goutsos and Alex Bystrov. Lightweight puf-based continuous authentication protocol. In 2019 International Conference on Computing, Electronics Communications Engineering (iCCECE), pages 229–234, 2019.
- [31] Hassan N. Noura, Reem Melki, and Ali Chehab. Secure and lightweight mutual multi-factor authentication for iot communication systems. In 2019 IEEE 90th Vehicular Technology Conference (VTC2019-Fall), pages 1–7, 2019.
- [32] Qi Jiang, Xin Zhang, Ning Zhang, Youliang Tian, Xindi Ma, and Jianfeng Ma. Two-factor authentication protocol using physical unclonable function for iov. In 2019 IEEE/CIC International Conference on Communications in China (ICCC), pages 195–200, 2019.
- [33] Blaise Gassend, Dwaine Clarke, Marten van Dijk, and Srinivas Devadas. Silicon physical random functions. In Proceedings of the 9th ACM Conference on Computer and Communications Security, CCS '02, page 148–160, New York, NY, USA, 2002. Association for Computing Machinery.
- [34] Elena Dubrova. A reconfigurable arbiter puf with 4 x 4 switch blocks. In 2018 IEEE 48th International Symposium on Multiple-Valued Logic (ISMVL), pages 31–37, 2018.
- [35] Yuan Cao, Wenhan Zheng, Xiaojin Zhao, and Chip-Hong Chang. An energy-efficient current-starved inverter based strong physical unclonable function with enhanced temperature stability. *IEEE Access*, 7:105287–105297, 2019.
- [36] Mona Moradi, Reza Faghih Mirzaee, and Sha Tao. Cmos arbiter physical unclonable function with selecting modules. In 2020 20th International Symposium on Computer Architecture and Digital Systems (CADS), pages 1–6, 2020.
- [37] Ding Deng, Shen Hou, Zhenyu Wang, and Yang Guo. Configurable ring oscillator puf using hybrid logic gates. *IEEE Access*, 8:161427–161437, 2020.
- [38] Qian Wang and Gang Qu. A silicon puf based entropy pump. *IEEE Transactions on Dependable and Secure Computing*, 16(3):402–414, 2019.
- [39] Amin A. Zayed, Hanady H. Issa, and Khaled A. Shehata. Finfet based low power ring oscillator physical unclonable functions. In 2019 31st International Conference on Microelectronics (ICM), pages 227–230, 2019.
- [40] D.E. Holcomb, W.P. Burleson, and K. Fu. Initial sram state as a fingerprint and source of true random numbers for rfid tags. *Proc. Conf. Radio Frequency Identification Security (RFID '07, 2007.*
- [41] Jorge Guajardo, Sandeep S. Kumar, Geert-Jan Schrijen, and Pim Tuyls. Fpga intrinsic pufs and their use for ip protection. In Pascal Paillier and Ingrid Verbauwhede, editors, *Cryptographic Hardware and Embedded Systems* - CHES 2007, pages 63–80, Berlin, Heidelberg, 2007. Springer Berlin Heidelberg.
- [42] Sriram Sankaran, S. Shivshankar, and K. Nimmy. Lhpuf: Lightweight hybrid puf for enhanced security in internet of things. In 2018 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), pages 275–278, 2018.
- [43] Venkata P. Yanambaka, Saraju P. Mohanty, and Elias Kougianos. Novel finfet based physical unclonable functions for efficient security integration in the iot. In 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), pages 172–177, 2016.

- [44] Pappu Srinivasa Ravikanth and Stephen A. Benton. Physical one-way functions. Science, 297:2026–2030, 2001.
- [45] Ravi Pappu, Ben Recht, Jason Taylor, and Neil A. Gershenfeld. Physical one-way functions. Science, 297:2026 2030, 2002.
- [46] Michael Geis, Karen Gettings, and Michael Vai. Optical physical unclonable function. 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), 2017.
- [47] Ulrich Rührmair, Christian Hilgers, and Sebastian Urban. Optical pufs reloaded. Eprint. Iacr. Org, 2013.
- [48] L. Chua. Memristor-the missing circuit element. IEEE Transactions on Circuit Theory, 18(5):507–519, 1971.
- [49] Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart, and R. Stanley Williams. The missing memristor found. *Nature*, 453(7191):80–83, 2008.
- [50] Mesbah Uddin, Md Sakib Hasan, and Garrett S. Rose. On the theoretical analysis of memristor based true random number generator. In *Proceedings of the 2019 on Great Lakes Symposium on VLSI*, GLSVLSI '19, page 21–26, New York, NY, USA, 2019. Association for Computing Machinery.
- [51] Patrick Koeberl, Unal Kocabaş, and Ahmad-Reza Sadeghi. Memristor pufs: A new generation of memory-based physically unclonable functions. In *2013 Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 428–431, 2013.
- [52] Garrett S. Rose, Nathan McDonald, Lok-Kwong Yan, Bryant Wysocki, and Karen Xu. Foundations of memristor based puf architectures. In 2013 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), pages 52–57, 2013.
- [53] Garrett S. Rose, Nathan McDonald, Lok-Kwong Yan, and Bryant Wysocki. A write-time based memristive puf for hardware security applications. In 2013 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pages 830–833, 2013.
- [54] Mesbah Uddin, MD. Badruddoja Majumder, Karsten Beckmann, Harika Manem, Zahiruddin Alamgir, Nathaniel C. Cady, and Garrett S. Rose. Design considerations for memristive crossbar physical unclonable functions. J. Emerg. Technol. Comput. Syst., 14(1), September 2017.
- [55] Muhammad Ibrar Khan, Shawkat Ali, Aref Al-Tamimi, Arshad Hassan, Ataul Aziz Ikram, and Amine Bermak. A robust architecture of physical unclonable function based on memristor crossbar array. *Microelectronics Journal*, 116:105238, 2021.
- [56] Muhammad Ibrar Khan, Shawkat Ali, Ataul Aziz Ikram, and Amine Bermak. Optimization of memristive crossbar array for physical unclonable function applications. *IEEE Access*, 9:84480–84489, 2021.
- [57] Boris Škorić. Quantum readout of physical unclonable functions. In Daniel J. Bernstein and Tanja Lange, editors, *Progress in Cryptology – AFRICACRYPT 2010*, pages 369–386, Berlin, Heidelberg, 2010. Springer Berlin Heidelberg.
- [58] W. K. Wootters and W. H. Zurek. A single quantum cannot be cloned. *Nature*, 299(5886):802–803, 1982.
- [59] Sebastianus A. Goorden, Marcel Horstmann, Allard P. Mosk, Boris Škorić, and Pepijn W. H. Pinkse. Quantumsecure authentication of a physical unclonable key. *Optica*, 1(6):421–424, Dec 2014.
- [60] J. Roberts, I. E. Bagci, M. A. M. Zawawi, J. Sexton, N. Hulbert, Y. J. Noori, M. P. Young, C. S. Woodhead, M. Missous, M. A. Migliorato, and et al. Using quantum confinement to uniquely identify devices. *Scientific Reports*, 5(1), 2015.
- [61] Myrto Arapinis, Mahshid Delavar, Mina Doosti, and Elham Kashefi. Quantum physical unclonable functions: Possibilities and impossibilities. *Quantum*, 5:475, 2021.
- [62] Koustubh Phalak, Abdullah Ash Saki, Mahabubul Alam, Rasit Onur Topaloglu, and Swaroop Ghosh. Quantum puf for security and trust in quantum computing. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 11(2):333–342, 2021.
- [63] Jayita Das, Kevin Scott, Drew Burgett, Srinath Rajaram, and Sanjukta Bhanja. A novel geometry based mram puf. In *14th IEEE International Conference on Nanotechnology*, pages 859–863, 2014.
- [64] Jayita Das, Kevin Scott, Srinath Rajaram, Drew Burgett, and Sanjukta Bhanja. Mram puf: A novel geometry based magnetic puf with integrated cmos. *IEEE Transactions on Nanotechnology*, 14(3):436–443, 2015.
- [65] Arash Nejat, Frederic Ouattara, Mohammad Mohammadinodoushan, Bertrand Cambou, Ken Mackay, and Lionel Torres. Practical experiments to evaluate quality metrics of mram-based physical unclonable functions. *IEEE Access*, 8:176042–176049, 2020.

- [66] Rashid Ali, You Wang, Haoyuan Ma, Zhengyi Hou, Deming Zhang, Erya Deng, and Weisheng Zhao. A reconfigurable arbiter puf based on stt-mram. In 2021 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1–5, 2021.
- [67] Yupeng Hu, Linjun Wu, Zhuojun Chen, Yun Huang, Xiaolin Xu, Keqin Li, and Jiliang Zhang. Stt-mram-based reliable weak puf. *IEEE Transactions on Computers*, pages 1–1, 2021.
- [68] S. T. Choden Konigsmark, Leslie K. Hwang, Deming Chen, and Martin D. F. Wong. Cnpuf: A carbon nanotubebased physically unclonable function for secure low-energy hardware design. In 2014 19th Asia and South Pacific Design Automation Conference (ASP-DAC), pages 73–78, 2014.
- [69] Mona Moradi, Sha Tao, and Reza Faghih Mirzaee. Physical unclonable functions based on carbon nanotube fets. In 2017 IEEE 47th International Symposium on Multiple-Valued Logic (ISMVL), pages 124–129, 2017.
- [70] Yongwoo Lee, Jinsu Yoon, Hyo-Jin Kim, Geon-Hwi Park, Dae Hwan Kim, Dong Myong Kim, Min-Ho Kang, and Sung-Jin Choi. Carbon nanotube network transistor for a physical unclonable functions-based security device. In 2019 IEEE 19th International Conference on Nanotechnology (IEEE-NANO), pages 227–230, 2019.
- [71] B. Srinivasu and Anupam Chattopadhyay. Cycle puf: A cycle operator based puf in carbon nanotube fet technology. In 2021 IEEE 21st International Conference on Nanotechnology (NANO), pages 13–16, 2021.
- [72] Daisuke Suzuki and Koichi Shimizu. The glitch puf: A new delay-puf architecture exploiting glitch shapes. In Stefan Mangard and François-Xavier Standaert, editors, *Cryptographic Hardware and Embedded Systems, CHES 2010*, pages 366–382, Berlin, Heidelberg, 2010. Springer Berlin Heidelberg.
- [73] Sandeep S. Kumar, Jorge Guajardo, Roel Maes, Geert-Jan Schrijen, and Pim Tuyls. Extended abstract: The butterfly puf protecting ip on every fpga. In 2008 IEEE International Workshop on Hardware-Oriented Security and Trust, pages 67–70, 2008.
- [74] Y. Su, J. Holleman, and B. Otis. A 1.6pj/bit 96% stable chip-id generating circuit using process variations. In 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, pages 406–611, 2007.
- [75] Jin Miao, Meng Li, Subhendu Roy, Yuzhe Ma, and Bei Yu. Sd-puf: Spliced digital physical unclonable function. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(5):927–940, 2018.
- [76] Yuki Tanaka, Song Bian, Masayuki Hiromoto, and Takashi Sato. Coin flipping puf: A novel puf with improved resistance against machine learning attacks. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65(5):602–606, 2018.
- [77] Yansong Gao, Hua Ma, Said F. Al-Sarawi, Derek Abbott, and Damith C. Ranasinghe. Puf-fsm: A controlled strong puf. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(5):1104–1108, 2018.
- [78] Haoyu Zhuang, Xiaodan Xi, Nan Sun, and Michael Orshansky. A strong subthreshold current array puf resilient to machine learning attacks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(1):135–144, 2020.
- [79] Zhen Cao, Shuai Zhang, Jian Zhang, Nuo Xu, Ruofan Li, Zhe Guo, Jijun Yun, Min Song, Qiming Zou, Li Xi, Oukjae Lee, Xiaofei Yang, Xuecheng Zou, Jeongmin Hong, and Long You. Reconfigurable physical unclonable function based on spin-orbit torque induced chiral domain wall motion. *IEEE Electron Device Letters*, 42(4):597–600, 2021.
- [80] Takanori Machida, Dai Yamamoto, Mitsugu Iwamoto, and Kazuo Sakiyama. A new mode of operation for arbiter puf to improve uniqueness on fpga. In 2014 Federated Conference on Computer Science and Information Systems, pages 871–878, 2014.
- [81] R. Sushma and N.S. Murty. Feedback oriented xored flip-flop based arbiter puf. In 2018 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), pages 1444– 1448, 2018.
- [82] Chongyan Gu, Yijun Cui, Neil Hanley, and Máire O'Neill. Novel lightweight ff-apuf design for fpga. 2016 29th IEEE International System-on-Chip Conference (SOCC), pages 75–80, 2016.
- [83] Kolasani Sahithi and N.S. Murty. Delay based physical unclonable function for hardware security and trust. In 2018 International Conference on Advances in Computing, Communications and Informatics (ICACCI), pages 797–803, 2018.
- [84] Chongyan Gu, Weiqiang Liu, Yijun Cui, Neil Hanley, Maire O'Neill, and Fabrizio Lombardi. A flip-flop based arbiter physical unclonable function (apuf) design with high entropy and uniqueness for fpga implementation. *IEEE Transactions on Emerging Topics in Computing*, pages 1–1, 2019.

- [85] Zhangqing He, Wanbo Chen, Lingchao Zhang, Gaojun Chi, Qi Gao, and Lein Harn. A highly reliable arbiter puf with improved uniqueness in fpga implementation using bit-self-test. *IEEE Access*, 8:181751–181762, 2020.
- [86] Lilian Bossuet, Xuan Thuy Ngo, Zouha Cherif, and Viktor Fischer. A puf based on a transient effect ring oscillator and insensitive to locking phenomenon. *IEEE Transactions on Emerging Topics in Computing*, 2(1):30–36, 2014.
- [87] Pierre Bayon, Lilian Bossuet, Alain Aubert, and Viktor Fischer. Electromagnetic analysis on ring oscillator-based true random number generators. In 2013 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1954–1957, 2013.
- [88] Wei Yan, Chenglu Jin, Fatemeh Tehranipoor, and John A. Chandy. Phase calibrated ring oscillator puf design and implementation on fpgas. In 2017 27th International Conference on Field Programmable Logic and Applications (FPL), pages 1–8, 2017.
- [89] Miguel Garcia-Bosque, Guillermo Díez-SEñorans, Carlos Sánchez-Azqueta, and Santiago Celma. Proposal and analysis of a novel class of pufs based on galois ring oscillators. *IEEE Access*, 8:157830–157839, 2020.
- [90] Jin Li, Lei Li, Ji Yang, Yuanhang He, Wanting Zhou, and Shiwei Yuan. An efficient and stable composed entropy extraction method for fpga-based ro puf. *IEICE Electronics Express*, 17(24):20200350–20200350, 2020.
- [91] Abby Aguirre, Michael Hall, Timothy Lim, Jonathan Trinh, Wei Yan, and Fatemeh Tehranipoor. A systematic approach for internal entropy boosting in delay-based ro puf on an fpga. In 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), pages 623–626, 2020.
- [92] Liang Yao, Huaguo Liang, Zhengfeng Huang, Cuiyun Jiang, Maoxiang Yi, and Yingchun Lu. A lightweight configurable xor ro-puf design based on xilinx fpga. 2021 IEEE 4th International Conference on Electronics Technology (ICET), pages 83–88, 2021.
- [93] Shen Hou, Ding Deng, Zhenyu Wang, Jiahe Shi, Shaoqing Li, and Yang Guo. A dynamically configurable lfsr-based puf design against machine learning attacks. *CCF Transactions on High Performance Computing*, 3(1):31–56, 2020.
- [94] Shen Hou, Yang Guo, and Shaoqing Li. A lightweight lfsr-based strong physical unclonable function design on fpga (january 2019). *IEEE Access*, PP:1–1, 05 2019.
- [95] Jason H. Anderson. A puf design for secure fpga-based embedded systems. In 2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC), pages 1–6, 2010.
- [96] Fathi Amsaad, Ahmed Sherif, Amer Dawoud, Mohammed Niamat, and Selck Kose. A novel fpga-based lfsr puf design for iot and smart applications. In NAECON 2018 - IEEE National Aerospace and Electronics Conference, pages 99–104, 2018.
- [97] Ting Zhou, Yuxin Ji, Mingyi Chen, and Yongfu Li. Pl-mro puf: High speed pseudo-lfsr puf based on multiple ring oscillators. In 2020 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1–5, 2020.
- [98] Amir Ardakani and Shahriar Baradaran Shokouhi. A secure and area-efficient fpga-based sr-latch puf. In 2016 8th International Symposium on Telecommunications (IST), pages 94–99, 2016.
- [99] Wenxuan Wang, Aijiao Cui, Gang Qu, and Huawei Li. A low-overhead puf based on parallel scan design. In 2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), pages 715–720, 2018.
- [100] Shen Hou, Yang Guo, Shaoqing Li, Ding Deng, and Yan Lei. A lightweight and secure-enhanced strong puf design on fpga. *IEICE Electronics Express*, 16(24):20190695–20190695, 2019.
- [101] Yijun Cui, Chenghua Wang, Yunpeng Chen, Ziwei Wei, Mengxian Chen, and Weiqiang Liu. Dynamic reconfigurable pufs based on fpga. In 2019 IEEE International Workshop on Signal Processing Systems (SiPS), pages 79–84, 2019.
- [102] Ziwei Wei, Yijun Cui, Yunpeng Chen, Chenghua Wang, Chongyan Gu, and Weiqiang Liu. Transformer puf: A highly flexible configurable ro puf based on fpga. In 2020 IEEE Workshop on Signal Processing Systems (SiPS), pages 1–6, 2020.
- [103] Manasa kalya and Sathish Kumar. Low complexity ldpc error correction code for modified anderson puf to improve its uniformity. In 2020 International Conference on Smart Electronics and Communication (ICOSEC), pages 997–1002, 2020.
- [104] Armin Lotfy, Masoud Kaveh, Diego Martín, and Mohammad Reza Mosavi. An efficient design of anderson puf by utilization of the xilinx primitives in the slicem. *IEEE Access*, 9:23025–23034, 2021.
- [105] J.W. Lee, Daihyun Lim, B. Gassend, G.E. Suh, M. van Dijk, and S. Devadas. A technique to build a secret key in integrated circuits for identification and authentication applications. In 2004 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.04CH37525), pages 176–179, 2004.

- [106] Daihyun Lim, J.W. Lee, B. Gassend, G.E. Suh, M. van Dijk, and S. Devadas. Extracting secret keys from integrated circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 13(10):1200–1205, 2005.
- [107] Crocus technology. https://crocus-technology.com/, Accessed 2021.
- [108] Yu Zhuang, Khalid T. Mursi, and Li Gaoxiang. A challenge obfuscating interface for arbiter puf variants against machine learning attacks, 2021.
- [109] Khalid T. Mursi, Yu Zhuang, Mohammed Saeed Alkatheiri, and Ahmad O. Aseeri. Extensive examination of xor arbiter pufs as security primitives for resource-constrained iot devices. In 2019 17th International Conference on Privacy, Security and Trust (PST), pages 1–9, 2019.
- [110] Blaise Gassend, Daihyun Lim, Dwaine Clarke, Marten Van Dijk, and Srinivas Devadas. Identification and authentication of integrated circuits. *Concurrency and Computation: Practice and Experience*, 16(11):1077–1098, 2004.
- [111] Shahin Tajik, Enrico Dietz, Sven Frohmann, Jean-Pierre Seifert, Dmitry Nedospasov, Clemens Helfmeier, Christian Boit, and Helmar Dittrich. Physical characterization of arbiter pufs. *Advanced Information Systems Engineering Lecture Notes in Computer Science*, page 493–509, 2014.
- [112] Ulrich Rührmair, Jan Sölter, Frank Sehnke, Xiaolin Xu, Ahmed Mahmoud, Vera Stoyanova, Gideon Dror, Jürgen Schmidhuber, Wayne Burleson, and Srinivas Devadas. Puf modeling attacks on simulated and silicon data. *IEEE Transactions on Information Forensics and Security*, 8(11):1876–1891, 2013.
- [113] B. M. S. Bahar Talukder, Farah Ferdaus, and Md Tauhidur Rahman. Memory-based pufs are vulnerable as well: A non-invasive attack against sram pufs. *IEEE Transactions on Information Forensics and Security*, 16:4035–4049, 2021.
- [114] Shahin Tajik. On the physical security of physically unclonable functions. *T-Labs Series in Telecommunication Services*, 2019.
- [115] Dominik Merli, Johann Heyszl, Benedikt Heinz, Dieter Schuster, Frederic Stumpf, and Georg Sigl. Localized electromagnetic analysis of ro pufs. 2013 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2013.
- [116] Yue Fang, Chenghua Wang, Qingqing Ma, Chongyan Gu, Maire O'Neill, and Weiqiang Liu. Attacking arbiter pufs using various modeling attack algorithms: A comparative study. In 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pages 394–397, 2018.
- [117] S. V. Sandeep Avvaru, Ziqing Zeng, and Keshab K. Parhi. Homogeneous and heterogeneous feed-forward xor physical unclonable functions. *IEEE Transactions on Information Forensics and Security*, 15:2485–2498, 2020.
- [118] Meznah A. Alamro and Khalid T. Mursi. Machine learning attack on a multiplexer puf variant using silicon data: a case study on rmpufs. In 2021 IEEE 6th International Conference on Computer and Communication Systems (ICCCS), pages 1017–1022, 2021.
- [119] Armin Babaei and Gregor Schiele. Spatial reconfigurable physical unclonable functions for the internet of things. Security, Privacy, and Anonymity in Computation, Communication, and Storage Lecture Notes in Computer Science, page 312–321, 2017.
- [120] Yansong Gao, Gefei Li, Hua Ma, Said F. Al-Sarawi, Omid Kavehei, Derek Abbott, and Damith C. Ranasinghe. Obfuscated challenge-response: A secure lightweight authentication mechanism for puf-based pervasive devices. 2016 IEEE International Conference on Pervasive Computing and Communication Workshops (PerCom Workshops), 2016.
- [121] Durga Prasad Sahoo, Phuong Ha Nguyen, Debdeep Mukhopadhyay, and Rajat Subhra Chakraborty. A case of lightweight puf constructions: Cryptanalysis and machine learning attacks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 34(8):1334–1343, 2015.
- [122] Mehrdad Majzoobi, Farinaz Koushanfar, and Miodrag Potkonjak. Lightweight secure pufs. In 2008 IEEE/ACM International Conference on Computer-Aided Design, pages 670–673, 2008.
- [123] Durga Prasad Sahoo, Sayandeep Saha, Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, and Hitesh Kapoor. Composite puf: A new design paradigm for physically unclonable functions on fpga. In 2014 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), pages 50–55, 2014.
- [124] Trevor Kroeger, Wei Cheng, Sylvain Guilley, Jean-Luc Danger, and Naghmeh Karimi. Cross-puf attacks on arbiter-pufs through their power side-channel. In 2020 IEEE International Test Conference (ITC), pages 1–5, 2020.