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Smooth plasma etching of GeSn nanowires for gate-all-around field effect transistors

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Abstract

We report on the nanopatterning of horizontal and vertical germanium-tin ($Ge_{1-x}Sn_x$ or GeSn) nanowires by inductively coupled plasma reactive ion etching for gate-all-around field effect transistors. First, a chlorine based chemistry has been investigated and optimal conditions identified for GeSn 6% alloys. Then, plasma etching was optimized to etch high Sn content GeSn alloys (up to 15%) with a high anisotropy, smooth sidewalls and a high selectivity versus a hydrogen silsesquioxane hard mask. We have shown that, in order to obtain smooth surfaces after plasma etching, a HCl pre-treatment was mandatory to eliminate the native Sn and Ge oxides. This behavior was even more pronounced for high Sn contents. Finally, we succeeded in patterning 20 nm wide suspended beams from GeSn layers with Sn concentrations up to 15% Sn.

Keywords: germanium-tin nanowire, GAA-FET, plasma etching, XPS

Q4 (Some figures may appear in color only in the online journal)

1. Introduction

Germanium tin alloys ($Ge_{1-x}Sn_x$) are promising candidates for next-generation complementary metal oxide semiconductor (CMOS) circuits, low power consumption devices and Si-photonics [1]. The energy bandgap of the GeSn alloys can indeed be controlled by changing the Sn content [2, 3]. For Sn contents 8% and above, unstrained GeSn exhibits a low and direct band gap, with an increase of carrier mobility and electron injection velocity compared to pure Ge [4]. For those reasons, GeSn alloys are currently being investigated as channel materials in next generation devices. Indeed, combining direct band-to-band tunneling and low bandgap should yield efficient tunnel field effect transistors [5]. Moreover, as a group IV alloy, GeSn is an ideal semiconductor for the co-integration of high speed CMOS transistors and Si photonic devices in the short-wave infrared range [6–8]. Gate-all-around field effect transistors (GAA-FETs) are considered as being the 'ultimate' devices to continue the downscaling of transistors. Such an architecture yields the best electrostatic control over the channel by the gate, limiting short-channel effects and significantly reducing the off-state leakage current (I_{OFF}). Vertical nanowires [9] and stacked nano-sheets [10], which have low footprints, are attractive candidates to integrate GAA-FETs in electronic circuits. GeSn nanowires patterning by inductively coupled plasma reactive ion etching (ICP-RIE) will then be key. Indeed, it will define the channel, one of the most crucial parts of such transistors.

Because of the low Sn solubility in Ge (less than 1% at thermal equilibrium), it is difficult to grow (and process) high Sn content GeSn layers. The Sn concentration should be high enough to have the desirable electrical properties, but not too high, to minimize process complexity. The thermal processing window is indeed substantially reduced as the Sn concentration increases (Sn surface segregation/precipitation) [11]. The

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fabrication of gate stacks [12] or ohmic contacts [13, 14] on GeSn was investigated. However, data are scarce concerning the plasma etching of GeSn. As the current study will show, different etching behaviors happen when the Sn content changes. Gupta *et al* [15] found Sn–F bonds on the GeSn surface after CF_4 plasma exposition. This study suggested that a SnF_x passivation layer was formed, preventing CF_4 plasma etching. After exposure to ambient air, there was SnO_yF_x on a GeSn surface exposed to a CF_4 plasma which can be removed thanks to a dip in diluted HCl. Shang *et al* [16] used this behavior for their digital dry-wet etching of GeSn. By alternating CF_4 plasma etchings and dips in HCl, they were indeed able to etch 1.5–3.2 nm of GeSn per cycle. This type of process is very effective to precisely define a pattern (fin or nanowire). It is however unsuitable for the anisotropic etching of patterns from as-grown GeSn films. Although a Cl_2 chemistry was mentioned [17], plasma etching processes were not reported in recent studies on nanoscale patterned GeSn transistors [5, 17]. Milord *et al* [9] used a fast etching process (340 nm min^{-1}) to fabricate micrometer scale disks. They were able to vertically etch hundreds of nm thick GeSn layers thanks to the addition of O_2 in a Cl_2/N_2 mixture. O_2 may have allowed the formation of weakly volatile species, which passivated the sidewalls, while ions brought enough energy to assist desorption or remove these species horizontally by physical sputtering [18]. However, 10 nm range patterns would require a slower and more precise process.

This article focuses on nanopatterning by ICP-RIE of GeSn alloys with Sn contents in the 6%–15% range. The morphology of nanowires and the chemical composition of the surface have been analyzed by scanning electron microscopy and x-ray photoelectron spectroscopy. We show that, in order to obtain smooth surfaces after plasma etching, HCl pretreatment is mandatory to eliminate the native Sn and Ge oxides.

2. Experimental details

The GeSn samples used in this study were grown in the 300 °C–350 °C range on Ge strain-relaxed buffers, themselves on 200 mm Si (100) substrates, by reduced pressure chemical vapor deposition. The 50 nm thick GeSn 6%, 10% and 15% layers were fully strained, as confirmed by x-ray diffraction [19]. Etching masks were defined by e-beam lithography (JOEL6300FS system) using a 60 nm thick hydrogen silsesquioxane (HSQ) resist. Two types of patterns were studied: dots with a diameter ranging from 10 to 110 nm for vertical GAA-FETs and fins with line widths ranging from 10 to 100 nm and a pitch of 50–100 nm for horizontal suspended GAA-FETs (after further removal of the under layer). The 1 cm^2 samples were bonded on 4 inches silicon wafers using poly methyl methacrylate and loaded in an Oxford Plasma Lab 100 ICP-RIE plasma etching chamber for fins and dots patterning. Samples were characterized by scanning electron microscopy (SEM) in tilted view at 85° from the surface using a ZEISS ULTRA$^+$ microscope in order to evaluate the fins profile and etching rates.

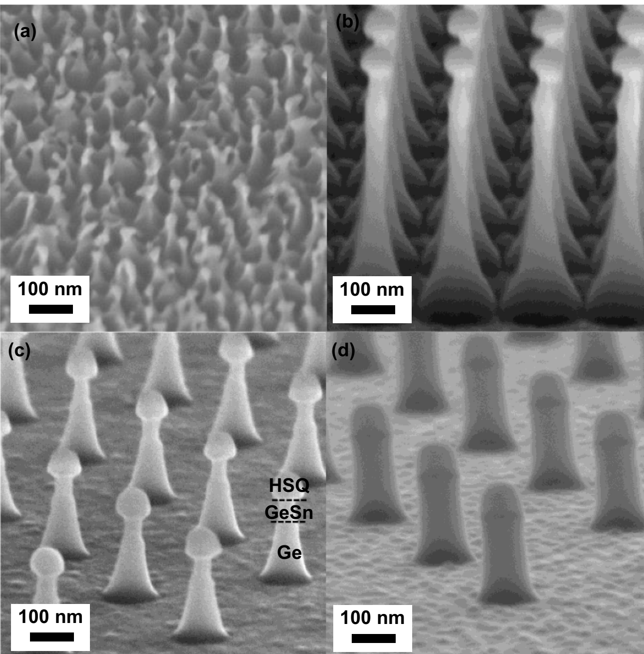

Figure 1. 85° tilted SEM images of $Ge_{0.94}Sn_{0.06}$/Ge after 60 s plasma etching with (a) 25/10/25, (b) 100/10/25, (c) 50/10/25, and (d) 18/5/13 sccm of $Cl_2/O_2/N_2$.

XPS analysis of the GeSn surface was carried out immediately after etching (a few minutes in ambient air only) in a customized thermo electron theta 300 spectrometer, using a high resolution monochromatic Al Kα source at 1486.6 eV. The detection angle was fixed at 21° to the normal of the wafer. XPS spectra were calibrated according to the C1s binding energy of 285 eV. Pass energy for narrow scan windows was set as 23.5 eV with a scan step size of 0.2 eV. The data were fitted using a Shirley function for the background and a pseudo-Voigt function with a Lorentzian contribution of 30% for the peaks. All parameters were left free during fitting, except for the full widths at half maximum that were kept the same for the different contributions of one element.

3. Results and discussion

3.1. Patterning of $Ge_{0.94}Sn_{0.06}$

We studied the etching process of GeSn 6% Sn with a $Cl_2/O_2/N_2$ chemistry. To obtain a precise control and low etching rates, ICP and platen radio-frequency powers were limited to 100 W. Figure 1 shows the influence of the $Cl_2/O_2/N_2$ gas flows. Varying these parameters is a straightforward method to adjust the ratio between etching and passivation. The resulting etching rate and verticality are severely impacted by chemistry changes. The starting $Cl_2/O_2/N_2$ gas mixture was fixed at 25/10/25 sccm. It resulted in the formation of so-called ‘grass’, as shown figure 1(a). This behavior usually occurs when an etch product is re-deposited, or, more probably in our case, when passivation is too strong against etching, generating needles all over the etched surface. Increasing the chlorine flow to 100 sccm results in a faster etching rate of ≈10 nm s^{-1},

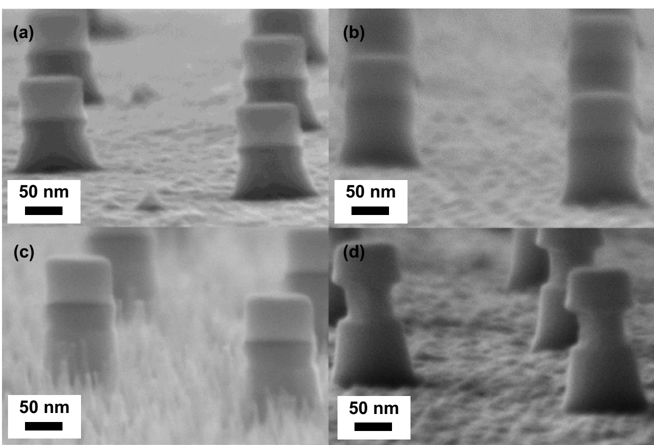

Figure 2. 85° tilted SEM images of etched samples: $Ge_{0.9}Sn_{0.1}$/Ge at (a) 10 mTorr and (b) 5 mTorr; $Ge_{085}Sn_{0.15}$/Ge at (c) 5 mTorr and (d) 5 mTorr without O_2.

which is not desirable for the fabrication of nanoscale GeSn fins and dots (figure 1(b)). Reducing the chlorine flow to a moderate value of 50 sccm reduced the etching rate to 3 nm s^{-1} and yielded smooth sidewalls. There was however an over-etching of GeSn below the HSQ patterns (i.e. an undercut), while dots were conically shaped (figure 1(c)). This was likely due to a poor surface passivation of the GeSn sidewalls.

Figure 1(d) shows the best result obtained with optimized parameters: the ICP power was reduced to 50 W to decrease the plasma density and the platen power was kept to 50 W. The overall gas flow was reduced and the O_2 and N_2 flows increased, proportionally, to improve sidewall passivation: $Cl_2/O_2/N_2$ flows of 18/5/13 sccm were then used, with a 10 mTorr etch pressure. The over-etching of GeSn below the HSQ patterns was then totally suppressed. With such process, sidewalls were vertical and smooth while the etching rate was limited to ≈3.4 nm s^{-1}.

3.2. *Transfer of the process to $Ge_{0.9}Sn_{0.1}$ and $Ge_{0.85}Sn_{0.15}$*

The optimized etching recipes were used on GeSn layers with higher Sn contents (10% and 15%). The etch rate decreased to ≈1.5 nm s^{-1} for 10% of Sn, with a reduced notching in the GeSn layer, as seen in figure 2(a). Decreasing the etch pressure from 10 mTorr down to 5 mTorr (figure 2(b)) restored the verticality of the sidewalls.

For 15% of Sn, the notch was still present even at 5 mTorr in figure 2(c). There was also unwanted needles on the bottom surface. A decrease of the pressure to 3 mTorr, which is the lowest pressure achievable within our equipment with these gases flows and pumping unit, restored the verticality of the sidewalls, but needles remained (not shown here). As needles in an etching process with passivation gas usually originate from too much passivation, we tried to remove oxygen from the recipe. As shown in figure 2(d), needles indeed disappeared, but the verticality of the patterns was lost, with a large etching of the GeSn layer under the HSQ mask.

3.3. *XPS study of the etching process*

To determine the origin of the needles, XPS analyses were carried out.

The top row of figure 3 shows the fitted Ge3d and Sn4d XPS spectra of the $Ge_{0.94}Sn_{0.06}$ surface (figure 3 S6-ref) and the same surface after 15 s (figure 3 S6-15) and 60 s (figure 3 S6-60) of etching. The bottom row shows XPS spectra of the $Ge_{0.85}Sn_{0.15}$ surface (figure 3 S15ref) and the same surface after 15 s (figure 3 S15-15) and 60 s (figure 3 S15-60) of etching. Regardless the sample, XPS spectra show a doublet at 22.4 and 24.4 eV, attributed to the Ge $Ge3d_{5/2}$ and $Ge3d_{3/2}$ and a board peak at 31.88 eV attributed to Ge oxide (Ge–O).

For S6ref and S15ref, the XPS spectra shows the presence of an additional doublet at 24.4 and 23.7 and a broad peak at 25.65 eV attributed to the $Sn4d_{5/2}$ and $Sn4d_{3/2}$ doublet and to Sn oxide (Sn–O), respectively. The intensity of the Sn–O peak is higher in the S15ref case, probably due to the higher Sn concentration. After 15 s of etch, the Sn–O peak is completely removed for S6-15 and S15-15. Moreover, the XPS spectra show an important decrease of the Ge–O peak in the S6ref case. This is not the case for the S15-15, with an almost steady Ge–O peak. This can be explained by a segregation of Sn–O compounds at the surface of GeSn, resulting in some micro-masking and therefore high surface roughness and/or the presence of needles, since the Sn–O etching seems to be faster.

After 60 s of etch, the GeSn layer was completely etched for S6-60 and S15-60 surfaces.

To confirm these hypotheses, the atomic percentages (%) of the different chemical compound detected on the GeSn surface were calculated with the Thermo Avantage® software. Table 1 gives the atomic percentages of Ge and Sn compounds. For a better understanding, three additional parameters were defined:

$$\mathrm{St_{Sn}}\,(\%) = \frac{\mathrm{Sn\%}}{\mathrm{Sn\%} + \mathrm{Ge\%}} \times 100 \quad (1)$$

$$\mathrm{P_{Ge-O\,(\%)}} = \frac{\mathrm{Ge-O\%}}{\mathrm{Ge-Ge\%} + \mathrm{Ge-O\%}} \times 100 \quad (2)$$

$$\mathrm{P_{Sn-O\,(\%)}} = \frac{\mathrm{Sn-O\%}}{\mathrm{Sn-Sn\%} + \mathrm{Sn-O\%}} \times 100 \quad (3)$$

where $St_{Sn}(\%)$ is the Sn percentage in the GeSn alloy, $P_{Ge–O}$ represents the Ge–O (%) in the total Ge compound and $P_{Sn–O}$ represent the Sn–O (%) in the total Sn compound.

Sn concentrations close to the surface were higher than bulk values in $Ge_{0.94}Sn_{0.06}$ (S6ref) and $Ge_{0.85}Sn_{0.15}$ (S15ref) samples. They were indeed equal to 9.5% and 22.5% instead of 6% and 15% for $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.85}Sn_{0.15}$, respectively. There was thus some Sn surface segregation, all the more so for high Sn content layers.

After 15 s of etching, the $P_{Sn–O}(\%)$ was 0 for $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.85}Sn_{0.15}$ surfaces, showing that Sn–O was completely removed. Meanwhile, $P_{Ge–O}(\%)$ decreased, after 15 s of etching, from 31.9% down to 17.3% for $Ge_{0.94}Sn_{0.06}$, at variance

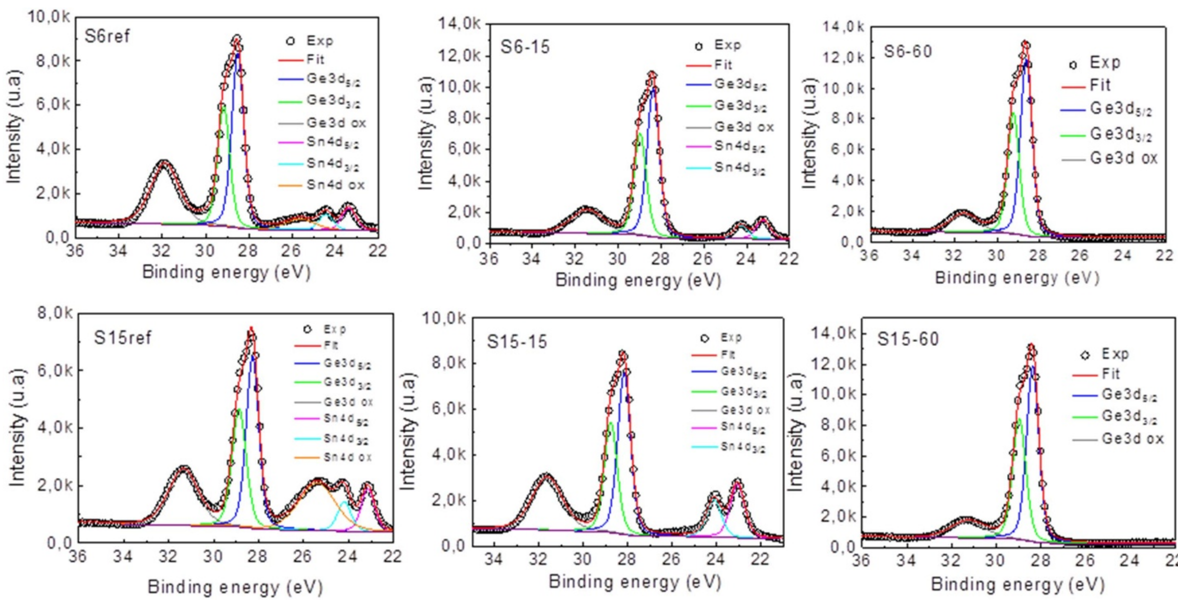

Figure 3. XPS spectra of Ge3d and Sn4d for (top row) the $Ge_{0.94}Sn_{0.06}$ reference sample and the same sample after 15 and 60 s of etching and (bottom row) the $Ge_{0.85}Sn_{0.15}$ reference sample and the same sample after 15 and 60 s of etching.

Table 1. Chemical composition of $Ge_{0.96}Sn_{0.06}$ and $Ge_{0.85}Sn_{0.15}$ surfaces before and after 15 s of etching.

	Ge–Ge (%)	Ge–O (%)	Sn–Sn (%)	Sn–O (%)	$P_{Ge–O}$(%)	$P_{Sn–O}$(%)	St_{Sn}(%)
S6ref	31.8	14.9	3.6	0.8	31.9	17.9	9.5
S6ref@15 s etch	49.7	10.4	4.5	0	17.3	0	6.5
S15ref	29.9	12.9	5.9	3.8	30.1	39	22.5
S15ref@15 s etch	29.9	12.8	8.4	0	29.9	0	19.4

with $Ge_{0.85}Sn_{0.15}$, with a $P_{Ge–O}$(%) staying more or less constant at 30% (table 1). All of this confirms that Sn–O etching was faster and the micro-masking hypothesis. Indeed, the Sn–O percentage was lower in the $Ge_{0.94}Sn_{0.06}$ case, resulting in its complete removal before the 15 s of etching, some removal of Ge–O and a Sn surface concentration closer to its bulk value, then (6.5% instead of 6%). This was not the case for $Ge_{0.85}Sn_{0.15}$, as the starting percentage of Sn–O was much higher. The Ge–O percentage stayed constant, then, while the Sn surface concentration remained definitely higher than in bulk value (19.4% instead of 15%).

XPS has thus shown that oxidized Sn on the GeSn surface was the origin of the micro-masking of GeSn, notably for high Sn contents. For that, samples were thus dipped in a 10% HCl solution prior to plasma etching, in order to remove the Ge and Sn surface oxide. Figure 4 shows a 15% Sn sample etched with the optimized process at 5 mTorr. Thanks to this process, needles have disappeared, sidewalls are perfectly smooth and the GeSn notch was removed.

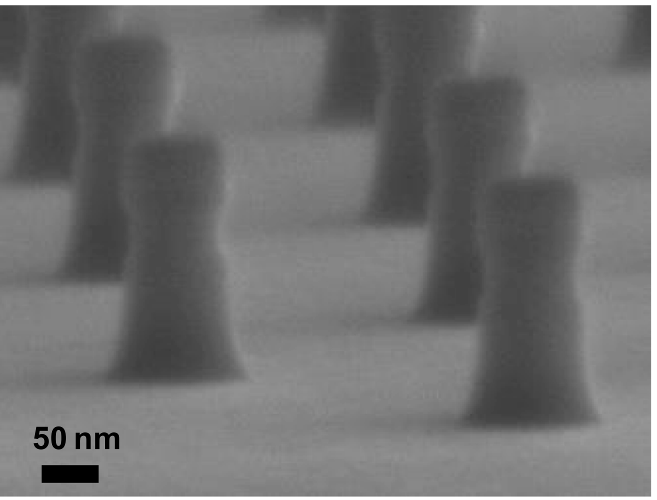

Figure 4. 85° tilted SEM image of a $Ge_{085}Sn_{0.15}$ sample after a dip in HCl prior to ICP-RIE.

3.4. GeSn horizontal nanowire formation for GAA MOSFET

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In this last section, a process sequence for the fabrication of horizontal suspended $Ge_{0.9}Sn_{0.1}$ nanowires for next generation GAA-FETs based on sequential GeSn and Ge plasma etching is presented. The first step consists in the definition of the HSQ hard mask by electron beam lithography. Nanowires with diameters ranging from 5 to 100 nm were targeted. We focus here on single fins 25 nm wide (figure 5(a)) and on networks of 5 fins 20 nm wide (figure 5(b)). GeSn/Ge fins were then

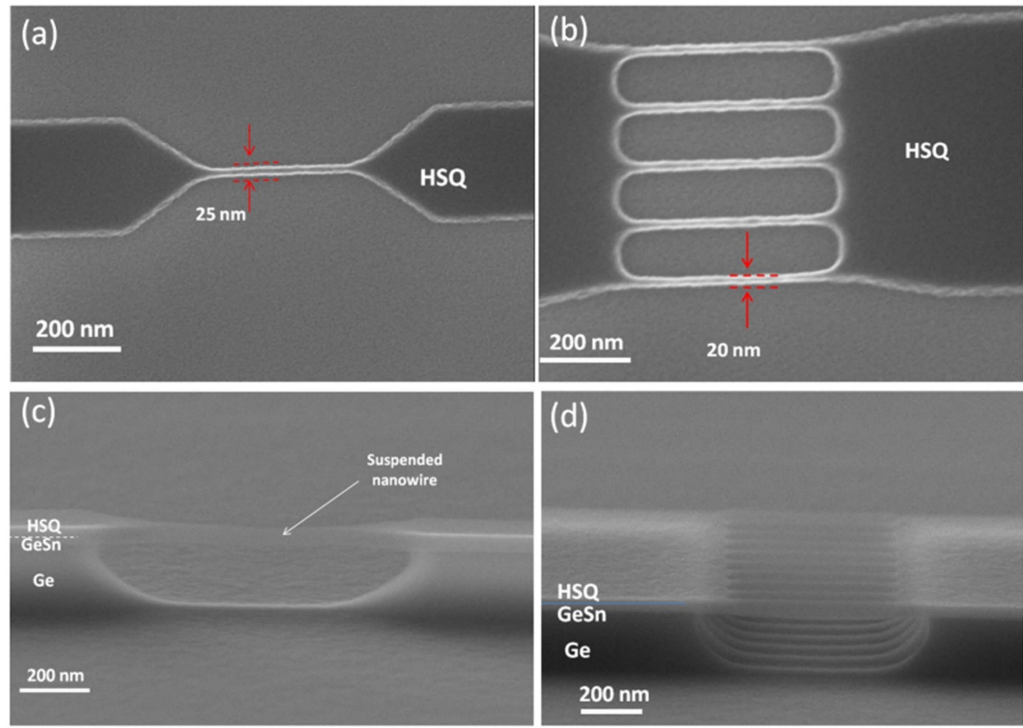

Figure 5. Process technology for the fabrication of suspended GeSn nanowires: (a) and (b) single and network of HSQ hard mask fins obtained by electron beam lithography. (c) and (d) Single and network of suspended GeSn nanowires with HSQ resist still present.

patterned by anisotropic plasma etching using the developed recipe (not shown). After that, Ge was selectively removed thanks to CF_4 isotropic ICP plasma etching, liberating the $Ge_{0.9}Sn_{0.1}$ nanowires. Figures 5(c) and (d) show a single and a network of 10 GeSn suspended nanowires. Thanks to the oxygen passivation during etching with our optimized recipe, the GeSn nanowires were perfectly protected during the Ge underetching step. Finally, the residual HSQ resist was etched in hydrofluoric acid, the sample surface rinsed in deionized water and dried with a N_2 flow. Suspended GeSn nanowires with such small diameters are highly desirable in ultimate GAA-FETs.

4. Conclusion

A process flow for the fabrication of GeSn nanowires for next generation GAA-FETs was evaluated. An anisotropic plasma etching that used a $Cl_2/O_2/N_2$ gas mixture was optimized in an ICP-RIE etching equipment. Gas flow, pressure and ICP power were adjusted to have a smooth and anisotropic etching of a GeSn 6% layer. The optimized etching process was then performed on GeSn layers with higher Sn concentrations. Etching parameters were adapted to avoid the presence of a notch in the GeSn layer (on top of Ge). Thanks to a pressure decrease and a better passivation capability, we were able to anisotropically etch GeSn alloys with up to 15% of Sn, with no notch anymore, smooth sidewalls and a high selectivity with respect to the HSQ hard mask. Finally, a process flow for the fabrication of horizontal suspended nanowires was successfully developed. The later could be used for the realization of next generation GeSn GAA-FETs.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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