International Journal of Control and Automation
Vol. 8, No. 9 (2015), pp. 131-138
http://dx.doi.org/10.14257/ijca.2015.8.9.13

Energy Efficient Design of Hyper Transport Protocol based Laser Driver using Low-Voltage Differential Signaling

BhagwanDas[1], M.F.LAbdullah[1], Mohd ShahNorShahida[1] and QadirBakhsh[1]

[1]*UniversitiTun Hussein Onn Malaysia (UTHM)*
he130092@siswa.uthm.edu.my

Abstract

In this paper, laser driver circuit is designed using current mode logic for safe mode interface of laser with devices attached ahead. Furthermore, energy efficient design is realized on FPGA virtex-6 using Low Voltage Differential Signaling technique. The energy efficient design is tested on Hyper Transport Protocol IO standard on FPGA that includes HTP 1.1, HTP 2.0, HTP 2.5, HTP 3.0 and HTP 3.1 having operating frequencies 1 GHz, 10 GHz, 100 GHz, 1 THz and 10 THz respectively. In LVDS, the four voltage swing values are taken2.5V, 1.2V, 0.9V and 0.3V. Laser driver is operated at mentioned hyper transport protocols for each voltage swing value. It is extracted that when laser driver is operated at all HTPs on voltage swing 0.3V; the maximum power reduction is recorded. For HTP 1.1. 87%, for HTP 2.0. 85%, for HTP 2.5. 85%, for HTP 3.0. 86% and for HTP 3.1. 86% power reduction is recorded at LVDS voltage swing 0.3V in comparison with LVDS voltage swing 2.5V. The main contribution of this work is that energy efficient design of laser driver is proposed that consume less power when signal is transferred at different protocols having high frequenciesusing LVDS technique.This laser driver will be integrated with other optical components in system to provide green optical communication. The design is demonstrated using Xilinx 14.3 software package.

Keywords*: Laser driver; Current Mode Logic; Hyper Transport Protocol (HTP); Low Voltage Differential Signaling (LVDS); Voltage Swing; Field Programming Gate Array*

1. Introduction

In this work, we have designed the energy efficient design of laser driver circuit is implemented for high frequency operation of laser in optical communication system. Laser output is very sensitive to temperature, current and input voltage; small change can produce drastic change in laser output that may destroy the supplementary components attached to it [1, 2].This uncontrolled output must be control to protect the other devices connected to laser using some driver circuits [3]. The main theme of this research work is that, to unify this energy efficient component with other components of optical communication system to develop green optical communication system for future next generation networks.

2. Literature Review

Laser are widely used optical sources in optical communication due to its exceptional size, spectral region of procedure, high efficiency [4]. Many components are interfaced with laser during communication; stable output of laser is always required to protect the additional components attached to laser [5]. Laserdriver works as a switch that reacts over an input signal modulated by the data pulses in either single ended or open-ended configuration for low speed operation and for high-speed operation respectively.There are various techniques are available to control the output of laser driver circuit as such as

ISSN: 2005-4297 IJCA

analog controlling, hybridcontrolling and etc. but all of them having serious concerned over high power consumption. The energy efficient design of laser driver is serious need in real time systems of optical communication systems. Today, FPGA supports high-speed communication; high-speed interface including Hyper Transport and Rapid IO, with design customization [6].

2.1. Low Voltage Differential Signaling (LVDS)

Low voltage differential signaling or TIA/EIA-644, is a standard that stipulates electrical characteristics of a differential, serial communications protocol to address the requirements of high-speed transmission [7]. LVDS delivers high data rates while consuming significantly less power than contending technologies. LVDS has voltage swing property that provides different output at different voltage level [8]. In LVDS, the voltage swing occurs in term of low common-mode voltage. The low common-mode voltage has specified ranges (0.3V, 0.9V, 1.2V and 2.5V). Typical value to be use is 2.5 V common mode voltage considered as with or without LVDS output. The LVDS provides the energy efficient output using higher driver capability and voltage swing(100–350mV) as mentioned in Figure 1 and in Figure 2.

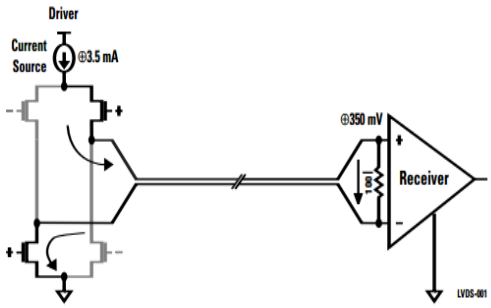


Figure 1. Diagram of LVDS Driver and Receiver Connected via Differential Impedance Media [7]

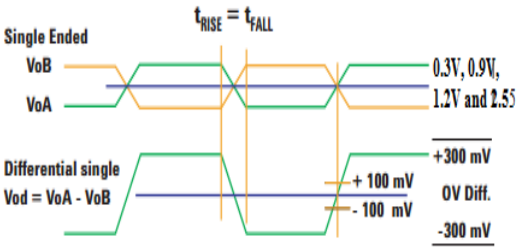
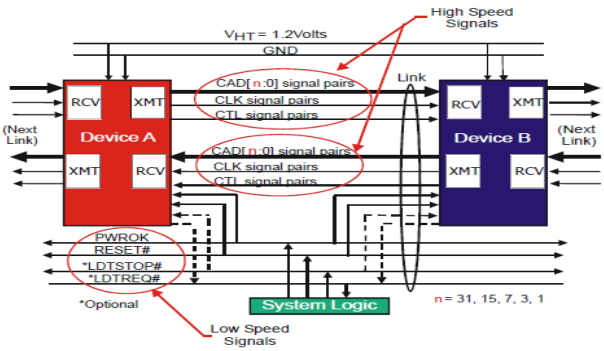


Figure 2. The Lowered Voltage Swing Maintains High Speed and Consume Less Power [8]

2.2. Hyper Transport Protocols (HTP's)

HTP is a technology for interconnection of different processors in bidirectional serial/parallel high-bandwidth configuration. HTP's comes in different frequency and in different signal groups as shown in Figure 3 [9]. Electrically, HTP works on LVDS ranges that provides power management for different voltage configurations. In HTP's the low speed signal requires low signaling such as LVDS and high-speed signals are scalable in terms of clock signals [10]. HTP link on each signal is consist of transmission set and receiving set of signal for each device routed in point to point link [10].



Hyper Transport Protocol	Max. HT frequency	Max. link width	Max. aggregate bandwidth (bi-directional)
1.1	1 GHz	32-bit	12.8 GB/s
2.0	10 GHz	32-bit	22.4 GB/s
2.5	100 GHz	32-bit	33.1 GB/s
3.0	1 THz	32-bit	41.6 GB/s
3.1	10 THz	32-bit	51.2 GB/s

Figure 3. Signal Groups in Hyper Transport Protocol [10]

3. Problem Statement

It is reasonably precarious, when laser devices are directly interfaced with the optical system ahead. It is mandatory to use interface circuit that can protect the ahead system when there is drastic change in laser output. When laser are transmitting more than 10 GHz, the power consumption of the device increased significantly. At 10 THz, the power consumption is increased up to 95%. This increase in power is disaster for laser and system ahead.

4. Methodology

In this work, we have designed the energy efficient laser driver circuit to control the output of laser when operating at different HTP's protocols i.e. at high frequencies. Figure 4 shows the step involves in designing the system. In the first step, the laser driver is designed using current mode logic. In second step, the current mode logic design is tested on high frequency HTP IO standard on field programming gate array (FPGA). When laser drier is operated at, different HTP's having high frequencies the power is increasing drastically. In third step, power consumption is reduced using LVDS for different HTP's. Finally, green optical laser driver circuit is achieved that can be operated at different HTP's having high frequencies at low power consumption.

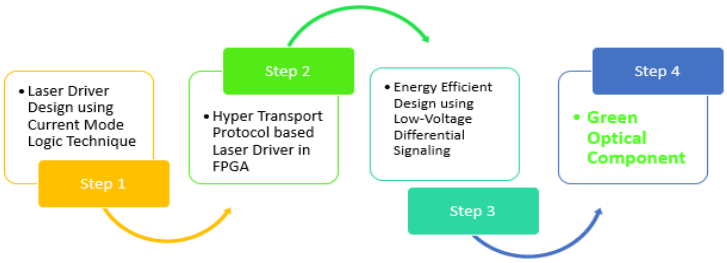


Figure 4. Steps for Designing the Energy Efficient HTP based Laser Driver using LVDS

4.1. Laser Driver Design using Current Mode Logic Technique

Current model logic (CML) is used to interface the fiber optic components [11]. In this work, laser driver is designed using CML because point-to-point transmission at destination on both differential line. Laser driverproduces regulated current by eliminating unwanted common mode noisy signal [12]. Figure 5 shows the design of laser driver that modulate a laser with serial data pulses and provides DC bias (reference) current to the laser. The design consist of N-channel MOSFET (NMOS) parallel logics that works as current switch between laser and optical fiber. The circuit produces IGS and IDD using two

parallel NMOS networks arrangement. IGS is produced with (NMOS1, NMOS3,andNMOS3) and IDDis produced with (NMOS6, NMOS7, NMOS8 and NMOS9). When laser produces the high frequency signal, this signal is controlled by IDD, using external source the current is generated IGS. Then both IDD and IGSare compared, if the laser output is in range the signal is directly transferred to additional circuit, if the laser produces uncontrolled output then, then laser regulates this uncontrolled output and after regulating the current, the output is transferred to circuit ahead.

$$I_{GS} + (I_{GS} + I_{TH}) \le I_{Source,CM} \le \min[\ I_{DD} - Load\ \frac{I_{SS}}{2} + I_{TH}, I_{DD}\ ] \quad (1)$$

Presumptuous that, CML is constrained within the operating range detailed in equation (1) [13], a small difference is produced between IGSandIDD, which is as follows:

$$\Delta I_D = I_{GS} - I_{DD} = \frac{1}{2}\mu_n \Delta I_{SOURCE} \sqrt{\frac{4I_{SOURCE}}{\mu_n}} - \sqrt{\Delta I_{SOURCE}}^2 \quad (2)$$

In Equation (2) [13] ΔID is called the laser driver current, which control the current of laser. Using this driver circuit with laser, safe interfacing between laser and other optical fiber components is possible. There are certain limitations with this design; driver circuit can only operate between 5.5 to 6.6 mA rating.

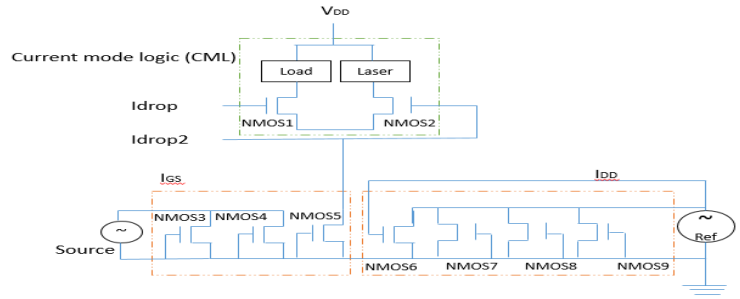


Figure 5. Laser Driver Circuit using Current Mode Logic

4.2. Energy Efficient Design of Laser Driver using LVDS at HTP on FPGA

CML based design of laser driver only regulates the currents and improves the switching performance of the laser. Unfortunately, the power consumption still drastically increases when laser frequency is increased from 10 GHz and above. The power consumption for laser driver design in FPGA is dropped using LVDS technique. The reason for selecting the LVDS among varous IO standard is that HTP is also knows as Lightning Data Transport (LDT) and can only be interface with low-voltage high speed interface and LVDS IO standard has the capability to operate LDT at low voltage with high speed interface. The energy efficient design is then tested on different HTP's to verify the power reduction. We have demonstrated the energy efficient design of CML based laser driver using FPGA. The design is experimentally demonstrated on FPGA virtex-6 board at ambient temperature of 25ºC, using hyper transport IO standard (because of its high-speed operation at low voltage). Figure 6 shows the RTL schematic diagram of laser driver circuit in Xilinx 14.3 suite. Furthermore, the energy efficient design is realized using LVDS technique and tested on different HTP formats. The laser driver is operated at different HTP's having high operating frequency. HTP 1.1 (1 GHz), HTP 2.0 (10 GHz), HTP 2.5 (100 GHz), HTP 3.0 (1 THz) and HTP 3.1 (10 THz). We verified that using LVDS the power consumption is reduced when laser driver is operated at different HTP's. The total power recorded on FPGA is combination of different power as described in (3) [15]. In (3) Device Static Power is leakage power that denotes the transistor leakage

power when the device is powered and not configured. Design Static Power represents the power feeding when the device is constituted but there is no switching activity. It includes static power in I/O DCI terminations, clock, managers, etc. Design Dynamic represents the power consumption from the user logic utilization and switching activity [16].

Total FPGA Power = Device Static + Design Static + Design Dynamic (3)

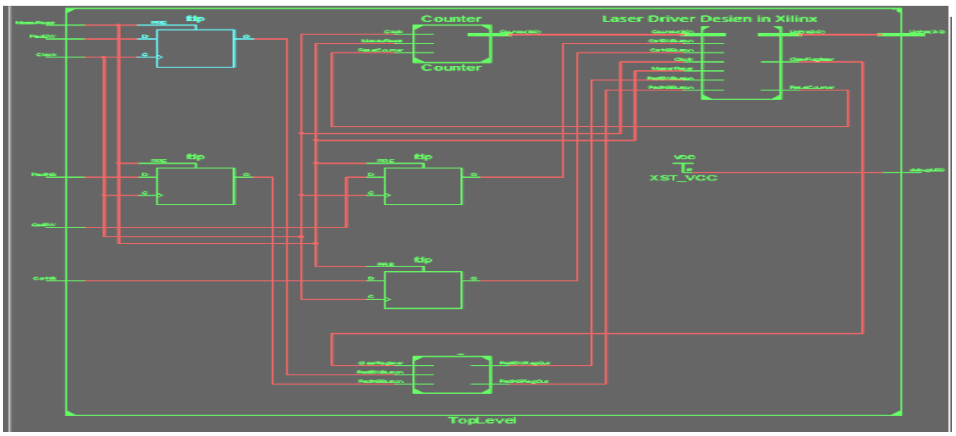


Figure 6. FPGA Based Design of Laser Driver using Xilinx 14.3

4.3 Power Consumption of laser driver at different HTP's standard Using LVDS technique

Power consumption of Xilinx based design of laser driver is observed at different HTP's; HTP 1.0, HTP 2.0, HTP 2.5, HTP 3.0 and HTP 3.1. In the beginning, the power is recorded on LVDS2.5V, which is default value of FPGA virtex-6 board states that LVDS is disabled. Then by changing the voltage swing of LVDS, for all HTP's protocols the power consumption is reduced. It is illustrated that Xilinx based laser driver is operated at different HTP's using LVDS voltage swing at 2.5V (LVDS disabled), 1.2, 0.9 and 0.3 V (LVDS enabled). The power reduction is observed for all HTP's when differential voltage swing of LVDS is reduced from 2.5 V to 0.3 V using LVDS technique.

4.4 Power Consumption of Laser Driver at different HTP's using LVDS at 2.5 V (LVDS disabled)

The power consumption is recorded for different HTP'sHTP 1.1 (1 GHz), HTP 2.0 (10 GHz), HTP 2.5 (100 GHz), HTP 3.0 (1 THz) and HTP 3.1 (10 THz) using voltage swing value of 2.5V(LVDS disabled). Table 1 described the power consumption of laser driver.

Table 1. Power Consumption using LVDSat 2.5 V Voltage Swing (LVDS Disabled) in W

Power → HTP's↓	Device Static	Design Static	Design Dynamic	Total FPGA
HTP 1.1	2.1	1.8	2.3	6.2
HTP 2.0	2.9	2.4	3.1	8.4
HTP 2.5	3.6	3.6	4.2	11.4
HTP 3.0	4.9	4.5	5.3	14.7
HTP 3.1	5.6	5.4	6.1	17.1

4.5 Power Consumption of Laser Driver at different HTP's using LVDS at 1.2V (LVDS enabled)

Tables 2 describes the power consumption of laser driver at HTP 2.0, HTP 2.5, HTP 3.0 and HTP using LVDS at voltage swing of 1.2 V. It is observed that for HTP 1.1. 38%, for HTP 2.0. 37%, HTP 2.5. 27%, for HTP 3.0. 22% and for HTP 3.1 31% power is reduced by enabling the LVDS at voltage swing of 1.2V in comparison with voltage swing 2.5 (LVDS disabled).

Table 2. Power Consumption using LVDS at 1.2 V Voltage Swing (LVDS Enabled) in W

Power → HTP's↓	Device Static	Design Static	Design Dynamic	Total FPGA
HTP 1.1	1.4	1.1	1.3	3.8
HTP 2.0	2.3	1.4	1.6	5.3
HTP 2.5	2.5	2.5	3.3	8.3
HTP 3.0	3.1	3.7	4.2	11
HTP 3.1	3.2	3.8	4.7	11.7

4.6 Power Consumption of Laser Driver at different HTP's using LVDS at 0.9V (LVDS enabled)

Table 3 describes the power consumption for different HTP's at LVDS of 0.9V. It is perceived that for HTP 1.1, HTP 2.0, HTP 2.5, HTP 3.0 and HTP 3.1; the 61%, 58%, 59%, 65% and 66% power is reduced respectively by using LVDS0.9V on contrary the LVDS 2.5.

Table 3. Power Consumption using LVDS at 0.9 V Voltage Swing (LVDS Enabled) in W

Power → HTP's↓	Device Static	Design Static	Design Dynamic	Total FPGA
HTP 1.1	0.9	0.7	0.8	2.4
HTP 2.0	1.6	0.9	1	3.5
HTP 2.5	1.7	1.6	1.3	4.6
HTP 3.0	1.8	1.7	1.6	5.1
HTP 3.1	2	1.9	1.9	5.8

4.7 Power Consumption of Laser Driver at different HTP's using LVDS at 0.3V (LVDS enabled)

When laser driver is operated a LVDS0.3V for different HTP's, the power reduction is recorded; 87% for HTP 1.1, 85% for HTP 2.0, 85% for HTP 2.5, 86% for HTP 3.0 and 86% for HTP 3.1 in comparison with power consumption of HTP's at LVDS2.5V as described in Table 4.

Table 4. Power Consumption using LVDS at 0.3 V Voltage Swing (LVDS Enabled) in W

Power → HTP's↓	Device Static	Design Static	Design Dynamic	Total FPGA
HTP 1.1	0.3	0.3	0.2	0.8
HTP 2.0	0.4	0.5	0.35	1.25
HTP 2.5	0.6	0.7	0.4	1.7
HTP 3.0	0.7	0.8	0.5	2
HTP 3.1	0.8	0.9	0.7	2.4

5. Results and Discussion

Energy efficient laser driver is demonstrated using FPGA virtex-6 at different Hyper Transport Protocols having different frequencies ranges using Low voltage differential signaling. Laser driver is operated at different voltage swings for different HTP's, the power reduction is achieved. At voltage swing value of 1.2 of LVDS for all HTP's, power reduction is realized. For HTP 1.1, HTP 2.0, HTP 2.5 and HTP 3.1, total 38%, 37%, 27%, 22%, and 31% power reduction is recorded in comparison with voltage swing of LVDS2.5V. When laser driver is operated at LVDS 0.9 V, 61% for HTP 1.1, 58% for HTP 2.0, 59% for HTP 2.5, 65% for HTP 3.0 and 66% for HTP 3.1 power reduction is recorded on contrary to LVDS 2.5 V. Finally, when laser driver is operated at LVDS 0.3 V, the 87%, 85%, 85%, 86% and 86% power consumption is reduced for device in compassion with LVDS2.5V. The LVDS consume very low power on different IO standards at high-speed operation because the power consumption is directly proportional to square of the voltage applied to circuit. When laser driver is operated at maximum voltage of FPGA i.e. LVDS2.5V (LVDS disabled), the power consumption is maximum. When laser driver is operated at below 2.5V FPGA core voltage, the power consumption is reduced. This power reduction is function of voltage utilized by FPGA board. Another reason for power reduction using LVDS at different HTP' is actual requirement of laser driver is ranges from 0.1 V to 1.0 V. When the voltage swing falls in this range, ultimately the power consumption is reduced. When the voltage swing cross the laser driver voltage ranges the power consumption is increasing drastically. In this way, the power is saved using LVDS technique, without changing the circuit structure. Figure 7 shows the power reduction curves for laser driver when operating at different HTP's using LVDS. It clearly states that when voltage swing is reduced from 2.5 to 0.3 V using LVDS the power reduction is achieved. It is concluded that for energy efficient output the laser driver must be operated at LVDS0.3V voltage swing for all hyper transport protocols.

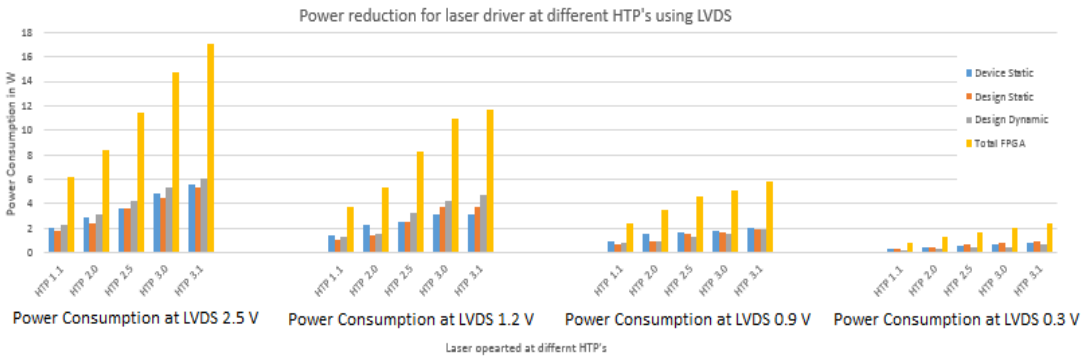


Figure 7. Laser Driver Power Reduction for different HTP's using LVDS Technique

6. Conclusion

We analyzed the significant reduction in power consumption of laser driver, when operating at different Hyper Transport Protocols at different voltage swing values of LVDS. Overall, the for HTP 1.1 87%, for HTP 2.0 85%, for HTP 2.5 85%, for HTP 3.0 86% and for HTP 3.1 86% power reduction is recorded for LVDS 0.3 V in comparison with LVDS 2.5 V. In future, the laser driver circuit can be implemented using ultrascle FPGA or 16 nm FPGA board to reduce more power even at high frequencies.

Acknowledgements

We are thankful to UniversitiTun Hussein Onn Malaysia (UTHM), Malaysia that encourages us to contribute in research. This work is supported by Research Acculturation Collaborative Effort (RACE) Grant [vot1437] & Postgraduates Incentive Grant (GIPS) UTHM.

References

[1] F. Aznar, S. C. Pueyo and B. C. López, "CMOS receiver front-ends for gigabit short-range optical communications", Springer Science & Business Media, **(2012)**.
[2] O. Graydon, "Laser diodes: Linewidth reduction", Nature Photonics, vol.9, **(2015)**, pp.7-7.
[3] S. Zheng, Z. H. Xu, J. J. Liu and Q. Fu, "The Application of Electronic Communication Relay Protection in Distribution Network with Distributed Generation", Advanced Materials Research, **(2015)**, pp.938-942.
[4] J. Turner and M. Jessup, "System and Method for Sensing Signal Disruption", **(2014)**.
[5] Ž. L. Vasić, Y. Gao, S. Pun, P. Mak, M. Vai and I. Krois, "Effect of Transmitter and Receiver Electrodes Configurations on the Capacitive Intrabody Communication Channel from 100 kHz to 100 MHz", The 15th International Conference on Biomedical Engineering, **(2014)**.
[6] J. L. Erb, S. Sundquist, J. E. Shapland, R. G. Walsh and J. Shimada, "Optical Fiber-Fine Wire Conductor and Connectors", **(2014)**.
[7] A. J. Aude, "Low voltage differential signaling (LVDS) circuitry and method for dynamically controlling common mode voltage at input", **(2014)**.
[8] L. S. Siong, A. Saad, L. Lini and K. W. Lee, "On-chip slew-rate control for low-voltage differential signalling (LVDS) driver", Intelligent Signal Processing and Communication Systems (ISPACS), International Symposium, **(2014)**.
[9] P. J. Fox, A. T. Markettos and S. W. Moore, "Reliably prototyping large SoCs using FPGA clusters", Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC), 9th International Symposium, **(2014)**.
[10] D. Anderson and J. Trodden, "Hypertransport system architecture: Addison-Wesley Professional", **(2003)**.
[11] G. S. Jeong, H. Chi, K. Kim and D. K. Jeong, "A 20-Gb/s 1.27 pJ/b low-power optical receiver front-end in 65nmCMOS", Circuits and Systems (ISCAS), IEEE International Symposium, **(2014)**.
[12] X. Wang, "Jitter suppression techniques for laser driver circuits", **(2004)**.
[13] G. N. Link, "High speed semiconductor laser driver circuits", **(1999)**.
[14] J. R. Templin and J. R. Hamlet, "A new power-aware FPGA design metric", Journal of Cryptographic Engineering, vol.5, **(2015)**, pp.1-11.
[15] L. Shang, A. S. Kaviani and K. Bathala, "Dynamic power consumption in Virtex™-II FPGA family", Proceedings of the ACM/SIGDA tenth international symposium on Field-programmable gate arrays, **(2002)**.
[16] L. Benini, A. Bogliolo and G. De Micheli, "A survey of design techniques for system-level dynamic power management", Very Large Scale Integration (VLSI) Systems, IEEE Transactions, vol.8, **(2000)**, pp.299-316.

