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Research Article

Design of Boosted Multilevel DC-DC Converter for Solar Photovoltaic System

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Integration of renewable energy sources to the grid-connected system has influenced scholarly research in recent times to evolve solutions for power electronic conversion. Particularly, solar photovoltaic (SPV), being a resource available throughout the year, demands needful research to meet the demand for industrial applications. To facilitate SPV, multilevel inverters (MLIs) and cascaded H-bridge inverters (CHBIs) are proposed in the literature to meet the power requirement. However, these circuits suffer from efficiency loss, economic aspects of DC sources usage, and switching losses. Hence, in this research, a new power converter topology is projected to improve the overall efficiency of SPV systems. Further, a three-level approach involving (i) SPV Panel-Temperature Reduction (SPV-PTR) Setup, (ii) Boost Multilevel Direct Current Link Converter (BMLDCLC), and (iii) use of effective snubber modules (SM) are effectively handled to promote the industry readiness of the proposed system. From a detailed system investigation, it is seen that the proposed arrangement has minimized the power loss to ensure better quality in output. Furthermore, the software-based results and hardware setup of the planned comprehensive converter have shown promising results in terms of (i) reduced voltage stress, (ii) reduced total harmonic distortion (THD) without filter component, and (iii) reduced power loss. It is observed that the experimental setup has reported a 12.9% of excess heat removal, 5% decrease in harmonics, and 33% switch reduction than the existing MLI schemes. In addition, the proposed setup is suggested to apply for industrial purposes indicate its efficacy to be a solution in real time.

1. Introduction

Alarming environmental concerns and exhaustion of fossil fuels have invoked the necessity of eco-friendly power generation via renewable energy resources [1]. Having the superiority to reduce greenhouse emissions, renewable energy is considered as one of the essential tools to avoid energy import. In particular, SPV systems have gained monumental recognition to emerge as a resource of the decade. Zero maintenance, harmless operation, abundant availability, and easy portability are its inherent merits over other renewable energy resources.

In general, SPV modules are constant voltage sources fed to a load via power conditioning circuits. However, fabricating an efficient and cost-effective converter prototype model is really challenging. Since the power conditioning circuitries are implemented over two or three-level converters, interfacing PV panels for high power application become complex

and uncertain. More importantly, sequential power electronic switching with three-level converters renders excessive voltage stress across the converter. This results in stressed transmission. Therefore, a supplementary snubber circuit at the output is mandated to reduce the transient power loss [2]. In addition, bulky filter components are also used to tap the hassle-free sinusoidal output. However, the system cost is increased beside the additional usage of transformers on the output side [3].

As an alternative to three-level converters, researchers have used multiple topologies with multilevel inverters (MLIs). It is important to note here that the advent of MLIs has enabled the efficient interface with multiple electrical applications such as (i) uninterrupted power supply (UPS) systems, (ii) motor drives, (iii) integration of renewable energy systems, (iv) static compensator, and (v) renewable energy sources [4–8]. Though MLIs have exhibited their significant merits from the end-user side, they are penalized with the necessity of high (i) power-switching components, (ii) regulator units, (iii) power supply units, (iv) gate driver circuits, (v) protection units, and (vi) DC sources to reduce its popularity [9–16]. This certainly increases the manufacturing cost of the system. Out of many configurations in MLI, a few important works in literature are presented as the review in the following. A typical nine-level multilevel inverter for induction motor application is presented in [9]. Also, the importance of high-frequency switches to control uncertainty and voltage diversity factor is critically analyzed in this research. With an objective to reduce power electronic switches, a seven-level MLI with three sources is presented in [10]. Alternatively, a nine-level MLI design with four DC sources is presented in [11]. Notably, usage of limited (twelve) Metal Oxide Semiconductor Field Effective Transistor (MOSFET) switch has gained research interest to reduce THD. However, all the aforementioned works have the drawbacks of (i) design of control circuit, (ii) elimination of lower-order harmonics, and (iii) requirement of high switching devices. Hence, a novel H-bridge-based MLI system has been proposed in [12]. But then, the research necessitates an additional DC source which remains an important downside of the topology. Sequentially to limit the source count with MLI, a seven-level MLI with only three DC sources is proposed in [13]. However, twelve controlled semiconductor switches are used. With a motive to reduce power electronic switches, a similar MLI design with eight controlled semiconductor switches is proposed in [14]. Using only three sources, the same seven-level MLI topologies are presented in [15, 16]. Nevertheless, usage of power semiconductor switches was found high compared to [14].

At the outset, in comparison to various topologies discussed in [13–20], it is seen that the output voltage is achieved either by a series connection of DC sources or using a transformer at the inverter side. Thus, it becomes a nonviable solution for grid-connected systems economically. Note that power losses are also increased due to the usage of the bulky transformer. This invokes a power converter system to maintain the nominal voltage at the DC link, and it is achieved by using appropriate DC to DC power converters. Alternatively, cascaded H-bridge inverters among MLI are also proposed in the literature. Owing to the simpler and lucid circuitry, few research works are reported by using cascaded H-bridge inverters (CHBIs) in [17–20]. In comparison over two or three-level inverters, the use of CHBI offers multiple salient features such as (i) meagre transient across the inverter, (ii) reduced total harmonic distortion (THD) without filter component, and (iii) less significant filter components.

Commencing from the extensive review survey, it is seen that there exist a wide gap in formulating an MLI with the following advantages: (i) limited DC sources, (ii) less stress on the converter, (iii) less THD, and (iv) limited use of power electronic switches. Therefore, a new and novel seven-level stepped DC-link converter is proposed in this research. In addition, the converter is integrated with the PV source to check its viability for industry applications. In order to appreciate the panel temperature within limits, an exclusive prototype testing of PV with an aluminum sheet supported by a DC fan for cooling arrangement is performed. It is important to note here that PV panels are provided with a hydrophobic nano coating (HNC) solution to avoid dust accumulation and stagnant water droplets on PV panels. This helps the PV to shield itself from corrosion, thus increasing the lifetime for its continued quality of operation. The distinguished merits of the proposed research are summarized in the following.

(i) A new seven-level stepped DC-link MLI with reduced stress on the converter is proposed for the first time

(ii) The seven-level stepped DC-link converters are interfaced with the PV module, and their industrial viability is studied

(iii) To subside the panel temperature in real time, the cooling arrangement is provided via aluminum sheet and DC fans

(iv) To enable durability and long sustainability with PV, hydrophobic nano coating (HNC) is used

(v) The use of two PV sources at the input side per phase eliminates the unnecessary stress on the converter

The entire paper is ordered as follows. In Section 2, PV modelling and design of DC-DC boost converter is detailed. In Section 3, the proposed converter design and its design constraints are given. Software-based results and hardware realization are given in Sections 4 and 5, respectively. To contribute to a fair comparative study, the usage of power electronic components and their losses are analyzed and compared in Section 6. Conclusions are addressed as the summary in Section 7.

2. PV Modelling

One-diode PV models are prevalently popular to use for simulation investigations. The representation of the corresponding electrical circuit of one diode PV model is represented in Figure 1 [21–23], and for better understanding,

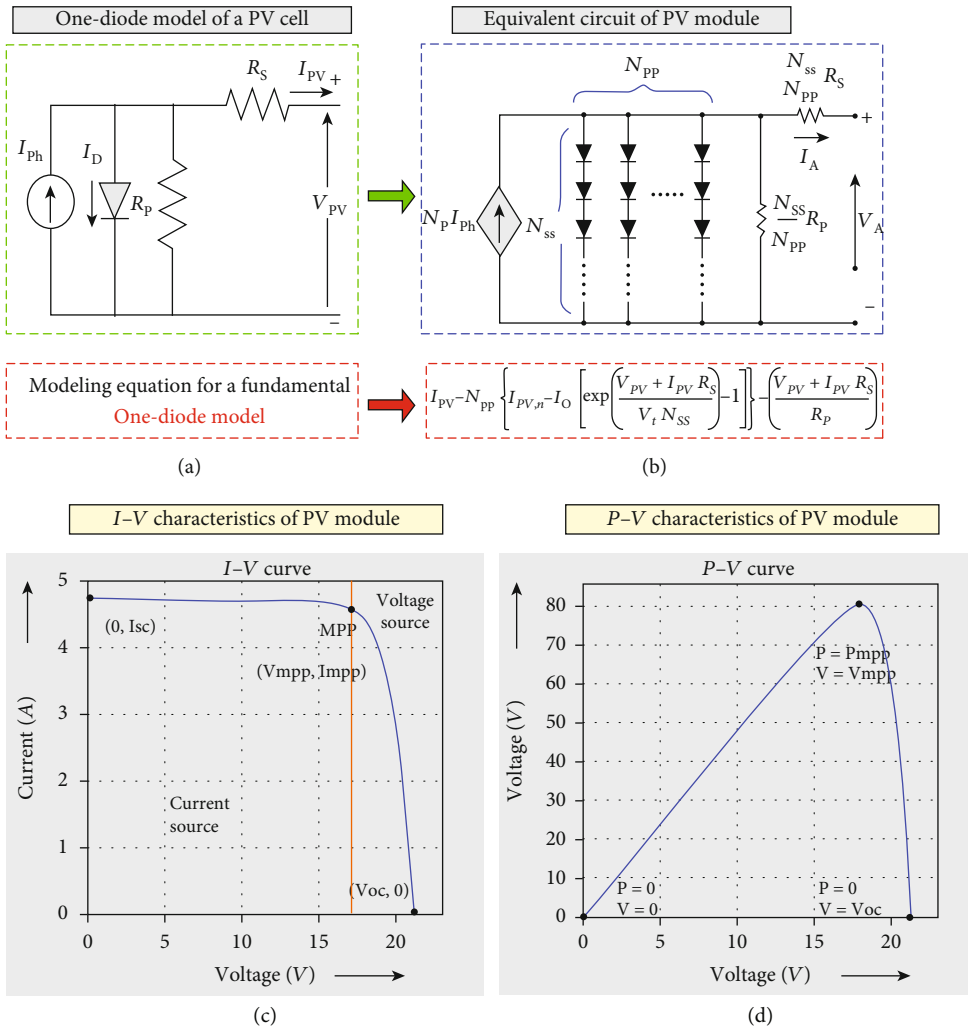


Figure 1: One-diode PV model and its characteristics.

the I-V and P-V distinctiveness of a PV module are also presented in the same figure. From the characteristics, it is seen that PV operates at a unique operating point where maximum power can be extracted. In addition, PV demands a power electronic interface to enable its smoother operation. The PV output current [23] by applying KCL is given by

$$I_{\mathrm{PV}} = I_{Ph} - I_D - \frac{V + I_{\mathrm{PV}} Rs}{Rp}. \tag{1}$$

The ideal diode current equation is mathematically given in Equation (2).

$$I_D = I_O\left(e^{V_D/\alpha V_T} - 1\right), \tag{2}$$

where "I_o" is the reverse saturation current, "a" is the diode ideality factor, and "V_T" is the thermal voltage proportional to temperature changes which is given by

$$V_T = \frac{N_S K T}{q}, \tag{3}$$

where "N_s" is the number of cells connected in series, "K" is the Boltzmann constant, "T" is the temperature at STC, and "Q" is the charge of the electron $1.9 * 10^{-19}$C. On incorporating "I_D" in "I_{PV}," then the output current equation (24) becomes

$$I_{\mathrm{PV}} = N_{pp}\left\{I_{Ph} - I_O\left[\exp\left(\frac{V_{PV}+I_{\mathrm{PV}}R_S}{V_t N_{ss}}\right) - 1\right]\right\} - \left(\frac{V_{\mathrm{PV}} + I_{\mathrm{PV}}R_S}{R_P}\right), \tag{4}$$

where "N_{SS}" and "N_{PP}" are the numbers of cells connected in series and parallel [24, 25].

3. Multilevel Stepped DC-Link Converter

Further, synthesizing sinusoidal voltage with less harmonic using multiple DC sources is its unique characteristic. Note that three-phase multilevel inverters gain more attention since each individual phase requires an "N" number of DC sources to obtain a "$2N+$" voltage output level. However, MLI greatly suffers due to the requirement for an increased

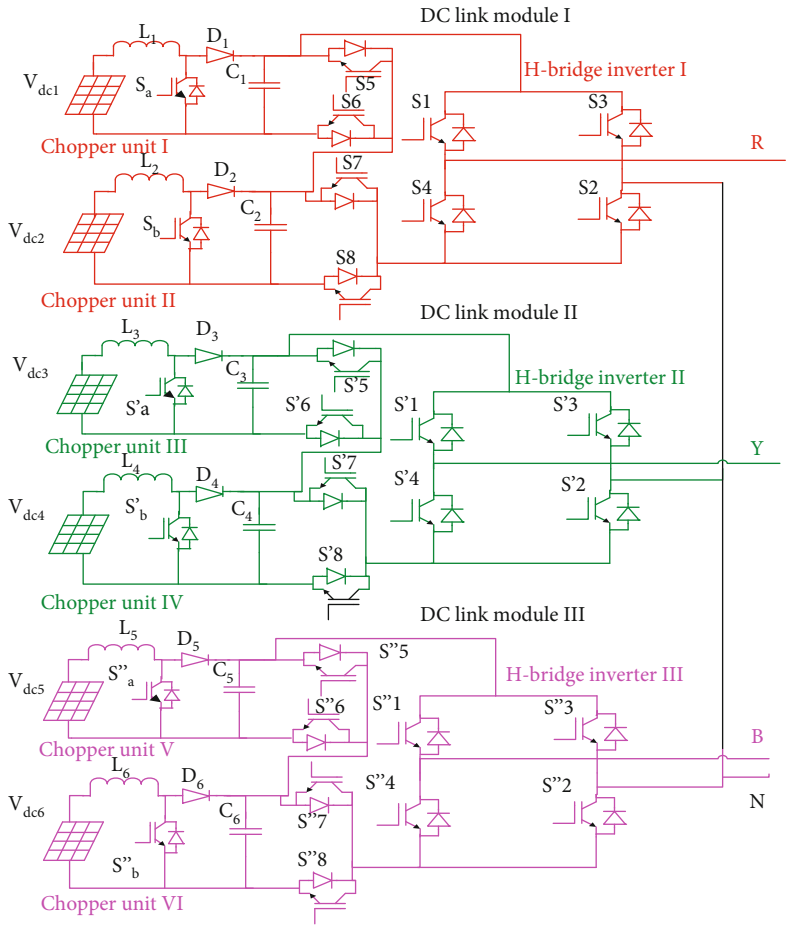


Figure 2: Equivalent circuit of three-phase seven-level BMLDCLC.

number of power electronic components, and this is reduced by using Boosted Multilevel DC Line Converter design. One such configuration with PV as the source is proposed in this research. The operating modes and their analysis on output voltage are discussed in the following.

3.1. Design of Boosted Multilevel DC-Link Converter (BMLDCLC). The schematic of the projected seven-level BMLDCLC circuit is represented in Figure 2. For understanding, each phase is highlighted in different colors and named in the convention as *R* phase, *Y* phase, and *B* phase. Note that each phase is provided with a provision to switch on and off to maintain the output voltage in limits. Further, the boost converter is interfaced among the MLI and PV sources. This eliminates the necessity of a transformer and thus improving the cost efficiency of the converter. Further, the equivalent circuit of BMLDCLC clearly shows that boost chopper takes responsibility to uphold DC-link voltage across each phase. In addition, two power sources are used in each phase reduces the stress on converter is a notable merit of proposed converter. The generalized equations (12–14) to estimate the power components, sources, and level of single-phase BMLDCLC are presented in Equations (5)–(7).

$$N_{\text{switch}} = 2s + 4H + b, \tag{5}$$

$$n = 2(H+1)^s - 1, \tag{6}$$

$$H = n - (n-1), \tag{7}$$

where "*s*" is the DC source count, "*n*" is the number of levels, "*H*" is the number of converter topology at load end, and "*b*" represents boost converter.

3.2. Design of Boosted Multilevel DC-Link Converter (BMLDCLC). The DC-DC boost converter is an integral part of the proposed converter design. Further, it is connected to the inverter via switching circuitry to generate AC waveforms. The schematic of the DC-DC boost converter is presented in Figure 3. Since PV is a constant voltage source, the task of boosting converter becomes much easier to maintain constant DC-link voltage across the inverter. As a known fact that PV is a nonlinear DC source, the system demands a maximum power point controller to track the MPP. To achieve this, each PV panel is provided with a current and voltage sensor to track the unique operating point where the highest accessible power is able to be pulled out. Note that a simple perturb and observe (P&O) algorithm is employed to appreciate simplicity. Besides, the necessity of a metaheuristic algorithm is not required since only one module is used as a DC source [26–30]. For brevity, the flowchart of the P&O algorithm is presented in Figure 4.

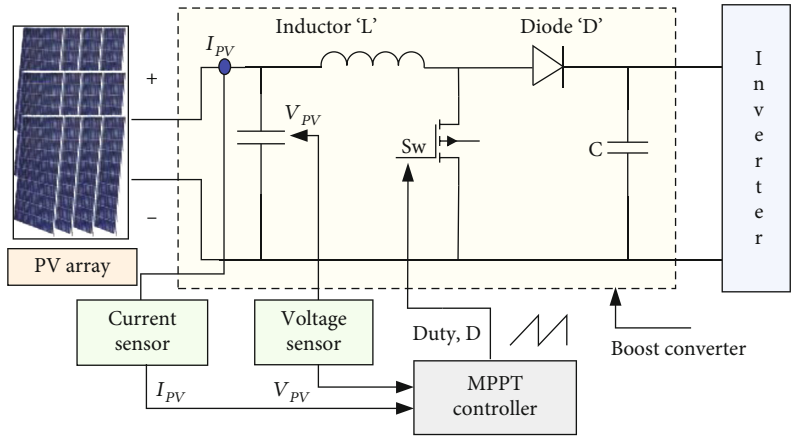


Figure 3: Representation of DC-DC boost converter.

In general, P&O works on the standard that repeated perturbation in voltage is made until the MPP is tracked. Based on the power values, the duty cycle of the boost chopper is altered [11]. Duty cycle equation of the boost chopper is given in the following.

$$D = \frac{V_o - V_s}{V_o}, \tag{8}$$

where "V_o" and "V_s" are the voltage across the load and source voltage, respectively, and "D" is the duty cycle. Further, the design considerations of boost chopper are given in the following. It is always ensured that the boost chopper is worked in continuous conduction mode, and the design of inductor "L" is made by following the equation given in (9).

$$L = \frac{V_o(1-D)}{\Delta i_L f_s}, \tag{9}$$

where "Δi_L" is the inductor current $(i_2 - i_1)$ and "f_s" is the switching frequency. For better output quality, 3% current ripple is considered for designing the inductor. Capacitor design is made by following the equation given in (10).

$$C = \frac{1-D}{8L(\Delta V_o/V_o)f_s^2}, \tag{10}$$

where $f_s = 1/T$ is the switching frequency and "$\Delta V_o/V_o$" is the voltage ripple, and it is approximately considered as 3%.

3.2.1. Modes of Operation of Boosted Multilevel DC-Link Converter (BMLDCLC). The proposed Boosted Multilevel DC-Link Converter (BMLDCLC) is designed for 3-phase load, and each phase constitutes six different operating modes. A detailed discussion on its working is given in the following.

(1) Modes of Operations in "R" Phase. During the first and fourth modes of operation, the source voltage "V_{dc1}"is boosted by turning on the switch S_a. The mathematical expression for "V_{dc1}" is given.

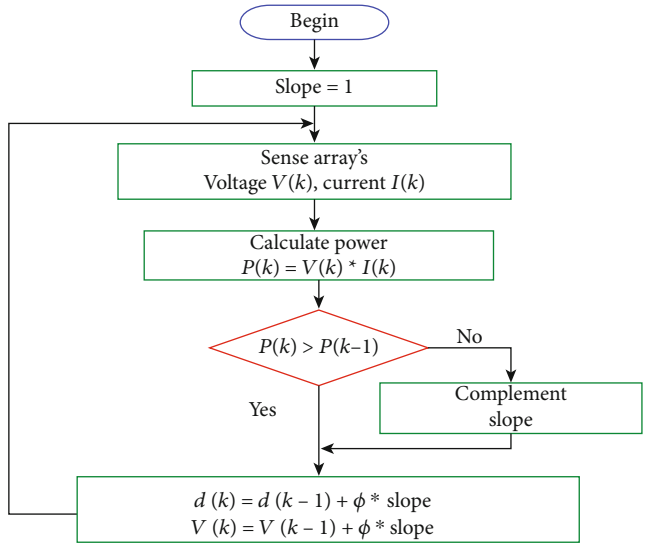


Figure 4: Perturb and observe algorithm for MPP tracking.

In Equations (8) and (9), further, the switches S_6 and S_7 are made to behaviour to attain the voltage level "V_{ob1}" at the inverter side.

$$V_{dc1} = L_1 \frac{I_2 - I_1}{T_{on1}}, \tag{11}$$

$$V_{dc1} = L_1 \frac{dI_1}{dt}. \tag{12}$$

The energy stored in the inductor "E_{i1}" can be calculated by using Equation (6).

$$E_{i1} = V_{dc1}.I_{s1}.T_{on1}. \tag{13}$$

At the time, $t = T_{off1}$, switch S_a is made to switch off, and hence, source current flows through L from I_2

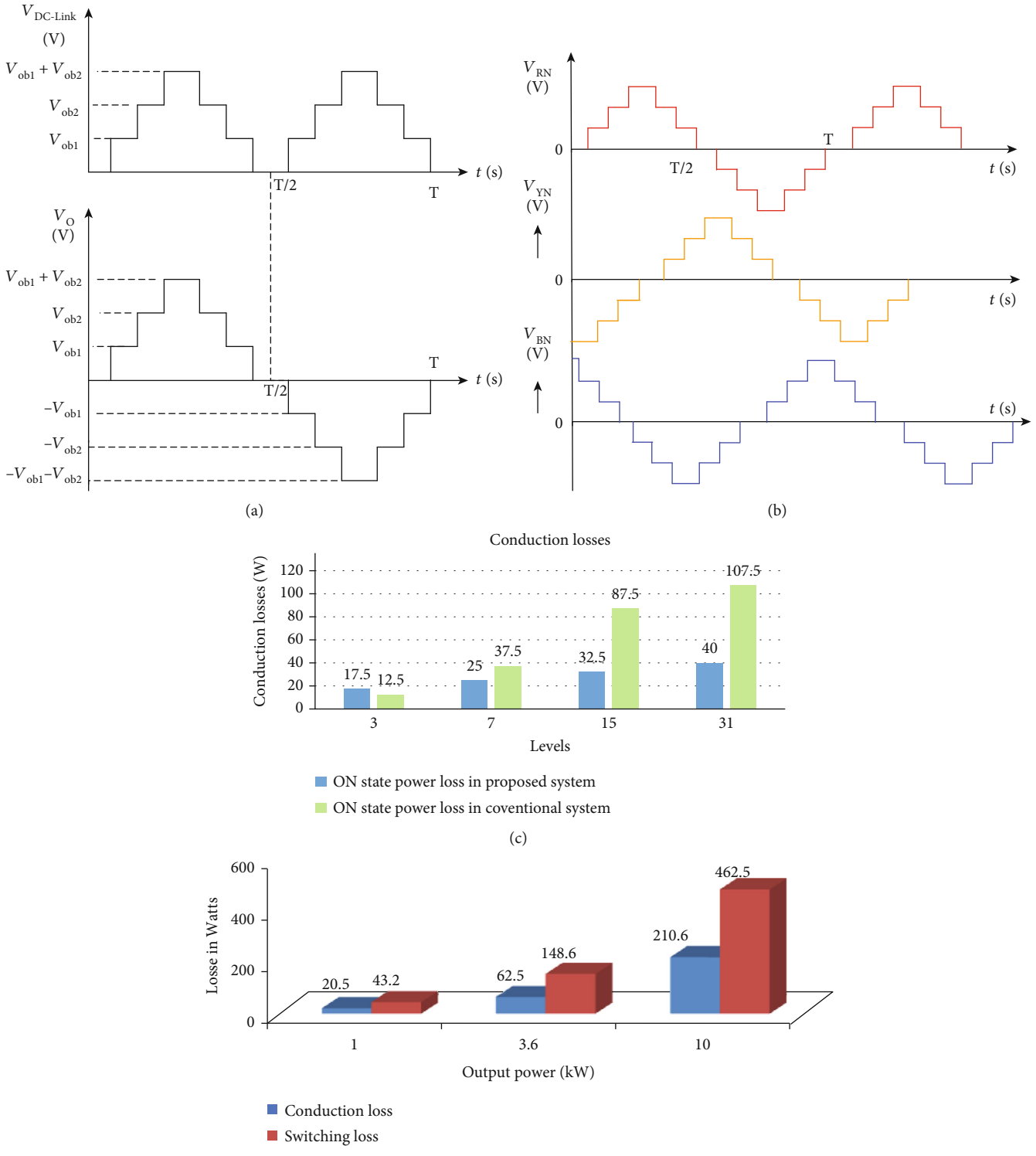
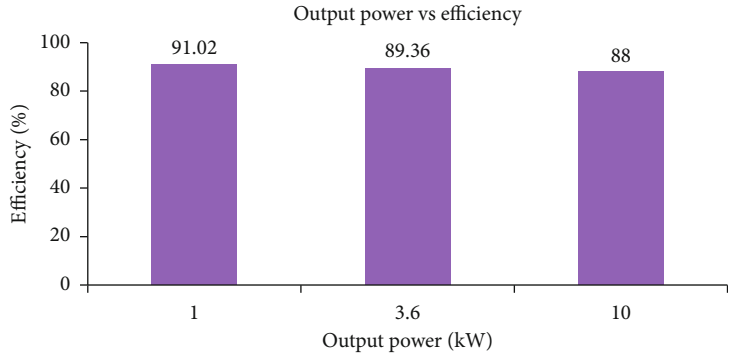


Figure 5: Continued.



(e)

FIGURE 5: (a) Distinctive voltage waveform of 1Φ seven-level BMLDCLC. (b) Characteristic output voltage waveform of 3Φ BMLDCLC. (c) Analysis of conduction loss of BMLDCLC. (e) Losses and efficiency.

to I_1. Therefore, the average output voltage at DC to DC boost converter I can be expressed as Equation (14)

$$V_{ob1} = V_{\mathrm{dc1}} + L_1 \frac{dI_{s1}}{T_{\mathrm{off1}}}. \tag{14}$$

The energy release 'E_{o1}' at this instant can be calculated using Equation (15).

$$E_{o1} = (V_{ob1} - V_{\mathrm{dc1}}) I_{s1}.T_{\mathrm{off1}}. \tag{15}$$

The output voltage of boost converter I of R phase is thus attained as in Equation (16).

$$V_{ob1} = \frac{V_{\mathrm{dc1}}}{1 - K_1}. \tag{16}$$

The change in capacitor voltage can be calculated by using Equation (17).

$$\Delta V_{C1} = I_{o1} * \left[\frac{V_{ob1} - L_1(I_2 - I_1)}{V_{ob1} * f * C_1}\right]. \tag{17}$$

In the second and fifth switching schemes of the chopper unit, the PV source voltage V_{dc2} is boosted to V_{ob2} by turning on the switch S_b in the boost chopper, while S_5 and S_8 are used as a snubber. At this time period, $t = T_{\mathrm{on2}}$; switch S_b of chopper unit-II is turned on to raise the inductor current I_3 and I_4 linearly. The voltage and energy equation corresponding to inductor L_2 is equated in Equations (18) and (19).

$$V_{\mathrm{dc2}} = L_2 \frac{I_4 - I_3}{T_{\mathrm{on2}}}, \tag{18}$$

$$E_{i2} = V_{\mathrm{dc2}}.I_{s2}.T_{\mathrm{on2}}, \tag{19}$$

where I_3 is the current flowing through the inductor during boost operation in boost chopper unit-II and I_2 is the current flowing through the inductor due to S_b in boost chopper unit-II. During $t = T_{\mathrm{off2}}$, switch S_b of the chopper-II unit gets turned off, because of which, the current through L_2 linearly falls from I_4 to I_3. The expression pertaining to the average output voltage and energy stored in the boost chopper IV is given in the following equations:

$$V_{ob2} = V_{\mathrm{dc2}} + L_2 \frac{dI_{s2}}{T_{\mathrm{off2}}}, \tag{20}$$

$$E_{o2} = (V_{ob2} - V_{\mathrm{dc2}}) I_{s2}.T_{\mathrm{off2}}. \tag{21}$$

For schemes 3 and 6, the source voltage V_{dc1} and $V_{\mathrm{dc2}}$are stepped up to obtain V_{ob1} and V_{ob2} by turning on switches S_a and S_b of DC-to-DC boost converter. During conduction, S_6 and S_8 act as a snubber to protect the boost converter switches. During the turn-on period ($t = T_{\mathrm{on3}}$), switches S_a and S_b remain conducting to linearly rise the inductor current L_1 and L_2 from I_1 to I_2 and from I_3 to I_4 respectively. The input energy of inductor L_1 from the source voltage V_{dc1} is given in Equation (22).

$$E_{i3} = (V_{\mathrm{dc1}} + V_{\mathrm{dc2}}).(I_{s1} + I_{s2}).T_{\mathrm{on3}}, \tag{22}$$

The output phase voltage (V_{RN}) of BMLDCLC is given as

$$V_{RN} = (V_{ob1} + V_{ob2}) \sin \omega t. \tag{23}$$

(2) Modes of Operations in Y Phase. Similar to the modes of operation of R phase, Y phase DC-link switches (S_5', S_6', S_7', and S_8'), boost chopper switches (S_a' and S_b'), and converter switches (S_1', S_2', S_3', and S_4') are triggered systematically with the phase shift of 120°. The phase voltage equation pertinent to the "Y" phase is given by (V_{YN}). For Y phase, the scheme of switching the 2nd and 5th DC-DC boost converter is followed. The PV source voltage V_{dc4} is boosted to V_{ob4} by turning on the switch S_b' in the DC-DC boost converter where S_5' and S_8' are used as snubbers. At time period $t = T'_{\mathrm{on2}}$, switch S_b' of DC-DC boost converter is turned on to raise the inductor current I_3' to I_4' linearly. The voltage

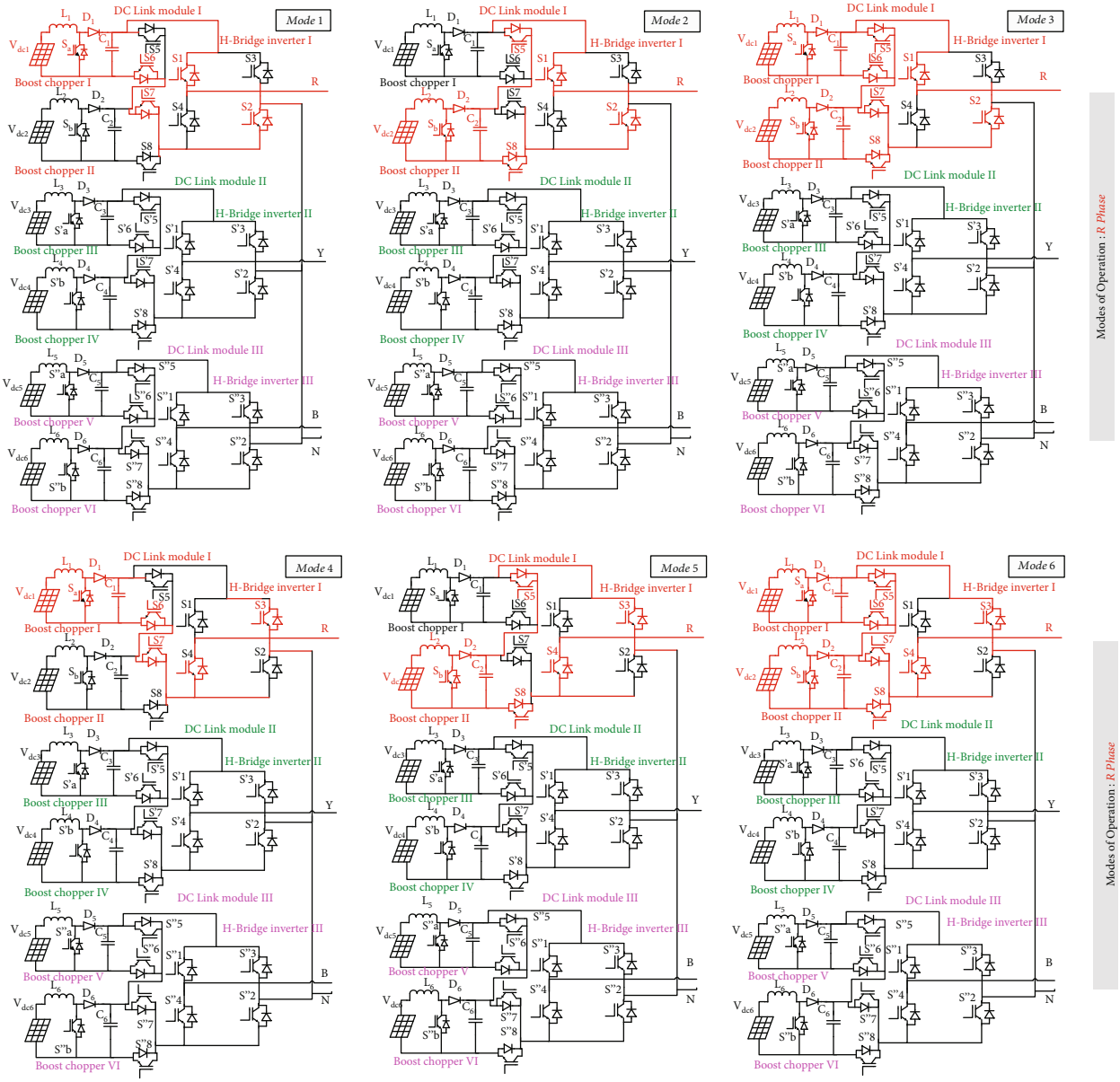


Figure 6: Modes of operation of proposed 3-phase seven-level BMLDCLC.

and energy equation corresponding to inductor L_4 is expressed as

$$V_{\mathrm{dc4}} = L_4 \frac{I'_4 - I'_3}{T'_{\mathrm{on2}}}, \tag{24}$$

$$E_{i4} = V_{\mathrm{dc4}}.I_{s4}.T'_{\mathrm{on2}}. \tag{25}$$

At time $t = T'_{\mathrm{off2}}$, switch S'_b of the DC-DC boost converter is turned OFF where the inductor current linearly falls from I_4 to I_3. The expression pertaining to the average output voltage and energy stored in the DC-DC boost converter IV is given in the following equations:

$$V_{ob4} = V_{\mathrm{dc4}} + L_4 \frac{dI_{s4}}{T'_{\mathrm{off2}}}, \tag{26}$$

Table 1: Specifications of three-phase BMLDLC systems.

Parameters	Range
Source voltage unit I (V_{ob1})	24 V
Source voltage II (V_{ob2})	48 V
H-bridge inverter output voltage (V_{phmax})	72 V
H-bridge inverter output voltage ($V_{L\ \mathrm{max}}$)	120 V
RL load system	218 Ω, 197 mH
Rated power	100 W

$$E_{o4} = (V_{ob4} - V_{\mathrm{dc4}})I_{s4}.T'_{\mathrm{off2}}. \tag{27}$$

The average output voltage of DC-DC boost converter IV

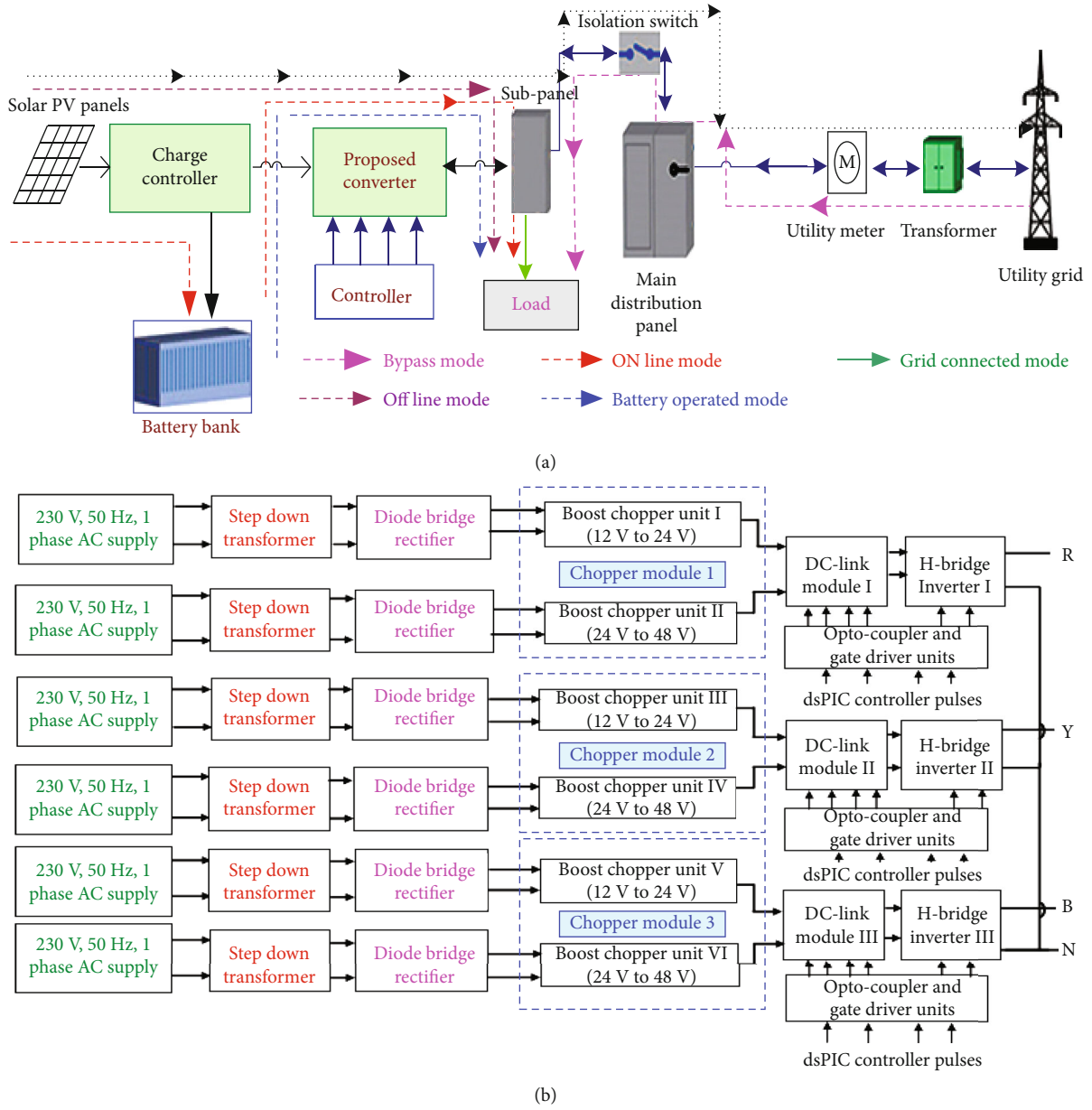


Figure 7: (a) Schematic diagram of BMLDCLC-based UPS system. (b) Block diagram of 3ϕ seven-level BMLDCLC.

under ideal conditions is expressed in Equation (28).

$$V_{ob4} = \frac{V_{dc4}}{1 - K'_2}. \tag{28}$$

The difference in voltage across the capacitor C_4 is articulated by Equation (29).

$$\Delta V_{C4} = I_{o4} * \left[\frac{V_{ob4} - L_4\left(I'_4 - I'_3\right)}{V_{ob4} * f * C_4}\right], \tag{29}$$

where V_{dc4} is the DC source voltage IV, I_{s4} is the DC source current IV, K'_2 is the duty cycle of DC-DC boost converter IV, and V_{ob3} is the output voltage of DC-DC boost converter IV.

$$V_{YN} = (V_{ob3} + V_{ob4}) \sin(\omega t - 120^\circ). \tag{30}$$

(3) Modes of Operations in B Phase. Similar to the modes of operation of R and Y phases, B phase DC-link switches (S''_5, S''_6, S''_7, and S''_8), DC to DC converter II (S''_a and S''_b), and inverter switches (S''_1, S''_2, S''_3, and S''_4) are triggered systematically with the phase shift of 240°. For schemes 3 and 6, the source voltage from PV, V_{dc3}, and V_{dc4} are stepped up to obtain V_{ob3} and V_{ob4} by turning on switches S'_a and S'_b of DC-DC boost converter. During conduction, S'_6 and S'_8 act as a snubber to protect the boost converter switches. During the turn-on period ($t = T'_{on3}$), switches

Table 2: Qualitative study of proposed work with other popular methods in literature.

Parameter	Ref [14]	Ref [15]	Ref [17]	Ref [18]	Ref [19]	Ref [20]	Proposed converter
Number of PV/DC sources required	3	4	3	3	3	3	2
Number of power electronic switches/phase	12	12	12	8	14	18	10
Number of gate drivers	6	6	6	3	6	10	3
TSV	176.3	153.4	No data	No data	No data	162.4	148.6
Voltage level of inverter	7	9	7	7	7	7	7
Series connected DC sources or transformer requirement at inverter	✓	✓	✓	✓	✓	✓	×
Efficiency	85.3	88.4	82.1	No data	No data	86.4	90.9

H: high; L: low; ✓: mandatory; ×: not mandatory.

S_a' and S_b' remain conducting to linearly rise the inductor current L_3 and L_4 from I_1' to I_2' and from I_3' to I_4', respectively. The input energy given to the inductor L_3 from the PV source voltage V_{dc3} is given in Equation (31).

$$E_{i5} = (V_{dc3} + V_{dc4}).(I_{s3} + I_{s4}).T'_{on3}. \quad (31)$$

At time instant $t = T'_{off3}$, the switches S_a' and S_b' are turned off, and the corresponding inductor current L_3 and L_4 current is observed to fall linearly from I_2' to I_1' and I_4' to I_3', respectively. The energy released from the inductors L_3 and L_4 to the snubber module can be estimated as follows:

$$E_{o5} = [(V_{ob3} - V_{dc3})I_{s3} + (V_{ob4} - V_{dc4})I_{s4}].T'_{off3}. \quad (32)$$

The difference in voltage across the capacitors C_3 and C_4 are articulated using Equation (33).

$$\Delta V_{C_3} + \Delta V_{C_4} = I_{o3} * \left[\frac{V_{ob3} - L_3\left(I'_2 - I'_1\right)}{V_{ob3} * f * C_3}\right] + I_{o4} * \left[\frac{V_{ob4} - L_4\left(I'_4 - I'_3\right)}{V_{ob4} * f * C_4}\right]. \quad (33)$$

$$V_{BN} = (V_{ob3} + V_{ob4}) \sin(\omega t + 240). \quad (34)$$

The expected output voltage waveforms for 1Φ and 3Φ inverter systems are represented in Figures 5(a) and 5(b), respectively. The equations for estimating the highest phase and line voltages of 3ϕ BMLDCLC are as follows.

$$V_{RY} = \sqrt{3}(V_{ob1} + V_{ob2} + V_{ob3} + V_{ob4}) \sin\left(\omega t + \frac{\pi}{6}\right), \quad (35)$$

$$V_{YB} = \sqrt{3}(V_{ob3} + V_{ob4} + V_{ob5} + V_{ob6}) \sin\left(\omega t - \frac{\pi}{2}\right), \quad (36)$$

$$V_{BR} = \sqrt{3}(V_{ob5} + V_{ob6} + V_{ob1} + V_{ob2}) \sin\left(\omega t + \frac{\pi}{2}\right). \quad (37)$$

Table 3: Load specifications of three-phase BMLDLC.

RL load		Motor drive load	
Parameter		Parameter	
R	26 Ω	V	440 V
L	30 mH	I	12 A
Z	27.6 Ω	P	5 HP
		R	26 Ω
		L	30 mH
		Z	27.6 Ω
		Inertia	0.0146 kg.m^2

For a better understanding of modes of operation with the proposed BMLDCLC system, six different modes of each phase are presented in Figure 6. Further, the equivalent circuit gives a detailed understanding of the on and off states of the power electronic switch to brief current flow in the proposed converter.

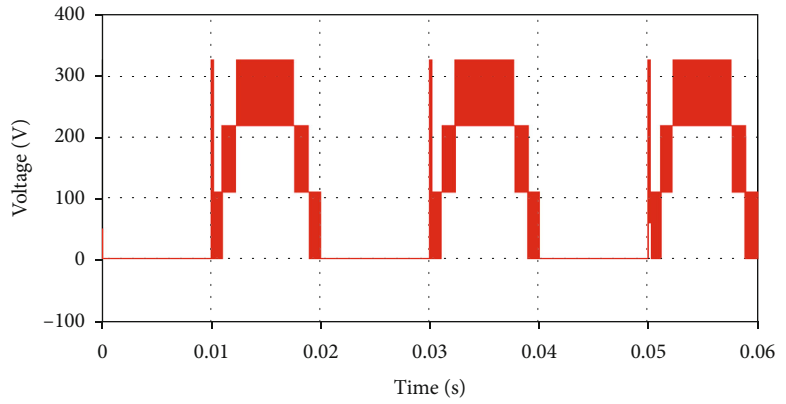
3.2.2. Estimation of Power Losses in BMLDCLC. In general, it is important to estimate the total losses that incur in a MLI. Hence, the mathematical formulations pertinent to various category to calculate losses in the proposed BMLDCLC are given in the following: (i) conduction losses, (ii) switching losses, and (iii) overall standing voltage.

(i) Conduction losses

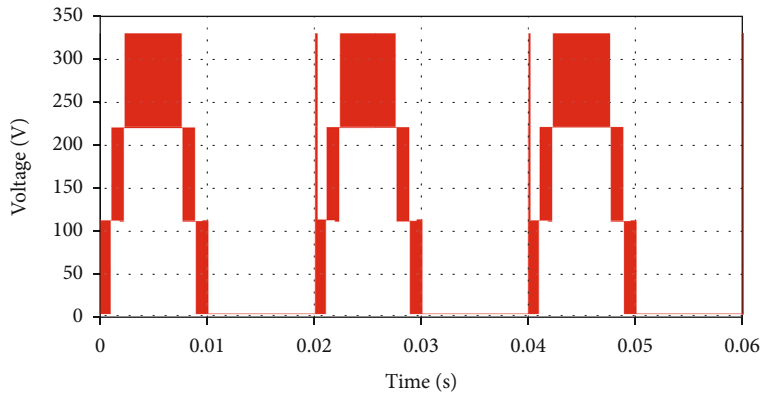
Conduction losses, in general, are associated with the power electronic switch. Nor the proposed BMLDCLC, it is seen that the conduction loss should be calculated for (i) chopper module, (ii) snubber circuit, and (iii) H-bridge inverters at the output. The mathematical equation to estimate the conduction losses of the chopper unit are premeditated in (38).

$$P_B = 3 * \sum_{k=1}^{N\text{switch}} V_{T,k}.i_{sw,k}. \quad (38)$$

Conduction losses of snubber module and H-bridge



(a)



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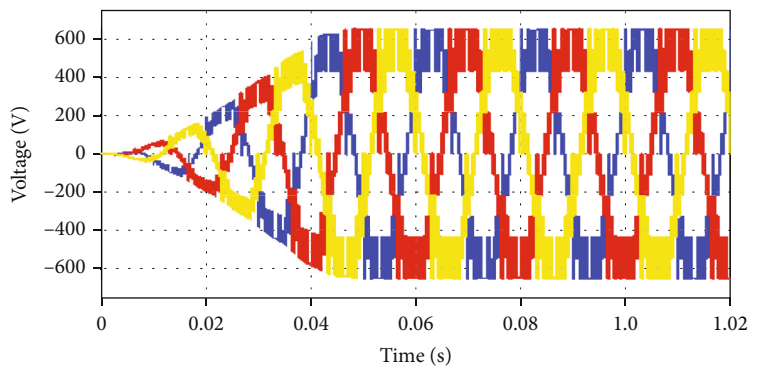
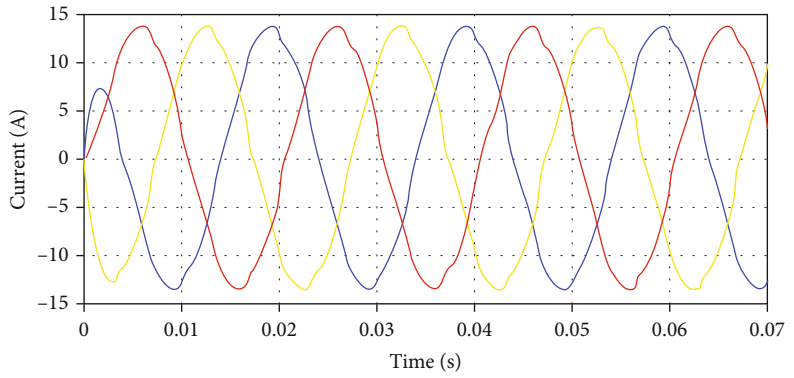
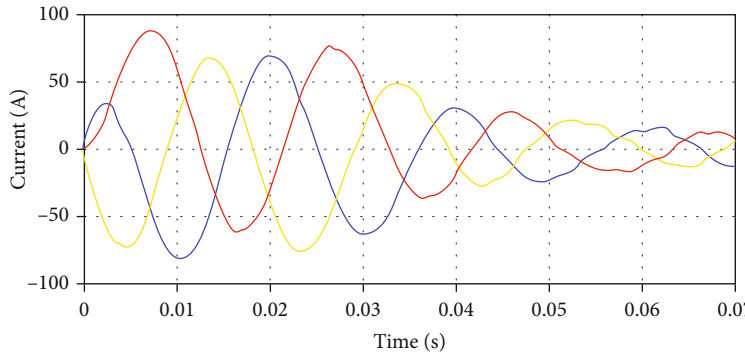


(c)

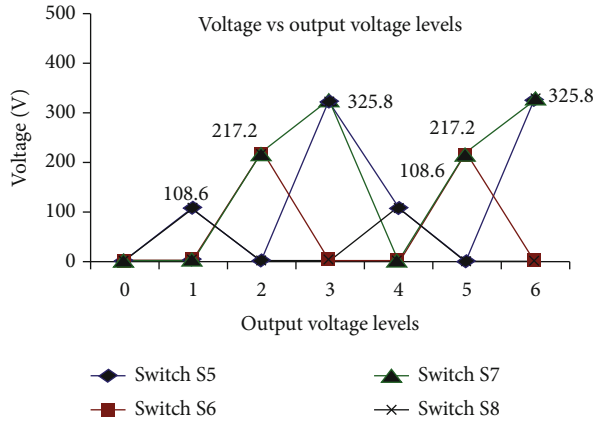


(d)

Figure 8: Continued.



(e)



(f)

FIGURE 8: (a) Voltage across H-bridge switches S_1 and S_2. (b) Voltage across H-bridge switches S_3 and S_4. (c) Output line voltage of 3ϕ BMLDCLC. (d) Load current 3-phase BMLDCLC—RL load. (e) Load current 3-phase BMLDCLC—motor drive. (f) Blocking voltage of DC-link switches.

DC to AC converter switches are analyzed as represented in Figure 2(c) and expressed by Equations (39) and (40).

$$P_{\mathrm{DCLM}} = \frac{3}{\pi \int_0^{\pi} p_{\mathrm{DCLM}}(t)\, d\omega t}, \tag{39}$$

$$P_H = \frac{3}{\pi \int_0^{\pi} p_h(t)\, d\omega t}. \tag{40}$$

The power losses of the suggested system are given by

$$P_{\mathrm{BMLDCLC}} = P_B + P_{\mathrm{DCLM}} + P_H. \tag{41}$$

(ii) Switching losses

Similar to conduction losses, switching losses of a power electronic switch are also estimated for (i) boost converter and (ii) snubber module. Switching loss pertinent to the DC-DC boost converter is estimated for both on and off time of the power electronic switch, and it is mathematically given in Equations (42) and (43).

$$E_{\mathrm{on},B} = 3 * \sum_{k=1}^{N\mathrm{switch}} V_{sw,k}.i_{sw,k}.t_{\mathrm{on}}, \tag{42}$$

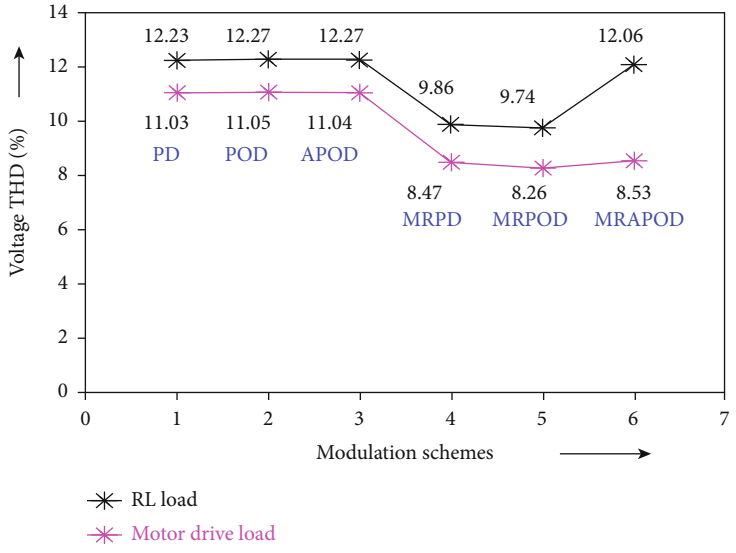
$$E_{\mathrm{off},B} = 3 * \sum_{k=1}^{N\mathrm{switch}} V_{sw,k}.i'_{sw,k}.t_{\mathrm{off}}. \tag{43}$$

The on state and off state loss of a "k^{th}" switch are estimated by using the formulation given in (44) and (45).

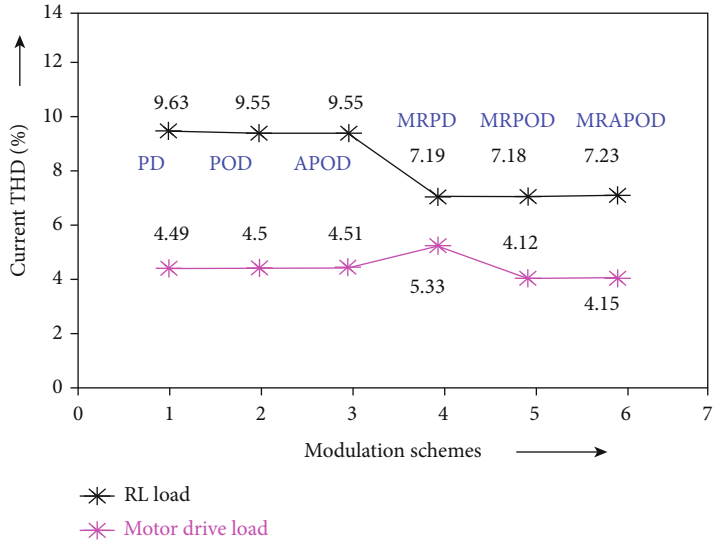
$$E_{\mathrm{on},K} = \frac{(V_{sw,k}.i_{sw,k}.t_{\mathrm{on}})}{6}, \tag{44}$$

$$E_{\mathrm{off},k} = \frac{\left(V_{sw,k}.i'_{sw,k}.t_{\mathrm{off}}\right)}{6}, \tag{45}$$

where $E_{\mathrm{on}-k}$ is the energy loss during the switch on, $E_{\mathrm{off}-k}$ is the energy loss during the switch off, and i_t is the source current flowing all the way through the power semiconductor switch subsequent to turning on. Further, on estimating the losses in a power electronic switch, the total losses in

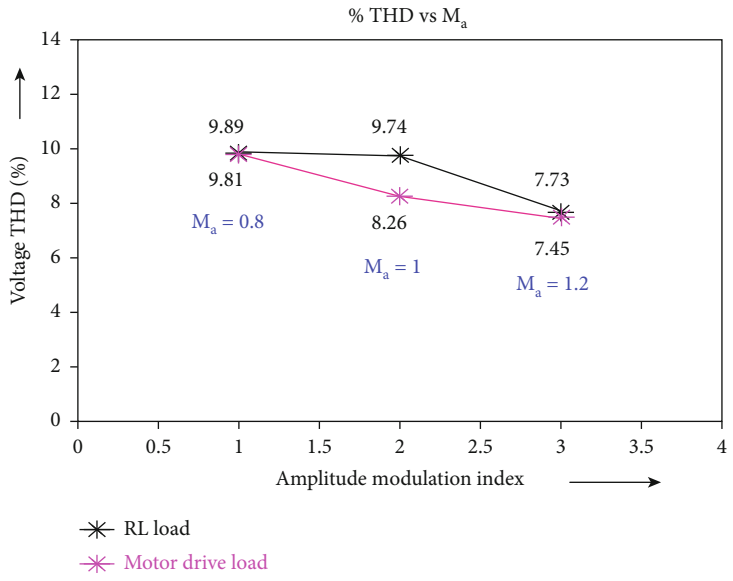


(a)

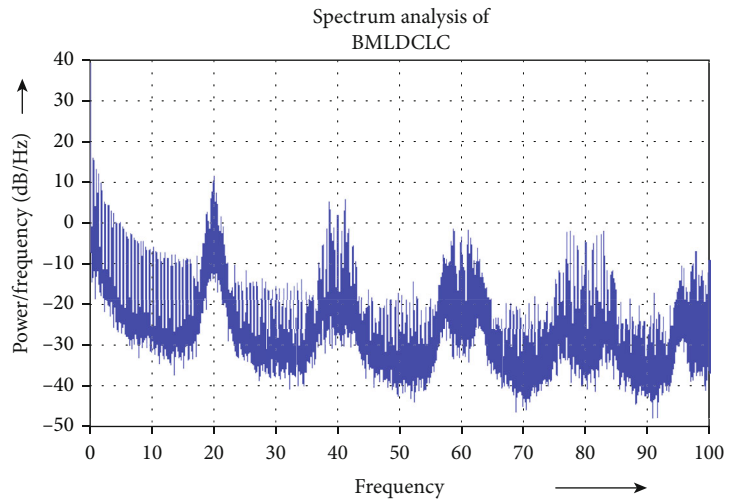


(b)

Figure 9: Continued.



(c)



(d)

Figure 9: THD investigation of the output voltage of 3ϕ BMLDCLC. (b) THD investigation of the load current of 3ϕ BMLDCLC. (c) Power Signal Density analysis for the output voltage of 3ϕ BMLDCLC.

the DC-link module can be calculated. Mathematical formulations to estimate the loss during on and off time are given in Equations (37) and (38), respectively.

$$E_{\text{on,DCLM}} = \sum_{k=1}^{N_{\text{switch}}} E_{\text{on},K}. \tag{46}$$

$$E_{\text{off,DCLM}} = \sum_{k=1}^{N_{\text{switch}}} E_{\text{off},K}. \tag{47}$$

(iii) Overall standing voltage (OSV)

Overall standing voltage (OSV) of the proposed unit is calculated as

$$\text{TSV} = \left(\frac{7s^2 + 5s - 2}{2}\right) V. \tag{48}$$

The average voltage drop at the switching frequency is 19.53 V and 20.68 V for the rated output voltage system. Hence, the average switching loss is considered as 148.6 W. Hence, the efficiency of the proposed converter is 90.9%. Losses and efficiency analysis are represented in Figure 5(e).

3.3. A Comprehensive Analysis on the Operation of BMLDCLC System in Grid-Connected Mode: Case Study.

Table 4: Harmonic investigation of three-phase BMLDCLC fed RL load (rated voltage).

Order of harmonics	$M_a = 0.8$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)
3	0.29	0.21	0.22	0.09	0.14	0.06
5	4.69	3.03	4.35	2.92	8.52	4.78
7	4.62	2.37	3.24	2.15	6.72	2.85
9	0.07	0.05	0.15	0.05	0.09	0.03
11	4.58	1.58	2.24	1.06	3.61	1.13
13	3.67	1.38	1.78	0.8	2.79	1.09
15	0.09	0.02	0.1	0.02	0.1	0.03
17	2.34	1.01	1.5	0.25	2.14	0.87
19	1.98	0.89	1.42	0.21	2.02	0.66

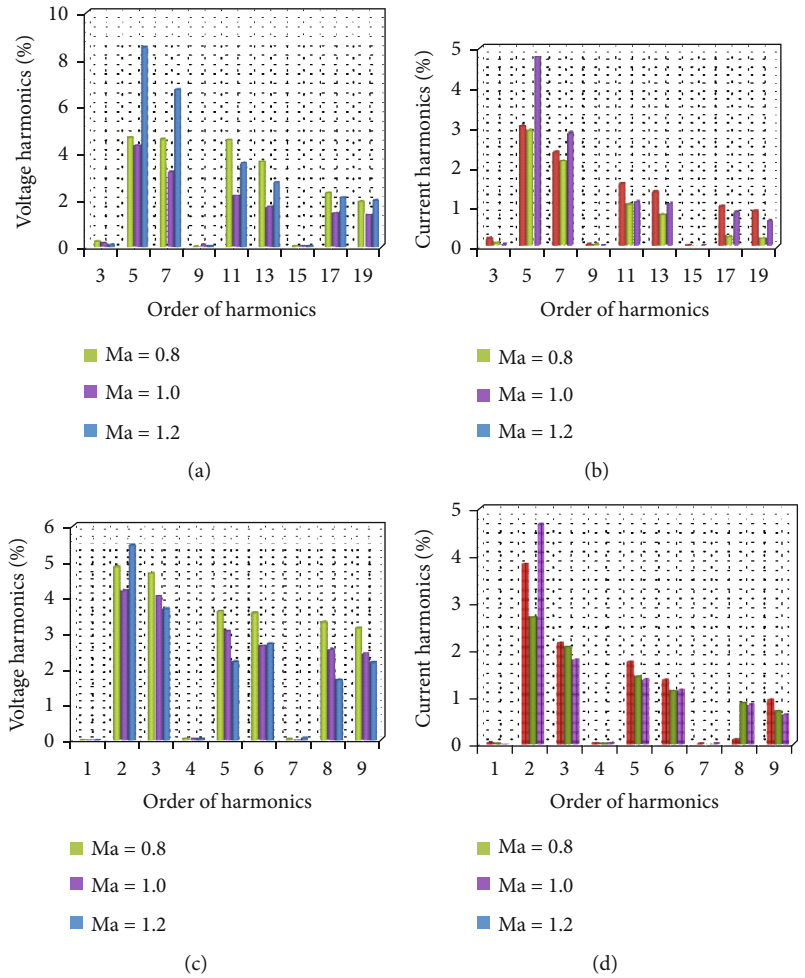


Figure 10: (a) Harmonic analysis of rated output voltage. (b) Harmonic analysis of load current. (c) Harmonic analysis of output voltage of 120 V. (d) Harmonic analysis of load current for 120 V output voltage system.

As the proposed converter arrangement is highly encouraged to get connected for a grid-connected mode, a quantitative case study on its operation to grid-connected modes is presented in this section. Design specifications of the recommended system and the data are related to voltage, and power ratings are represented in Table 1. Also, the schematic of the proposed converter connected to the utility is given in Figure 7(a). From the figure, it is understood that the

Table 5: Harmonic investigation of three-phase BMLDCLC fed RL load (for 120 V).

Order of harmonics	$M_a = 0.8$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)	Voltage harmonics (%)	Current harmonics (%)
3	0.03	0.05	0.04	0.03	0.02	0.02
5	4.87	3.82	4.21	2.71	5.46	4.67
7	4.69	2.16	4.06	2.08	3.69	1.81
9	0.08	0.04	0.08	0.03	0.07	0.05
11	3.63	1.76	3.08	1.45	2.22	1.39
13	3.58	1.38	2.67	1.15	2.72	1.17
15	0.06	0.03	0.04	0.01	0.09	0.04
17	3.32	0.12	2.57	0.89	1.71	0.86
19	3.16	0.96	2.46	0.72	2.20	0.65

proposed system has a battery bank and an isolation switch. Note that isolation is mandatory to disconnect it from the utility. Further, the proposed seven-level BMLDCLC connected to a three-phase load system offers five operating modes as follows: (i) bypass mode, (ii) off line mode, (iii) on line mode, (iv) battery-operated mode, and (v) grid-connected mode.

The operating characteristics of various modes in the grid-connected system are discussed in detail as follows:

(i) In grid-connected mode, subpanel and isolation switches are activated, and the excess power produced by the solar PV panels is imported to the grid

(ii) In off line mode, the load is operated through a solar fed BMLDCLC system. Note that subpanel and isolation switches are in off state during off line mode

(iii) In on line mode, the load is operated through solar fed battery-operated BMLDCLC system, and in the same mode, the energy storage device is acquired to completely store the energy by the solar panels through the charge controller

(iv) Battery operating mode is activated only for emergency and backup loads

In bypass mode, subpanel and isolation switches are activated, and the load is directly connected to the grid. This mode is activated only when solar power is not competent to attend to the load demand. It is noteworthy to mention here as master control manages the operation of the entire system, including the battery bank and the grid-isolation device.

From the specifications of Table 2, it is anticipated that grid-connected systems need nominal power components and PV panels compared to topologies proposed in [14, 15, 17–20]. Thus, it is confirmed that the proposed converter reduces the overall cost for grid-connected UPS applications. The inductor values of L_1 and L_2 pertinent of boost converters 1 and 2 are calculated using the following equations:

$$L_1 = \frac{V_{\mathrm{dc1}} * (V_{ob1}\text{-}V_{\mathrm{dc1}})}{(I_2 - I_1) * f * V_{ob1}}, \tag{49}$$

Table 6: Properties of various metals.

Material	Specific heat (kJ/kg°C)	Thermal conductivity (W/m°C)
Aluminum	0.99	205
Iron	0.45	79.5
Steel	0.46	50.2
Copper	0.39	385
Brass	0.38	109
Zinc	0.38	112
Water	4.18	0.6
Glass	0.84	0.8
Silver	0.23	406

$$L_2 = \frac{V_{\mathrm{dc2}} * (V_{ob2}\text{-}V_{\mathrm{dc2}})}{(I_4 - I_3) * f * V_{ob2}}. \tag{50}$$

To contribute to a fair comparative study, the BMLDCLC system is also presented in Figure 7(b) with a transformer and single-phase supply. However, the system is extremely complicated, and the use of transformers leads to higher costs. Detailed discussions on a transformerless MLI configuration fed UPS system related to (i) transient analysis, (ii) ripple current analysis, (iii) sliding mode controller analysis, and (iv) robustness and multiport analysis can be referred in [31–34].

4. Simulation Results and Discussion

The converter is tested with two various loads (i) RL load and (ii) motor drive load. Further, software-based system modelling is performed in a MATLAB Simulink environment with a system configuration of 4 GB RAM and an *i3* processor. For simulations, SPV panels are associated in series and parallel approaches to attain the source voltage $V_{\mathrm{dc1}}\text{-}V_{\mathrm{dc6}}$. Note that 250 watts PV sources having open-circuit voltage of 36 V and short circuit current as 8 A are used. Further, battery banks are connected in series and parallel approaches to achieve the source voltage of a stepped DC-link hybrid converter and to achieve an uninterrupted power supply for industrial applications. It is noteworthy to mention here that 12 V batteries having 85 AH capacity

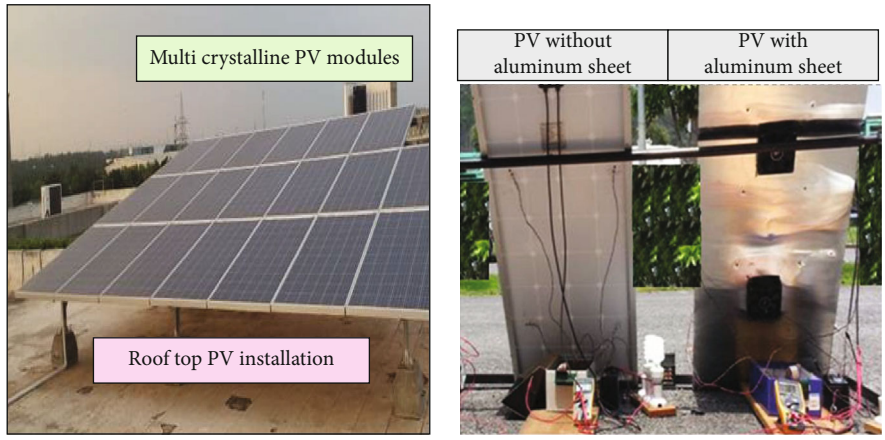


Figure 11: (a) Solar plant; (b) experimental analysis with aluminum metal sheet.

are used as a backup to serve in the absence of PV. BMLDCLC initiates its operation as boost chopper; source voltages of 36 V and 72 V are boosted up to 109 V and 216 V, respectively, to achieve the rated voltage of 415 (V_{rms}). Furthermore, the power electronic switches of the DC-DC boost converter are fed with a 10 kHz switching frequency to maintain the DC-link voltage. Additional grid-powered storage with an inverter system is also provided to run the backup loads for emergency purposes. The load specifications are represented in Table 3.

The simulation results of the snubber-assisted module are presented in Figures 8(a) and 8(b), respectively. From the acquired waveforms, it is incidental that four switch back-end conversions are performed at the zero-crossing points for every 10 ms, as presented in Figure 8(a). Thus, ensuring that switching losses is minimal. In addition, the reproduction of three-phase voltage with definite steps in the waveform gives the judicial validation of the proposed MLI. In order to operate the converter switches efficiently, peak inverse voltage across front-end switches is considered at different levels, as presented in Figures 8(c) and 8(d). Further, the voltages measured at switches give three various DC values to confirm the seven operations of the inverter. Stability analysis has been carried out for the proposed system, and it is inferred that the system is operated in equilibrium with respect to electrical parameters only after 0.05 ms. From Figure 8(c), it is noticed that the steady-state voltage is achieved only after 0.05 ms. To measure the appropriate modulation index with the proposed system, various pulse width modulation (PWM) schemes [35–37] are investigated for both RL load and motor drive load as shown in Figures 9(a) and 9(b), respectively. Over and above, the MCMRPOD-PWM technique is found effective to have reduced THD without filter component, and the same is adopted for the proposed converter topology. Further, the system has also been examined for different modulation indexes (M_a) like 0.8, 1.0, and 1.2, as shown in Figure 9(c). From the results, it is established that the projected system fed RL load and motor drive load systems generate lower THD (without filter component) values of 7.45% and 7.73%, respectively, for $M_a = 1.2$. Also, it is evidenced that hybrid converter generates 40% higher 5^{th} and 7^{th}-order voltage and current harmonics. In order to notice the strength of power signals, spectrum analysis has been conducted, and the results are shown in Figure 9(d).

PSD for the inverter voltage of the recommended inverter topology at 10 kHz, 20 kHz, 30 kHz, and 40 kHz is -6 dB/Hz, 12 dB/Hz, -18 dB/Hz, 8 dB/Hz, and -2 dB/Hz, 14 dB/Hz, -16 dB/Hz, and 4 dB/Hz, respectively. The ratio of output voltage in the recommended seven-level inverter fed RL and motor drive load systems at 10 kHz, 20 kHz, 30 kHz, and 40 kHz is 1.25%, 9.95%, 0.31%, 6.27%, and 1.98%, 12.5%, 0.39%, and 3.96%, respectively. Thus, the efficiency of the proposed converter is estimated as 90.9%, and the proposed three-phase stepped DC-link inverter has improved efficiency of 4.7% and 12.9%, respectively, against two-level and three-level boost chopped fed inverter configurations.

For an inverter, individual order harmonic ensures the converter efficiency. Hence, the voltage and current harmonics of the proposed converter are tested and analyzed for three various modulation index (M_a). The values pertinent to the order of harmonics are numerically presented in Table 4. For better understanding, a bar chart to measure harmonics in output voltage and current is plotted as shown in Figures 10(a) and 10(b). From the figure, it is noticed that 5^{th}-order harmonics get augmented for overmodulation ($M_a = 1.2$) state. In addition, the average voltage ratio for the proposed topology fed RL and motor drive load system is 4.44% and 4.70%, respectively. The system parameters are designed for the inverter output voltage of 600 V (Vm). The average output voltage of boost chopper units are as follows:

Case 1.

$$V_{ob1} = \frac{36}{(1 - 0.67)} \ (\text{assuming } K_1 = 0.67 \text{ for } M_a = 1),$$
$$V_{ob1} = 109\text{V}, \tag{51}$$

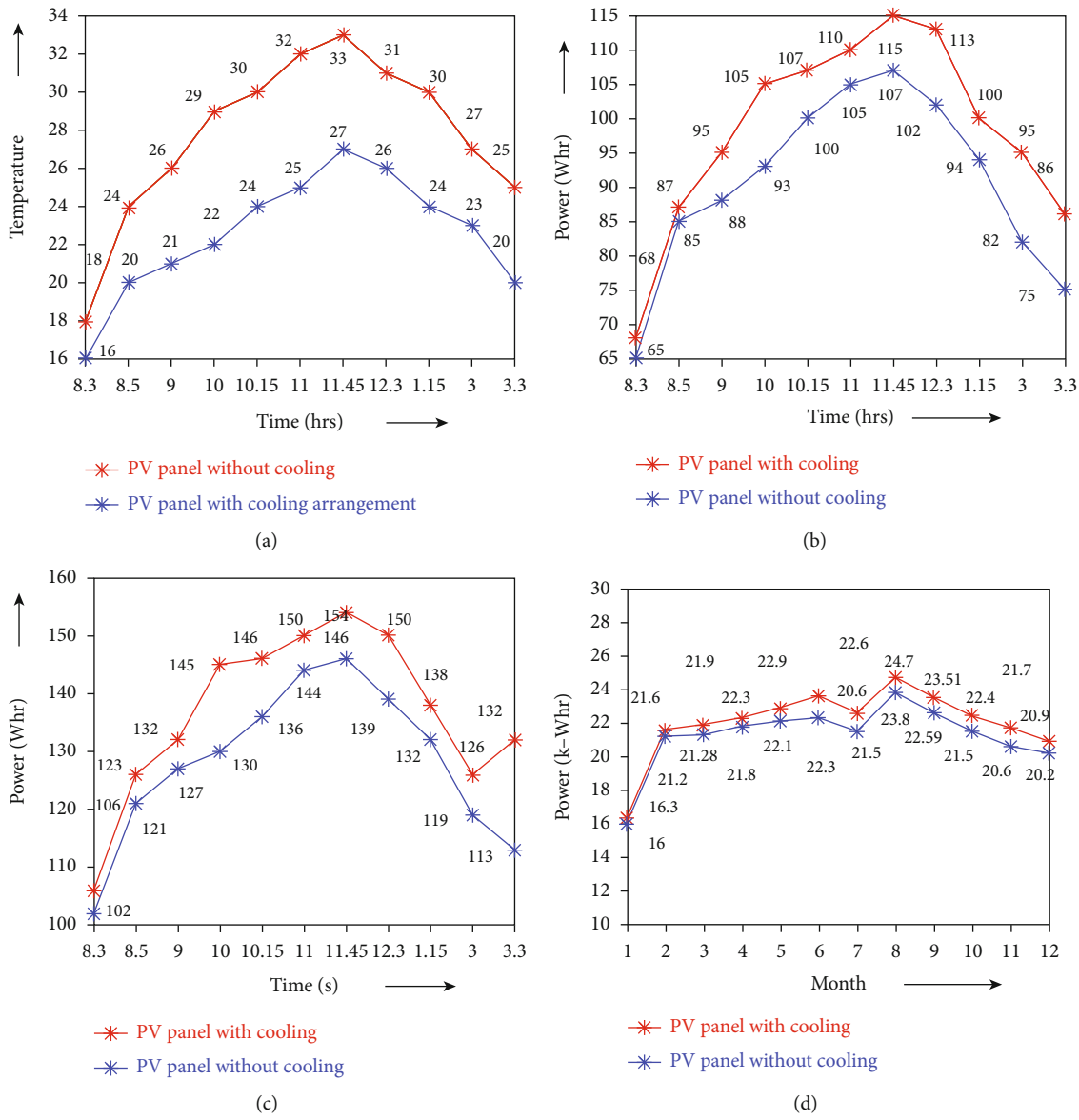


Figure 12: (a) Thermal characteristics of solar panel in the month of August. (b) Power generation in the month of January. (c) Power generation in the month of June. (d) Overall power generation for a year.

$$V_{ob1} = \frac{72}{(1-0.67)} \text{ (assuming } K_1 = 0.67 \text{ for } M_a = 1),$$
$$V_{ob1} = 216\text{V}, \tag{52}$$

Case 2.

$$\text{V}_{ob1} = \frac{36}{(1-0.73)} \text{ (assuming } K_1 = 0.73 \text{ for } M_a = 1.2),$$
$$\text{V}_{ob1} = 140\,\text{V}, \tag{53}$$

$$\text{V}_{ob1} = \frac{72}{(1-0.73)} \text{ (assuming } K_1 = 0.73 \text{ for } M_a = 1.2),$$
$$\text{V}_{ob1} = 280\,\text{V}. \tag{54}$$

Since the provisions to visualize hardware results for rated voltage is not possible, the hardware design is made for 120 V phase voltage. Thus, to validate the proposed system with 120 V as output voltage, the simulation trials of the proposed converter are repeated, and the results pertinent to the modulation index are shown in Figures 10(c) and 10(d). Further, the detailed investigations pertinent to numerical are given in Table 5.

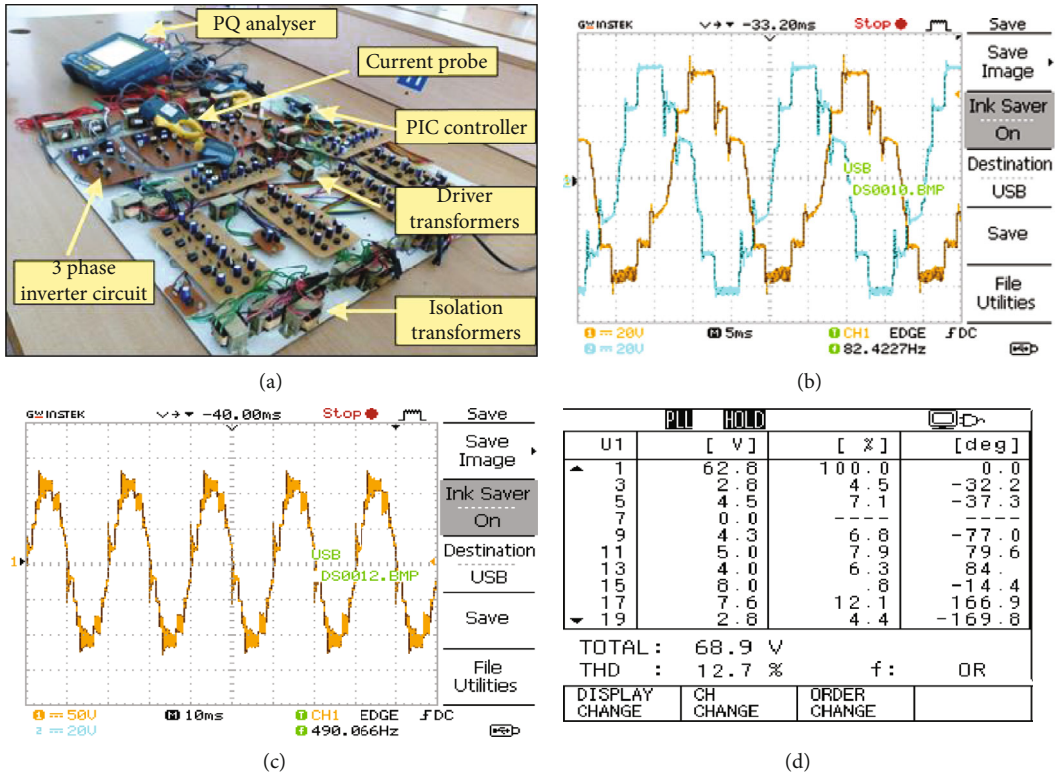


Figure 13: (a) Hardware setup of three-phase seven-level BMLDCLC system. (b) Output phase voltage of three-phase BMLDCLC. (c) Output line voltage of three-phase BMLDCLC. (d) THD spectrum.

5. Hardware Experimentation

To experiment with the proposed converter, a lab-made prototype model is exclusively constructed. Further, 250 watts PV panels installed on the rooftop of the electrical engineering building of KPR Institute of Engineering and Technology is utilized as the source. In general, SPV panels are nonimmune to geographical and seasonal variations. Further, the overall efficiency gets affected negatively by a rise in temperature. Additionally, excessive heat may significantly increase the output current, which may account for power loss up to 10-22 percentage, hence an attempt to cool PV panels with the help of temperature coefficient. In general, PV panel manufacturers provide a "temperature coefficient" (TC) value for each SPV panel, whose value varies based on manufacturing technology and materials used. This parameter can be used to determine the amount of power loss for each one degree Celsius of temperature rise.

5.1. Design of Thin Aluminum Sheet-Based Cooling System. The panel's temperature is one of the key components to drag the overall power; hence, a new method to reduce the panel temperature is explored by using thin aluminum sheet. Aluminum was chosen for its high thermal conductivity (267 watts per metre-kelvin) and low weight per square. For a fair comparative study, the thermal conductivity and specific heat of various metals are presented in Table 6. Further, the implementation cost was also found economical with aluminum metal. The experimental setup of the PV system is shown in Figures 11(a) and 11(b), respectively. From Figure 11(b), it is seen that one of the PV panels was used as it is, while the other one was wrapped with thin aluminum sheet in the rear, and the setup was also braced with two DC-cooling fans to enhance the cooling effect. The cooling fain decreases the panel temperature and helps to extract the maximum available power.

The experimental study for cooling is extended for one year, and the instantaneous voltage and power values are recorded. Further, the measure of PV thermal characteristics (PV panel temperature) is measured for the month of August and presented as shown in Figure 12(a). From the figure, it is seen that aluminum-based cooling arrangement has always maintained the temperature in limits compared to the original. To understand the impact of power generation of PV panels with cooling, the power generated from the PV plant is recorded for the months of January and June which is shown in Figures 12(b) and 12(c), respectively. Further, the total power yield for a year is also presented as in Figure 12(d). In all the aforementioned cases, the cooling effect with PV panels had a major impact to improve the power extraction from PV systems. From Figure 12(a), it is inferred that aluminum-based cooling arrangement system has an average of 5°C to 6°C better hear absorption or removal which is equivalent to 12.9% of total heat removal. As a safety measure to protect PV from dust accumulation, panels were coated with hydrophobic nano coating (HNC)

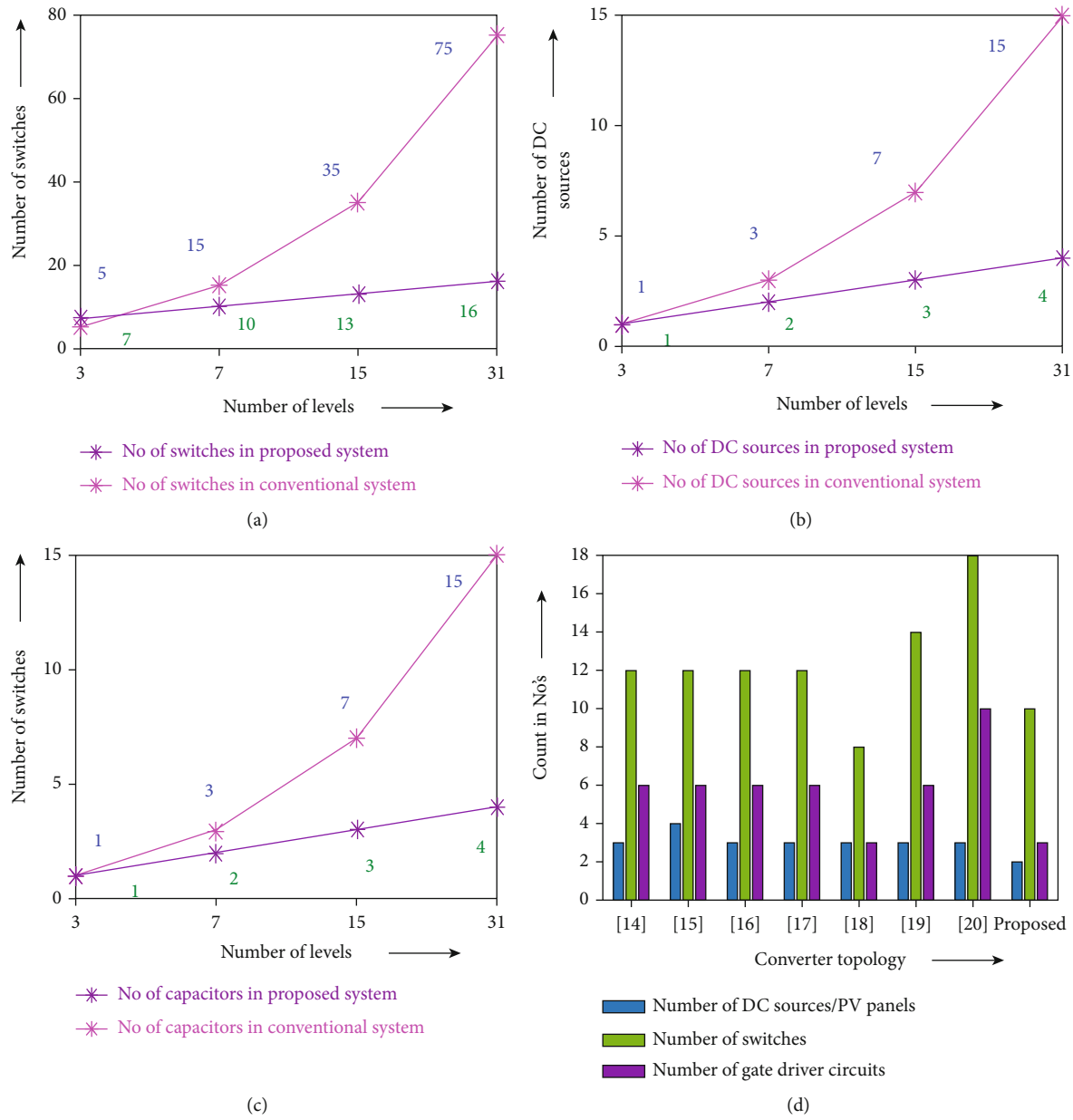


FIGURE 14: Comparative analysis of controlled switches. (b) Comparative analysis of DC sources. (c) Comparative analysis of capacitors. (d) Comparative analysis with different seven-level hybrid converter topologies.

solution. This enabled the PV to prevent from (i) accumulation of water drops, (ii) dust, and (iii) bird droppings over SPV panel surface. In addition, the arrangement has enhanced the surface contact, and the light transfer to the SPV cells was increased, ensuring the higher amount of electricity production. It is noteworthy to mention here that the use of HNN has decreased cleaning of PV panel on average.

5.2. BMLDCLC Setup. The entire system is designed and implemented as prototype model as represented in Figure 13(a). PIC microcontroller is used for providing gating sequence of the converter. Hardware results (i) output phase voltage (V_{RN} and V_{YN}) and (ii) line voltage of the 3ϕ seven-level BMLDCLC scheme are shown in Figures 13(b) and 13(c), respectively. To evaluate the virtues and system performance, the operation of proposed BMLDCLC is tested for diverse modulation indices and its electrical parameters are specified in Table 6. From the table, it is inferred that the individual harmonic is within the limit for the modulation index $M_a = 1.0$. Thus, the same is recommended for real-time operation. From the examination, it is authenticated that the 3rd, 5th, and 7th-order harmonics are mitigated through the switching schemes. Furthermore, to authenticate the simulation results, power quality analysis was conducted experimentally and the results are represented in Figure 13(d). From the investigation, the THD of the recommended system is 12.7%.

6. Comparative Analysis

In order to compare the proposed work comprehensively in a common platform, a qualitative assessment of anticipated BMLDCLC topology is made with other literatures as represented in Table 2. Various parameters considered for comparison are as follows: (i) PV panels/DC sources required, (ii) power semiconductor switches used, (iii) gate drivers used, (iv) levels in voltage stress, (v) output voltage levels, and (vi) series connected DC sources. Also, an interesting comparison related to parameters (i) number of power electronic switches, (ii) number of DC sources, and (iii) number of capacitors are considered for conventional MLI (three, seven, fifteen, and thirteen level), and it is compared with proposed inverter topology. This comparison is benchmarked as bar chart and presented in Figures 14(a)–14(c), respectively. From the comparative study, it is inferred that the proposed seven-level BMLDCLC has comparatively utilized 66.66% less (i) switching components, (ii) DC sources, and (iii) capacitors. Further, the same analysis is extended for various literature works, and it is compared with proposed inverter topology as bar chart in Figure 14(d). Yet, the proposed system topology has emerged as one of the best alternatives for existing seven-level inverter configurations. Thus, on overall, the proposed system has greater scope for real-time implementation towards industrial applications is proved. Also, the experimental findings and simulation results confirm that BMLDCLC has conceived greater interest to be as a suitable replacement for existing three-phase seven-level MLI. It is evident from Table 2 that the proposed system requires lesser number of power switches and DC sources. Analysis on the basis of system requirements has been made for various configurations. Hence, from the abovementioned table and analysis part, the authors have given a clear picture about the cost reduction for the proposed system. The comparative study confirms that the proposed 7-level BMLDCLC system has only utilized 33.33% switches compared to other conventional MLI schemes. Hence, the proposed system has the reduced cost of 175.24 US dollars compared with conventional CMLI.

The proposed BMLDCLC configuration required at least six DC sources for synthesizing 7-level three-phase AC output, which is the main limitation of the proposed system over conventional three-phase voltage source inverter system. Also, the proposed BMLDCLC configuration required three boost chopper units for achieving 7-level three-phase AC output. In future, the above constraints can overcome by integrating all the submultilevel modules with a common H-bridge inverter module.

7. Conclusion

A new BMLDCLC topology is proposed in this research work for industrial applications. Further, effectiveness of converter in real-time operating conditions is analyzed using a prototype model, and the following conclusions are arrived.

(i) The BMLDCLC is effective to reduce stress on the primary DC-DC converter since two DC sources are used to serve the DC-link voltage

(ii) The case study on grid-connected systems reveals the importance of proposed design to serve as a solution for energy management system

(iii) The comparative study confirms that the proposed 7-level BMLDCLC system has only utilized 33.33% switches compared to other conventional MLI schemes

(iv) From the power frequency spectrum analysis and perceived output waveforms, the recommended power converter is proved to reduce 41% voltage stress

(v) From the circuit analysis, it is confirmed that the output voltage is achieved without any series connected DC sources and inverter and transformer. This certainly proves the cost-effectiveness of BMLDCLC compared to conventional MLIs

(vi) A converter efficiency of 90% is recorded in real-time investigation

Abbreviations

APOD: Alternate phase opposition disposition
AC: Alternating current
M_a: Amplitude modulation index
BCMLI: Boost cascaded multilevel inverter
CLSPWM: Carrier level shifted pulse width modulation
CDCLHBI: Cascaded DC-link H-bridge inverter
CMLI: Cascaded multilevel inverter
CSI: Current source inverter
dsPIC: Digital signal peripheral interface controller
DC: Direct current
FCMLI: Flying capacitor multilevel inverter
M_f: Frequency modulation index
IGBT: Insulated gate bipolar transistor
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
MRAPOD: Modified reference alternate phase opposition disposition
MRPD: Modified reference phase disposition
MRPOD: Modified reference phase opposition disposition
MLI: Multilevel inverter
PD: Phase disposition
POD: Phase opposition disposition
PSD: Power spectral density
PWM: Pulse width modulation
SPWM: Sinusoidal pulse width modulation
SVM: Space vector modulation
SVPWM: Space vector pulse width modulation
THD: Total harmonic distortion
UPS: Uninterrupted power supply
VSI: Voltage source inverter
ZVS: Zero voltage switching.

Data Availability

The data used to support the findings of this study are included in the article.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this article.

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