

Programmable Ring Oscillator (PRO): A Multipurpose Design for On-chip Side-channel Countermeasure and Fault Detection

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Abstract—Side-channel and fault injection attacks reveal secret information by monitoring or manipulating the physical effects of computations involving secret variables. Circuit-level countermeasures help to deter these attacks, and traditionally such countermeasures have been developed for each attack vector separately. We demonstrate a multipurpose ring oscillator design - Programmable Ring Oscillator (PRO) to address both fault attacks and side-channel attacks in a generic, application-independent manner. PRO, as an integrated primitive, can provide on-chip side-channel resistance, power monitoring, and fault detection capabilities to a secure design. We present a grid of PROs monitoring the on-chip power network to detect anomalies. Such power anomalies may be caused by external factors such as electromagnetic fault injection and power glitches, as well as by internal factors such as hardware Trojans. By monitoring the frequency of the ring oscillators, we are able to detect the on-chip power anomaly in time as well as in location. Moreover, we show that the PROs can also inject a random noise pattern into a design's power consumption. By randomly switching the frequency of a ring oscillator, the resulting power-noise pattern significantly reduces the power-based side-channel leakage of a cipher. We discuss the design of PRO and present measurement results on a Xilinx Spartan-6 FPGA prototype, and we show that side-channel and fault vulnerabilities can be addressed at a low cost by introducing PRO to the design. We conclude that PRO can serve as an application-independent, multipurpose countermeasure.

Index Terms—Side-channel Analysis, Ring Oscillator, Power Sensor, Fault Attacks.

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1 INTRODUCTION

In a physical side-channel attack, an adversary learns secret information by passively monitoring or else actively influencing the implementation of a secure electronic system. While power consumption is a popular target in side-channel attacks, many other sources of physical quantities have been identified and used as side-channel leakage. Besides passive monitoring of circuit behavior, an additional cause of information leakage stems from targeted faults. By analyzing the corresponding fault response, an attacker can retrieve the secret information from a target [1]. The most common methods to inject faults include power glitches, clock glitches, electromagnetic pulses, and laser pulses. Finally, fault injection and side-channel monitoring can also be used in a combined attack, for example, to break a masking side-channel countermeasure [2].

Even though many existing works have demonstrated side-channel and fault attack countermeasures, there are no simple circuit-level solutions to solve **both** side-channel and

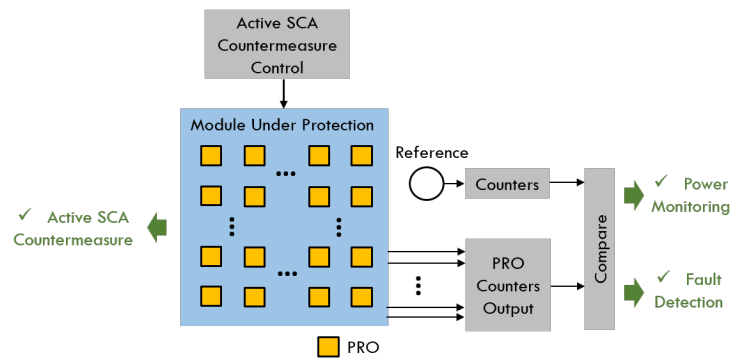


Fig. 1: PRO based on-chip Secure Network Hardware Extension

fault attack vulnerabilities in a generic manner. Generally, even for individual side-channel or fault countermeasures, a significant overhead will be introduced to the design. Moreover, many of the existing countermeasure mechanisms have to be specifically adjusted for the implemented algorithm.

In recent years, researchers have further demonstrated that the placement of the attacker and the victim circuitry on the same chip while sharing a common Power Distribution Network (PDN) brings new side-channel and fault attack opportunities. Having a common PDN intrinsically relates the perturbations from the victim's logic to the attacker's logic and vice versa. Therefore, a neighboring adversary logic can interpret information about the victim operations by monitoring the changes on the shared PDN. On the

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other hand, the same physical effect exists in the other way around; The victim logic can infer malicious operations of its neighbor circuitry by monitoring the shared PDN. Therefore, in order to guarantee the security of the PDN, a monitoring sensor network on the PDN should be built to detect on-going attacks. The monitoring sensor network should fulfill the requirements including large spatial coverage, i.e., covering the full PDN area, and large temporal coverage, i.e., continuously monitoring the PDN [3].

Previously, Ring Oscillators (ROs) were widely used by silicon design houses as test structures or on-chip sensors to monitor the performance of their technologies and circuits [4]. But a multi-purpose design of RO-based on-chip sensors has not been investigated in adding resistance against both side-channel and fault attacks to the circuit. In this work, we introduce a new multi-purpose Ring Oscillator design - programmable RO (PRO). With a low overhead, the proposed PRO can provide the following solutions within the same structure:

- Active Side-channel hiding countermeasure;
- On-chip power monitoring;
- Fault injection monitoring;

The proposed PRO design has multiple configurations of oscillation frequency, which are under the control of the user (i.e., the defender). Each PRO has its own counter which can be read to calculate the PRO's frequency by comparing it with a reference counter. We first demonstrate that with low overhead, an individual PRO can provide sufficient disturbance to the power to hide the side-channel leakage of the secret information in the system. Moreover, we further demonstrate that by combining multiple PROs into an array and by placing them within the module under protection, a secure on-chip monitoring network can be constructed to monitor the power fluctuations on the PDN to detect abnormalities and fault attacks.

Figure 1 shows the overall structure of the PRO-based on-chip secure system. The PROs are evenly placed on the chip to form a secure on-chip network. The PRO secure network can be controlled by the external user configuration. The user can turn on the Side-Channel Analysis (SCA) countermeasure by configuring the PRO to oscillate at randomized oscillation frequencies. Besides, the user can monitor the oscillation frequency of each PRO in the array by reading out its corresponding counter value. We demonstrate that by monitoring the frequency change of the PROs, on-chip local power attacks and EM fault injections can be detected.

The proposed design can be used on any secure module, from small hardware accelerators to complex System-on-Chips (SoCs). To the best of our knowledge, this is the first work to comprehensively study the potential of RO-based designs in SCA countermeasure, power sensing, and fault detection.

Adversary Model

PRO covers adversaries with side-channel and fault attack capabilities listed in the following:

Side-channel Attacker Model. We consider two attacker models. The first attacker model has physical access to the

device which enables the attacker to control the input data and monitor the power dissipation by shunting the device's power supply. The second attacker model works remotely; The attacker circuit shares a PDN with the victim circuit and can control *only the attacker circuit* remotely. Therefore, the attacker is able to implement malicious logic to monitor the changes on the shared PDN and measure the power consumption of the device [5], [6]. This enables the attacker to perform side-channel attacks, such as Simple Power Analysis (SPA) [7], Differential Power Analysis (DPA) [8], and Correlation Power Analysis [9], to retrieve the secret information used in the victim circuit.

Fault Attacker Model. We also assume the adversary can induce faults into the victim circuit by stressing the electrical environment, such as injecting clock glitch, power glitch, and EM glitch. These glitches can induce targeted transient faults which can flip bits, change the control flow of the secure algorithm, set/reset the circuit, etc. Fault injection can be done either by exerting disturbance to the circuit directly, which requires the adversary to have physical access to the device, or by having remote access to the shared cloud computing environment with the victim circuit [10], [11], [12], [13]. The exact fault effects to the circuit highly depends on the fault injection parameters, victim circuit's architecture and algorithm, and fault injection technique. By monitoring the fault response of the circuit after injecting targeted faults, the adversary can retrieve the secret information by performing Differential Fault Analysis (DFA) [14], Statistical Fault Analysis (SFA) [15], or instruction skip attacks [16]. PRO as a secure on-chip add-on can be integrated to the circuit to protect against the aforementioned attackers. Adversaries may try to tamper with the PRO sensor itself to bypass the PRO's security mechanisms, but we don't consider this adversary model within this work.

The structure of the paper is as follows. The next section reviews related work of Ring Oscillators and highlights our contribution. Section 3 describes our proposed PRO design. In Section 4, we explain and demonstrate the effectiveness of PRO as a side-channel countermeasure. Next, we present the PRO's power sensing functionality in Section 5. We further show that PRO can detect power fault and EM fault in Section 6. Finally, we conclude the paper in Section 7.

2 RELATED WORK

When sharing the same PDN, seemingly unsuspecting parts of the implemented logic can perform adversarial operations on the other parts. In this work, our focus is on two categories of adversarial operations; fault injection and power side-channel analysis. In the following, we categorize the related work into three parts: using on-chip logic as a countermeasure against power SCA, using on-chip sensors as power sensors to detect power perturbation, and using on-chip sensors to detect fault injection attacks.

2.1 On-chip sensors as a countermeasure against power SCA

Liu et al. [17] use an array of ROs, randomly switched on and off, to dynamically hide the power consumption of AES SBox and hinder the first-order Differential Power

Analysis (DPA). Similarly, Krautter et al. [18] use ROs as a power-based SCA mitigation methodology. In their work, the part of the implementation that needs to be protected is surrounded by a network of ROs. By switching an arbitrary number of the ROs on and off, the Signal-to-Noise Ratio (SNR) in power traces decreases, and therefore, the number of traces required for a Correlation Power Analysis (CPA) attack to be successful is increased. This approach is called *hiding* side-channel leakage. However, the RO in both designs are running at a fixed oscillation frequency, and thus, only a single-frequency noise is injected. In this case, it is straightforward for an attacker to apply post-processing techniques to remove the noise effect. To avoid this weakness, PRO uses user-controlled but random frequency changes (Section 4). Moreover, to further reduce the overhead, we show how a simple modification can enhance the countermeasure efficacy.

2.2 On-chip sensors to detect/cause power perturbation

Zick et al. [19] use ROs to measure on-chip voltage variations. Indeed, the oscillation frequency is proportional to the supplied voltage on the PDN. To measure the frequency of an RO accurately, counters are required that are clocked with the output of the RO. This limits the maximum sample rate attainable by the RO counter structure, and hence, the bandwidth of the side-channel signal. This limitation has motivated research on other voltage-sensitive Time-to-Digital Converter (TDC) methods. For instance, Gnad et al. [20] use carry-chain primitives available on Xilinx FPGAs as TDCs. However, the use of carry-chain primitives makes their approach specific to certain FPGA families. Similar TDC structures have been explored in the context of CMOS design simulation to measure the operating voltage of a chip [21].

Moreover, ROs have been used in offensive scenarios affecting the PDN for both passive (power-based) and active (fault injection-based) physical attacks. As an example of power-based SCA, Zhao et al. [5] presented on-chip power monitors with ROs. They demonstrated that ROs can be used as a power monitor to observe the power consumption of other modules on the FPGA or SoC. Using their power monitor, they captured power traces of the device running the RSA algorithm and were able to successfully find the private key by applying Simple Power Analysis (SPA). Gravelier et al. [22] perform CPA on power traces acquired with RO-based power sensors.

To inject timing faults, Mahmoud et al. [10] employ ROs to increase the voltage drop on the power network and lower the voltage level. Effectively, they make the victim chip slower, causing timing faults. Similar attacks have been shown in other works [11], [12], [13].

2.3 On-chip sensors to detect fault injection

Next, we consider on-chip sensors for fault detection. Miura et al. [23] present a sensor consisting of Phase-Locked Loop (PLL) and ROs. In their work, ROs are routed in a specific way to ensure their path travels through most parts of the chip. Once an EM fault is injected, the path delay of the ROs will be affected, resulting in changes in the RO phase. The

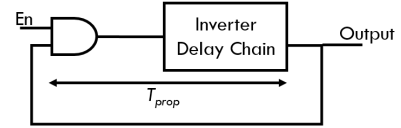


Fig. 2: Propagation delay of a ring oscillator.

PLL logic can capture this phase disturbance and detect the ongoing fault injection. Similarly, He et al. used PLL block to detect the laser disturbance on RO oscillation frequency [24].

Provelengios et al. [12] show that on-chip ROs can not only detect fault injection, but also locate the origin of the fault injection. With a similar structure, RON [25] builds a ring oscillator network, distributed across the entire chip, to detect hardware Trojans. Their work confirmed that RO-based power sensors can have a sufficiently high sample rate to detect fluctuations on the PDN.

However, the scope of their work is limited to the power fault detection, whereas, in our work, we further investigate EM fault detection (Section 6). Additionally, the unique programmable design of our proposed RO structure also enables its usage for power SCA countermeasure (Section 4).

2.4 Our contribution

In general, each previous work addresses one single aspect at a time: a side-channel countermeasure, a power monitor, or a fault detector. In practice, an adversary is capable of performing a combination of attacks. Hence, it is crucial to find a security mechanism that encapsulates protection against these attacks. Our goal in this work is therefore to design a *programmable* RO structure that can provide the following functionalities within the same structure:

- 1) Hiding protection against power-based SCA.
- 2) On-chip power monitoring of the fluctuations on the PDN.
- 3) Detecting fault injection.

To the best of our knowledge, this is the first work to comprehensively investigate the RO's potential in addressing all these three aspects. In the following sections, we introduce our proposed design and demonstrate through experiments the capability of the proposed system. Even though we demonstrate our experiments as an FPGA prototype, our design is not limited to FPGAs and can be extended to other electronic chips.

3 PROGRAMMABLE RO DESIGN

3.1 Background

In this section, we introduce our Programmable RO (PRO) sensor design. As shown in the Figure 2, Ring Oscillator (RO)'s output oscillation frequency depends on the propagation delay of their internal signals. In each oscillation period of a RO, the signal has to propagate twice through the propagation path. Therefore, the oscillation period (T_{RO}) of a RO is $T_{RO} = 2 \cdot T_{prop}$ and its frequency follows the following equation:

$$f_{RO} = \frac{1}{2 \cdot T_{prop}} \quad (1)$$

More specifically, the propagation delay path is composed of an odd number of inverters and each inverter contributes to the delay of the path. If t represents the delay of an individual inverter, and n denotes the number of inverters in the chain, its frequency follows the following equation:

$$f_{RO} = \frac{1}{2n \cdot t} \quad (2)$$

Hence, the frequency of a RO can be controlled by adjusting the number of stages in the inverter chain.

3.2 PRO Design and Configuration

In this work, we aim to have a programmable design of the RO which gives the designer the flexibility to choose the RO oscillation frequency.

Figure 3 shows the basic structure of our proposed design of the programmable sensor. The PRO consists of multiple delay cells. Each delay cell includes two delay paths; one consisting of inverters and the other a shorting path which bypasses the inverters. The multiplexer in the delay cell can control the delay cell's propagation delay by selecting between the delay path and the shorting path with the control input signal SEL . Each delay cell has its independent control signal. Suppose there are N inverters configured in the delay cell, when $SEL = 1$, the delay path is selected and when $SEL = 0$, the shorting path is selected. The propagation delay of each delay cell T_C is therefore:

$$T_C = SEL \cdot T_d + (1 - SEL) \cdot T_s \quad (3)$$

Where T_d denotes the propagation delay of the delay path and T_s denotes propagation delay of the shorting path. The propagation delay of the shorting path T_s is a very small value compared to T_d but not 0, this is because of the delay of routing and the delay of the multiplexer. Other user control inputs include EN which controls whether PRO is enabled (oscillating) or not, and a control signal to reset/read the PRO counter. The structure of the PRO design gives flexibility to the designer in manifold. As shown in Table 1, there are multiple initial structural configurations to be decided by the hardware designer at design time, including the number of inverters per delay cell, as well as the number and type of different delay cells. These parameters determine the range of the programmable RO's oscillation frequency and the number of frequency configurations the programmable RO can have.

Several constraints can be used as the guidance while configuring the Initial Design Configurations of PRO:

- 1) Oscillation frequency range;
- 2) Number of configurations;
- 3) Size of frequency changing step;
- 4) Area;

As a starting point of PRO parameter configuration, the designer should estimate the propagation delay T_{prop} for a single inverter. This knowledge can be obtained through the design library, timing simulation, or measuring RO's oscillation frequency with a single inverter (when working on an FPGA environment). Then, based on the designated Oscillation frequency range of PRO, the designer can calculate the minimum and maximum number of inverters are needed by

TABLE 1: Configurations for PRO

Configuration Type	Configurations
Initial Design Configurations	number of delay cell type, number of delay cells, number of stages in delay cells
User Configurations	EN , $SELs$, Counter Start/Stop

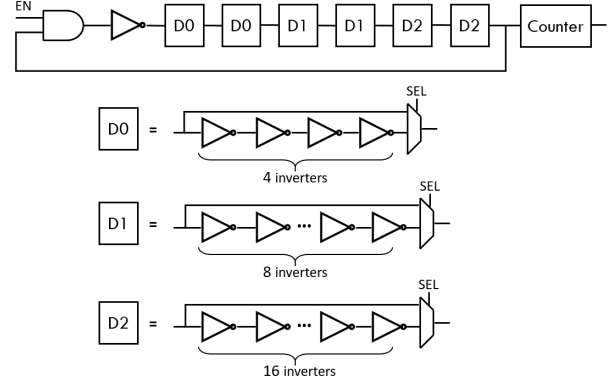


Fig. 3: PRO Design. D0 donates the delay cell type-0, D1 donates the delay cell type-1, D2 donates the delay cell type-2.

Equation 2. After deciding the number of inverters needed, the designer can group the inverters into different types of delay cells based on the designated frequency changing step and number of configurations that are needed. Theoretically, more inverters result in a larger oscillation frequency range at a cost of larger PRO area. Therefore, based on the targeted protect design area, the designer should decide the area constraint for the PRO, so that the each PRO can have a good spatial coverage of the design while at the same time wouldn't be too close to influence other PROs' local power distribution.

Next, to better explain our proposed structure, we pick one configuration as an example. Figure 3 shows the structure of the PRO with three types of delay cells. The type-0 delay cell (D0) has 4 inverters, the type-1 delay cell (D1) has 8 inverters and type-2 delay cell (D2) has 16 inverters. We instantiated 2 of each type of delay cells in the inverter chain. All the delay cells have an even number of inverters, and 1 inverter is instantiated at the start of the inverter chain to make sure that there is always an odd number of inverters in the inverter chain. When all the inverters are configured to be used in the delay path, the propagation delay T_{prop} is maximal, therefore, the overall programmable RO will oscillate at its lowest frequency. When all the delay cells are configured to use the shorting path, the propagation delay T_{prop} is minimal, therefore, the overall programmable RO will oscillate at its highest frequency.

In our experiment setup, we implement PRO on Xilinx Spartan-6 FPGA, which is fabricated with 45nm CMOS technology. Under the aforementioned configuration, we measured that the lowest oscillation frequency is 22MHz and the highest oscillation frequency is 123.44MHz. Since each delay cell's SEL is independent, there are in total 15 frequency configurations consisting of $\{1, 5, 9, \dots, 57\}$ inverters. Since there are six SEL signals, there are 64

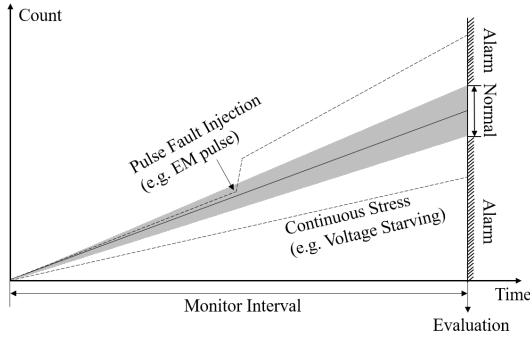


Fig. 4: Basic principles for PRO fault detection

configurations in total which redundantly map into the 15 achievable configurations. Through this redundancy, we are able to estimate the local manufacturing process variations, which is helpful to decide when a deviation should be cause for alarm (i.e., fault detection) or not.

The designers can control the RO's frequency by setting the input value of SEL. We are using the same configurations for all the later experiments in this paper. For under this PRO configuration, each PRO can be implemented with 128 LUTs and 32 Registers, in total 160 slices. In our experimental setup, a PRO array with 36 PROs can cover the whole FPGA (46648 LUTs and 93296 Registers, in total 139944 slices) to provide the whole chip power monitoring and fault detection. Therefore, only an overhead of 4.1% is introduced.

3.3 PRO Integration and Basic Principles

As a security resistance add-on, PRO can be integrated into the design to protect simple designs such as hardware encryption engines as well as complex systems such as an SoC. Control signals are needed for communicating with the PRO. The control signals set up the user control configurations in Table 1. Generally, different control mechanisms can be adopted by the designer. In an SoC, the designer can add PROs as a co-processor which can be controlled by the processor through memory-mapped registers. Under this environment, the software running on the processor can configure the PROs on the chip. Therefore, PRO-based countermeasures can be dynamically enabled/disabled while the software is running. Besides, a hardware-based Finite State Machine (FSM) can be used to control the PROs as well. In our experiments, we are using the UART protocol to communicate with PRO, and the control signals sent through the UART are generated by a python script in this paper.

Figure 4 shows the high-level basic principles for the fault detection mechanism using the PROs. The counter value will be evaluated at the end of each monitoring interval and compared with the reference counter value to get the actual oscillation frequency of the PRO. Under normal circumstances, each PRO oscillates at a certain constant frequency, and thus, its counter value will increase linearly during the monitoring interval. There will be some small variances caused by the environmental changes, jitters, process variance of the manufacturer, etc. A characterization procedure, therefore, is needed to define the range of normal operation [3]. However, in the occurrence of instant fault

injection (e.g. power glitch, EM pulse, time glitch, laser pulse), the counter will be disturbed. The counter value read out at the evaluation time will deviate from the normal range, and thus, a pulse fault injection will be detected by the PROs. Additionally, an adversary can inject timing faults by stressing the PDN continuously (e.g. power starving). As a result, the victim circuit will operate slower and cause timing violations to create faults. In this case, the PRO counter value will also deviate from the normal value and capture the fault injection event. In this paper, we use power fault and EM fault as an illustration, but PRO's fault detection coverage is not only limited to these two fault types.

4 SIDE-CHANNEL COUNTERMEASURE

Masking and hiding are two popular techniques for side-channel countermeasures. In masking, each secret variable is split into two or more shares which are concealed by random numbers. The side-channel leakage of each share alone does not reveal the secret variable because of the randomization introduced by random numbers. A random source that provides fresh random variables is significantly important in masking implementations. Hiding countermeasures reduce the SNR for secret data-dependent operations. Hiding can be achieved by several techniques, such as by reshuffling cryptographic operations in a data-dependency consistent but random order [26], inserting random delays [27], and running multiple tasks in parallel [6]. In this work, we utilize the proposed PRO design as a hiding countermeasure by injecting noise with random frequency. Previous work has proposed injecting noise for reducing the SNR [28] [29]. However, since only single-frequency noises are injected, it is not tricky for an attacker to decrease the effect of noise either by using a band-pass filter while collecting traces or by post-processing the collected power traces, such as applying averaging, filtering, and frequency domain analysis. Thus previously proposed noise-injection-based hiding mechanisms still have security flaws. In our proposed design, we inject random-frequency noises with the PRO design so that it will be much harder for an adversary to eliminate the noise.

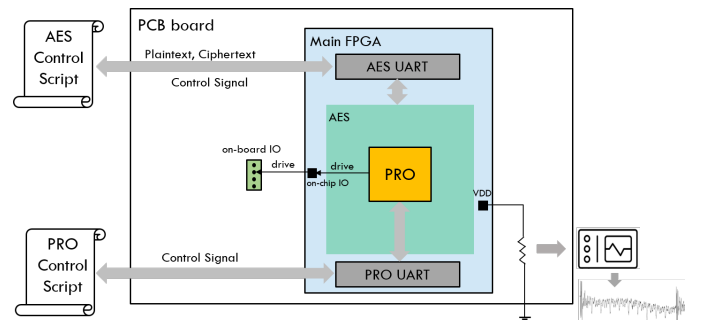


Fig. 5: Experimental Setup for Evaluating RO's performance in side-channel leakage hiding

The countermeasure circuit consists of a single PRO whose frequency can be controlled by the SEL input signals. The PRO drives one of the IO pins on the board. As demonstrated in previous work [29] [30], the power consumed by a single RO is not large enough to have a significant influence

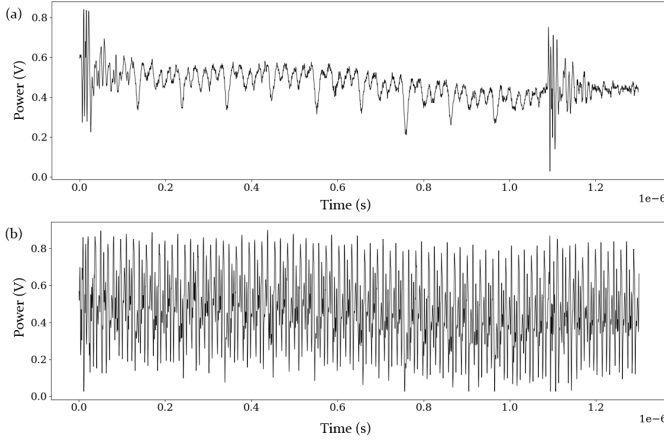


Fig. 6: AES power traces when PRO is (a) Off; (b) On;

on the power profile of a complete chip or a complete cipher. Instead, hundreds of RO need to be instantiated on the chip to have a profound hiding influence. This approach will cause significant design overhead and has the potential risk of inducing power fault to the circuit [31]. In our proposed mechanism, by driving an I/O pin with a PRO, the effect of a single (randomly-switched) PRO to influence the off-chip power network is amplified. Since the load capacitance of an IO-pin is much larger than the load capacitance of an internal FPGA net, the IO-pin requires more energy to charge and discharge. In this manner, even with a single Programmable Ring Oscillator (PRO), significant additional power is consumed to change the power consumption characteristic. In practice, an adversary senses the on-chip power consumption using a probe, either by connecting an external probe to the system via a power supply pin [32] or else using an EM probe. Both of these are dependent on the off-chip power network, and therefore, affecting the off-chip power network is an important factor to defeat an attacker maliciously monitoring the power profile.

The performance of our proposed hiding countermeasure design is evaluated with AES. Figure 5 shows our experimental setup. We put hardware AES as well as the programmable sensor on the FPGA. The output signal of the PRO is mapped to drive the IO pin to amplify the noise effect. For each encryption scenario, plaintext and ciphertext are provided through the UART for AES. The communication procedure is controlled by the AES control script. At the same time, we use the sensor control script to send in control signals through the PRO UART. The control signals can enable/disable the RO and configure the oscillation frequency of the RO. While AES is running, the sensor's control script generates random numbers for the frequency configuration so that the frequency of the PRO can change randomly. Equally, an on-chip Pseudo-Random Number Generator (PRNG) can be used for this purpose. Figure 6(a) shows the collected AES power trace when the programmable sensor is off. We can clearly see the pattern of ten rounds of the AES algorithm. By comparison, the power trace changes to a repeated oscillation pattern when we turned the PRO on, as shown in Figure 6(b), which indicates the strong influence of PRO on the power profile. Under our setup, the complete AES takes 41ms, and we configure the PRO control script such that the frequency of the PRO

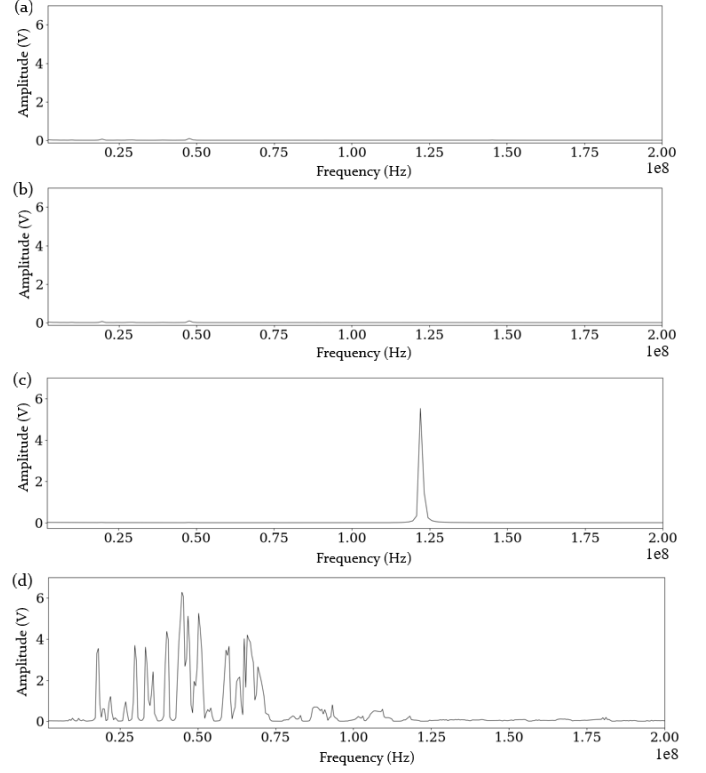


Fig. 7: Power Spectrum for power traces when (a) PRO off; (b) PRO on without driving IO pin; (c) PRO with fixed oscillation frequency and driving IO pin; (d) PRO with random oscillation frequency and driving IO pin;

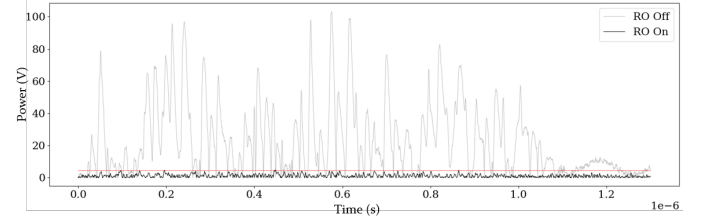


Fig. 8: T-value Comparison when PRO is on/off

changes every 2ms, which means that the PRO's frequency will change at least 20 times while AES is running. Figure 7(a) shows the frequency spectrum of the power traces when the PRO is off. We can observe small peaks at the clock frequency (24MHz). We do not observe a significant influence on the power spectrum if we only put a single PRO without driving the IO pin. Figure 7(c)(d) shows the power spectrum when the PRO is on and driving the output pin. By comparing to Figure 7(a), a significant influence on the frequency spectrum of the power profile can be observed while PRO is on. Figure 7(c) shows a sharp peak when we fix the PRO's oscillation frequency to 120MHz.

Suppose one tries to protect the secure component by injecting noise with a regular RO with a single oscillation frequency. It is easy for the attacker to implement frequency spectrum analysis, find the injected noise frequency, and apply the corresponding filter to eliminate the influence of the injected protection noise. As a sharp comparison, Figure 7(d) shows that when random frequency noise is injected by PRO the frequency spectrum is expanded within

the PRO's oscillation range from 22Mhz to 123.44Mhz. This makes it much harder for the adversary to filter out the noise by post-processing. To further evaluate the effectiveness of the proposed design on increasing side-channel resistance, we applied TVLA [33] on 50k collected traces; As shown in Figure 8, a dramatic decrease of t-value can be observed when the PRO is turned on compared to when the PRO is off. This indicates that the PRO design can significantly reduce the side-channel leakage of the circuit.

Note. Generally, even though the adversary is aware of the noise signal, since the noise is injected by PRO at a random frequency which also changes at a fast pace, it is exceedingly hard to remove its effect by normal post-processing techniques; The adversary needs to monitor both the power consumption and the output of the PRO simultaneously with sufficient precision and should be able to remove the part of power consumption related to the output pad's oscillation using noise-cancellation techniques, which requires high-end devices. Additionally, to have sufficient information and perform a successful side-channel analysis from the obtained side-channel traces, the sampling rate for side-channel attacks has to be at least $2\times$ the clock frequency (according to the Nyquist theorem). We suggest that while choosing the initial design configurations in Table 1, the designers should adjust the configurations such that the oscillation frequency range of the PRO covers at least $3\times$ the clock frequency. Under our experimental setup, the clock frequency is 24MHz. Therefore we configured PRO's oscillation frequency to 22MHz - 123.44MHz, which covers about $5\times$ the clock frequency. As a result, the adversary will need a higher-end device with a much higher sampling frequency (at least $10\times$ the clock frequency) to successfully apply the same side-channel attack. Hence, PRO as a hiding countermeasure makes it much harder to attack the circuit by largely elevating the technique bar for the adversaries.

5 POWER SENSING

In this section, we demonstrate the on-die power monitoring functionality of the proposed PRO design. Power integrity is essential to guarantee the nominal function of the circuit. Therefore, monitoring of the fluctuations on the PDN is critical to detect abnormalities. We first explore the PRO's oscillation frequency with regard to the external power deviation. Then, we look into the PRO's performance in terms of local power sensing on the PDN of the chip.

Electric circuits use PDNs to deliver power to the transistors in the circuit via external voltage regulators. PDNs are still affected by sudden current consumption changes despite these voltage regulators. Thus, the sudden change in the switching activity induces transient voltage drops in the PDN. PDNs can be modeled using RLC networks. The transient voltage drop seen by the PDN can be defined as follows

$$V_{drop} = IR + L\frac{di}{dt} \quad (4)$$

Here, the IR drop is due to the resistive components of the PDN and is dependent on the steady-state current I. The other term, $L\frac{di}{dt}$, influences voltage drop due to the

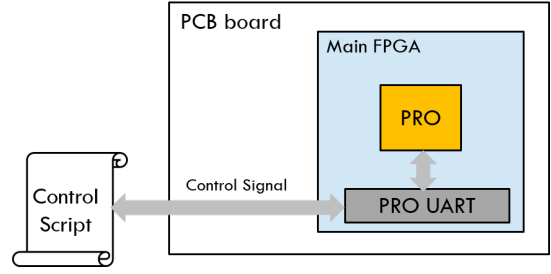


Fig. 9: Experimental Setup for PRO frequency changing as a function of external power supply

inductive components of the PDN and is dependent on the changes in the current over time. Hence, as soon as there is a high current consumption/variations due to some switching activities of the logic circuit, the voltage drop will increase.

The propagation delay of signals is affected by the on-chip voltage level; Higher voltage levels increase the switching speeds of transistors, whereas lower voltage levels decrease them. Since the voltage level affects the propagation delay of signals, the immediate frequency of a ring oscillator can indicate the level of the voltage on a chip. We take advantage of this property in our proposed PRO sensor to monitor the integrity of the on-chip power network.

5.1 PRO Power Sensing with Regard to External Power Variations

We first investigate the PRO's frequency with respect to external power variations. Figure 9 shows the setup for this experiment scenario. We put a single PRO sensor on the FPGA. For the PRO's frequency measurement, we start the PRO sensor's counter and system clock counter at the same time. After running for an arbitrary amount of time T_{arb} , we read out the RO sensor's counter value C_{RO} and the reference system clock counter value C_{clk} through UART. Then, we calculate the PRO's frequency by:

$$f_{PRO} = \frac{C_{PRO}}{C_{clk}} \cdot f_{clk} \quad (5)$$

Where f_{PRO} is the PRO sensor oscillation frequency, f_{clk} is the reference clock frequency. We measure the value of C_{PRO} 1000 times and take the average for better precision. The measurement procedure is automated through a control script running on a PC.

As we mentioned in Section 3, the PRO's oscillation range is 22 Mhz to 123.44 Mhz. To investigate the PRO's power sensing sensitivity when operating under different frequencies, we set the PRO sensor to several oscillation frequencies at the starting (highest) power supply voltage for the main FPGA core (1.33V). The frequency configurations we pick are 153.2MHz, 100MHz, 66.8MHz, 40.5MHz, and 27.2MHz. We gradually decrease the FPGA's supply voltage and monitor the PRO sensor's oscillation frequency.

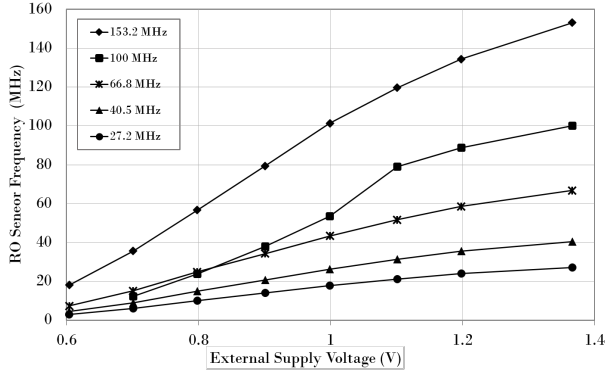


Fig. 10: PRO's oscillation frequency with Regard of External Power Supply Voltage

Figure 10 shows the result of the PRO oscillation frequency with regard to the external supply voltage. As shown in the figure, when the external supply voltage drops, the PRO's frequency drops steadily. The PRO's oscillation frequency reflects the power supply voltage, and therefore, it can sense the changes of the power supply and can be used for power monitoring. With respect to the sensitivity of power sensing, it can be observed that the higher the oscillation frequency is, the sharper the slope of the frequency vs. the external supply voltage line will be. This indicates that a higher oscillation frequency can achieve higher sensitivity in detecting power variations.

5.2 PRO Power Sensing with Regard to On-die Local Power Variations

After investigating the correspondence between the PRO sensor's oscillation frequency and the variations of external power variations, we evaluate the power sensing performance with regard to the on-die local power changing. Several previous works have shown that RO-based power wasters can cause a local power supply drop [34] [35] [5]. This will cause the local circuit's logic to operate at a lower voltage, therefore the local power sensor should show a decrease in the oscillation frequency when the power wasters are turned on. In this work, we adopt the RO-based power waster shown in Figure 11. Each power waster has five inverters in the delay chain with an AND gate and oscillates at 245MHz. A global enable signal is used to turn on/off all the power wasters in the circuit.

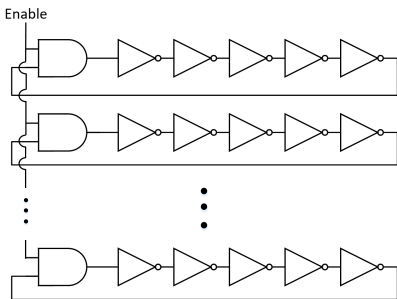


Fig. 11: The structure of the employed RO-based power wasters.

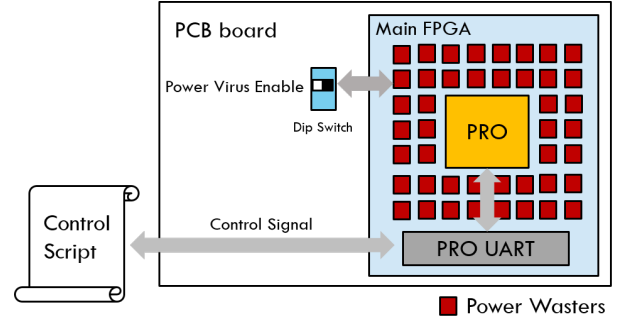


Fig. 12: Experimental Setup for PRO Power Sensing with Regard to On-die Local Power Variations

Figure 12 shows the experimental setup for the local power sensing evaluation. In this setup, UART communication is used to read out PRO's counter value. We constrain the power waster to locate around the PRO sensor to induce the local power drop around the sensor. By configuring the number of power wasters, we can control the amount of local power drop. An on-board dip switch is used to enable/disable the power wasters. In a measurement scenario, we gradually increase the number of power wasters. For each number of power waster configuration, we measure the PRO's oscillation frequency 1000 times and take the average with power waster on/off, respectively. Next, we calculate the Frequency Drop Ratio as follows:

$$\text{Frequency Drop Ratio} = \frac{f_{off} - f_{on}}{f_{off}} \quad (6)$$

In Equation 6, f_{off} denotes the PRO sensor's frequency when the power wasters are disabled (turned off) and f_{on} denotes its frequency when the power wasters are enabled (turned on). The results from the experiment are shown in Figure 13 when different numbers of power wasters are enabled. As more power wasters are enabled, the frequency drop ratio increases correspondingly. We can observe a nearly linear relationship between the number of power wasters and sensor oscillation slowdown. The linear regression which can closely model the correlation between the number of power wasters and the frequency drop ratio can be constructed as $f(x) = 0.00031x + 0.247$ with an R-squared value of 0.991. Therefore, we conclude that PRO can effectively sensing the local power variations as well.

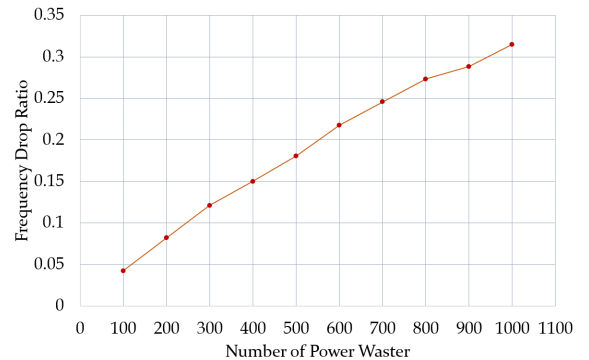


Fig. 13: PRO Frequency with Regard of Local Power Supply

5.3 PRO Power Sensing with Regard to Sensor Locality

In this experimental scenario, we evaluate the PRO sensor’s frequency change with respect to the spatial proximity to the switch logic that consumes the power. In this experiment, we instantiate 36 PRO sensors to get full spatial coverage of the FPGA. As shown in the floorplan in Figure 14 for this experimental scenario, 36 sensors residing in 9 rows, and each row has 4 sensors.

To remove the process variations among the PRO instances, we calculate the Frequency Drop Ratio for each PRO instance following Equation 6. We first measure the Frequency Drop Ratio for all the sensors. Then, we take the average of the frequency drop of the 4 PROs in each row. The results are shown in Figure 15. We observe that as the PRO sensors are placed closer to the power wasters (from Row 0 to Row 8), the Frequency Drop Ratio increases. Therefore, we can see the spatial distance of the PRO sensor to the switching logic (power wasters) indeed can be reflected in the Frequency Drop Ratio. We can further use this feature to detect the location of injected faults on the chip (will be demonstrated in Section 6). Note that there is an outlier in our designed sensor, which might be attributed to the power distribution network structure of the electronic circuits in which the power in the center of the chip is built to be more stable [36].

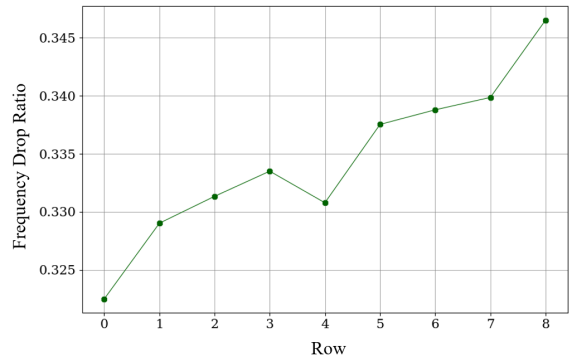


Fig. 15: PRO’s average Frequency Drop Ratio for each row versus the spatial proximity of the power wasters

We demonstrate that PRO can not only detect the occurrence of a power-based fault, but also the sensor array can detect the location of the power fault. This enables the designer (or the system administrator) to identify the source of the fault injection or the malicious circuits and build highly targeted fault response mechanisms accordingly. Moreover, We further demonstrate that PRO can be used for EM fault detection as well.

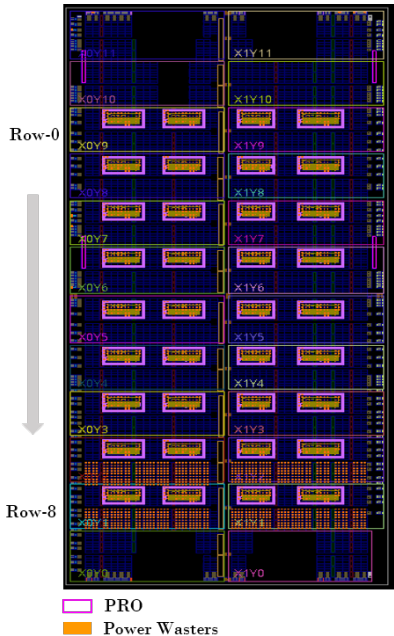


Fig. 14: FPGA Floorplan for Evaluating PRO Performance with Regard to Sensor Locality

6 FAULT DETECTION

In this section, we focus on evaluating our proposed on-die PRO sensor’s performance in sensing the occurrence of fault injection attacks. We show that PRO can be used to protect the circuit from adversaries who have physical access or remote control of the device [10] which enables them to inject power or EM faults. However, we assume that PRO itself is protected against the manipulation of the attacker.

6.1 Power Fault Detection

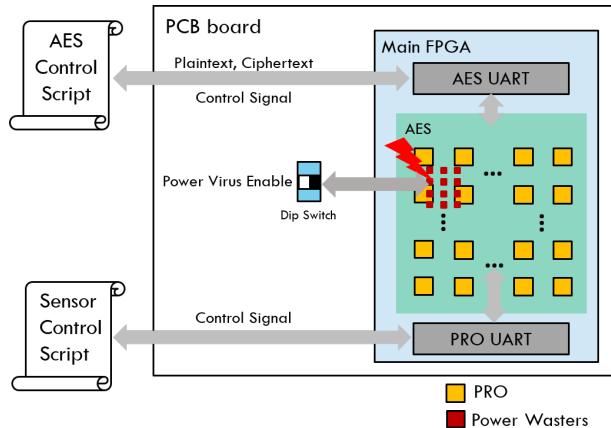


Fig. 16: Experimental Setup for PRO Power Fault Detection

Sharing the same PDN between a potential adversary and a victim opens the door to a new array of attacks. An adversarial logic can impose strong changes on the voltage level to cause timing faults in the victim circuit [11], [12], [13], [10]. Since all these attacks affect the PDN, we aim to build sensors that are sufficiently sensitive to the voltage level and therefore can detect such attacks. Detecting ongoing fault injection attacks will prevent resulting timing faults to go unnoticed.

Figure 16 shows our experimental setup for evaluating the power fault detection performance of our sensor. We instantiate AES as well as the PRO sensors array on the FPGA. Power wasters are placed locally on the chip to simulate the situation when local power faults are induced by an adversary. An on-board dip switch can control the turning on/off of the power wasters. AES control script is used to control starting the AES, send in plaintext, and

read out the ciphertext. The AES control script is also used to monitor the correctness of the resulting ciphertext. We adjust the number of power wasters instantiated while AES is running. When faulty ciphertexts are observed, we know that an effective power fault is successfully injected. This ensures that the power fault detected by PRO are actually effective faults. Next, we read out the PRO's counter value through the sensor's control script both when the fault is injected and not injected respectively, and compare their values. Note that as a chip-level sensor, our goal is to detect the location of the attacker instead of identifying the fault effect within the victim algorithm/circuit.

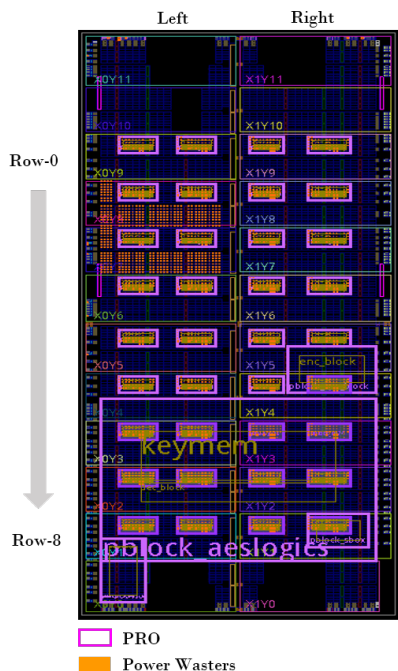


Fig. 17: FPGA floorplan for Evaluating PRO Performance in Power Fault Detection, power wasters simulate local power fault happens at location-1.

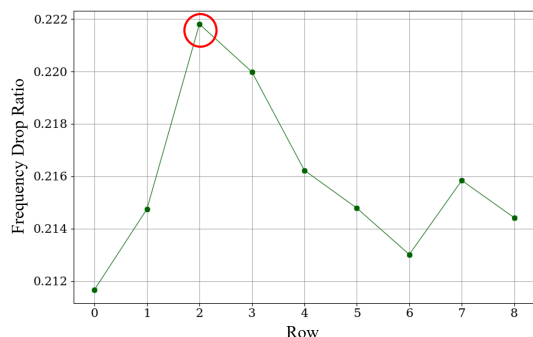


Fig. 18: PRO average frequency drop ratio for each row when power fault happens at location-1

Figure 17 shows the floorplan of the aforementioned setup. We placed 36 sensors on the chip and 524 power wasters are instantiated to generate power fault. We first put the power wasters at Row 1 and Row 2 on the left as shown in the orange blocks in Figure 17. While AES

is running, we read out the sensor's counter value when the faults are injected and not injected by power wasters respectively. Then we calculate the Frequency Drop Ratio based on Equation 6. With the PRO sensor data, we are able to find the location of the power fault. First, to locate which row has the power fault, we take the average of the 4 PRO sensors' frequency drop ratio in each row. Figure 18 shows the result of each row's average Frequency Drop Ratio. The maximum Frequency Drop Ratio points to a location adjacent to Row 2. This demonstrates that our sensor array can point to the correct row that the fault has occurred. Then, we divide the chip into two regions, left and right. To locate the fault region, we take the average of the Frequency Drop Ratios of the 18 sensors in the left and right two columns separately. The average Frequency Drop Ratio on the left region is 0.2184, and the average frequency drop for the right region is 0.213. The left region is higher than the right region, which indicates that the source of the fault is in the left region. This demonstrates that our sensor array can point to the correct fault column. Now, after analyzing the data of the sensor array, we can locate the power fault's location at Row 2, left region.

To further demonstrate the capability of the proposed PRO sensor in detecting the location of the fault, we placed the power wasters in different locations to inject fault while AES is running. We repeat the same experimental scenario to locate the faulty row and faulty column. We first put the power wasters in the location Row 4 and Row 5 on the left region and gets the result of locating the faulty row as demonstrated in Figure 19. The highest frequency drop ratio points to Row 4, which indicates that the fault happens adjacent to Row 4. By analyzing the faulty column, we see the left region's average frequency drop is 0.2159 and the right region's frequency drop is 0.2091 which indicates that the left region has the fault. Therefore, the sensor array locates the place where the fault is injected is at the left region Row 4 which meets our expectation. Next, we move the power wasters to another location at Row 1 and Row 2 on the right as shown in Figure 20. We observe the left region's average frequency drop is 0.2083 and the right region's frequency drop is 0.2204 which indicates that the right region has the fault. As shown in the result of analyzing the faulty row in Figure 19, the highest frequency drop ratio points to Row 2 correctly. Therefore, we demonstrate that our proposed sensor can detect the location of the on-chip power fault.

6.2 Electromagnetic Fault Injection (EMFI) Detection

EMFI is a well-known active attack and describes the use of an active probe to apply an intense and transient magnetic field to Integrated Circuits (ICs). EM pulse causes a sudden current flow in the circuit of the targeted IC and therefore, the local supply voltage drops. The voltage drop reflects in the form of power consumption peaks. This produces timing faults such as bit-flips, bit-sets, and bit-resets due to timing constraint violation and sampling faults by disrupting the switching process of D-Flip Flops if EM perturbations are synchronous with clock rising edges. This enables the adversary to exploit such faults to extract sensitive content from the device. Previous research has shown that EM perturbations can cause faulty computations, alter the

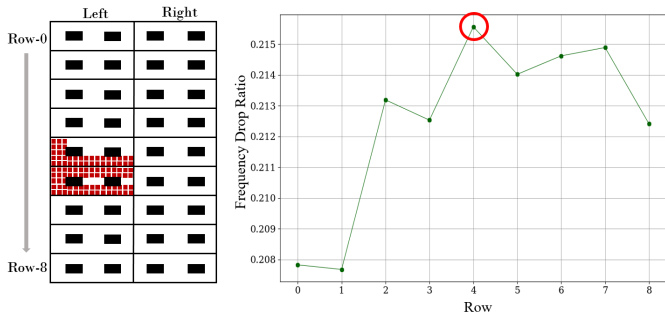


Fig. 19: Floorplan and corresponding PRO average frequency drop ratio for each row when power fault happens at location-2. Black blocks donate PROs in the floorplan, red blocks donate power wasters positions in the floorplan.

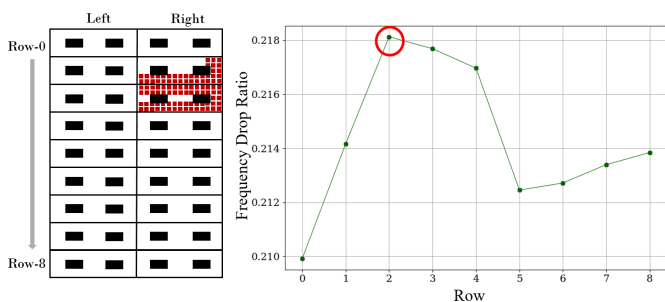


Fig. 20: Floorplan and the corresponding PRO average frequency drop ratio for each row when power fault happens at location-3. Black blocks denote PROs in the floorplan, red blocks denote power wasters positions in the floorplan.

program flow, and cause bit-flips in the contents of the memory. Other authors have demonstrated that EM can induce faults into the devices [37], [38]. In the past few years, EM fault injection attack has gained increasing attention. In this section, we investigate the performance of our proposed PRO sensor with regard to EM fault injection.

Figure 21 shows the experimental setup for evaluating the EM fault injection detection performance. In this setup, we instantiate AES and the PRO array with 36 sensors on the FPGA. AES control script is used to control the starting of the AES, send in the plaintext, and read out the ciphertext. While AES is running, the EM probe is placed in a fixed position on top of the FPGA chip surface with a vertical distance of approximately 1.5mm and generates an EM pulse to induce faults. The EM probe’s tip is 4mm in diameter and produces a magnetic field that is perpendicular to the surface of the chip. A glitch controller controls the time and intensity of the EM pulse. While AES is running, we adjust the intensity of the EM pulse. When a faulty ciphertext is observed, we know that an effective EM fault is injected. Next, in each measurement, we read out the PRO sensor’s counter value through the sensor’s control script when the fault is injected and not injected respectively, and compare their values.

We collect 1000 frequency measurements for all 36 PROs. For each PRO sensor, we investigate the distribution of the 1000 frequency measurements when the EM fault is injected and not injected. We observe that the EM fault can cause variations of the PRO’s frequency distribution. Figure 22

shows comparisons of the frequency distribution when the EM fault is injected and not injected for RO-0 to RO-15. We notice that the PRO sensor’s frequency shifts to a larger value when faults are injected. We also observe that besides frequency shifting, there is another fault injection reaction that the PRO sensors can have. We observe that EM faults can also cause faulty counter value for RO-23 to RO-27 and RO-31 to RO-36. When the faults are injected, the counter values are read out by the UART jump to an extremely huge (and faulty) value of 4.08×10^7 MHz. Therefore, by monitoring the value of the PRO counters, we can detect ongoing Electromagnetic Fault Injection (EMFI) at run-time.

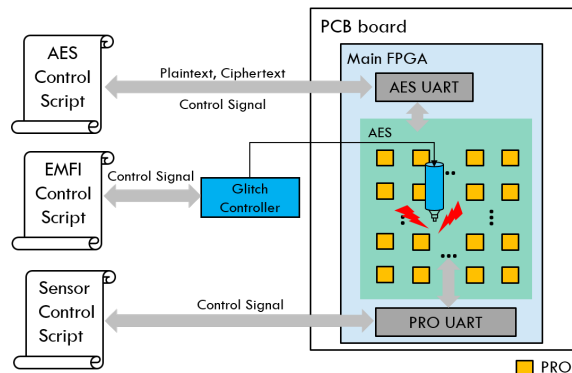


Fig. 21: Experimental Setup for PRO EM Fault Detection

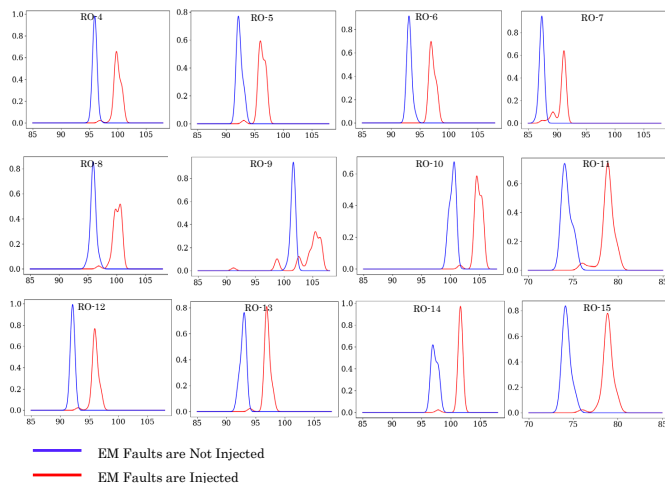


Fig. 22: Influence on the Frequency Distribution, X-axis is probability and Y-axis is frequency.

7 CONCLUSION

In this work, we proposed a multi-purpose Ring Oscillator design. We demonstrated that it is possible, with a low cost, to have a side-channel countermeasure and fault detection mechanism within the same design. We showed that PRO can provide an effective hiding countermeasure to the circuit with low overhead by injecting random frequency noise. We further demonstrated that the PRO array can form a comprehensive on-chip secure monitoring network. The network can potentially provide both temporal and spatial coverage of on-chip power monitoring and fault

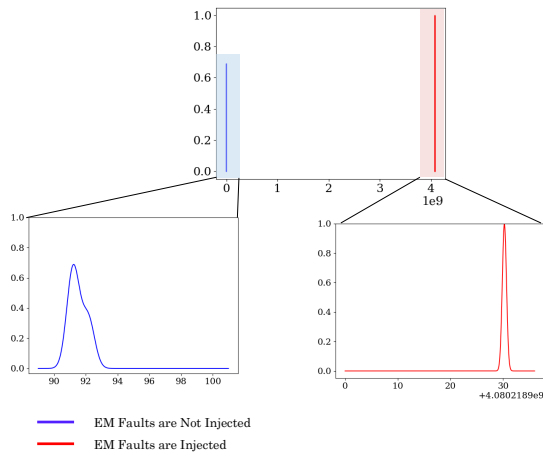


Fig. 23: Influence on the Frequency Distribution for PRO-32 detection. PRO has the flexibility for the user to communicate and control its configurations, such as its oscillation frequency, in real-time. This feature highlights its potential to be integrated into large designs, such as SoCs, as a secure extension to build more comprehensive side-channel and fault-resistant systems. As the future work, we will further investigate integrating PRO into an SoC and build up a real-time side-channel countermeasure and fault detection/response system that can protect both software and hardware applications.

REFERENCES

- [1] Hagai Bar-El, Hamid Choukri, David Naccache, Michael Tunstall, and Claire Whelan, "The sorcerer's apprentice guide to fault attacks", *Proceedings of the IEEE*, vol. 94, no. 2, pp. 370–382, 2006.
- [2] Yuan Yao, Mo Yang, Conor Patrick, Bilgiday Yuce, and Patrick Schaumont, "Fault-assisted side-channel analysis of masked implementations", in *2018 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*. IEEE, 2018, pp. 57–64.
- [3] Shahin Tajik, Julian Fietkau, Heiko Lohrke, Jean-Pierre Seifert, and Christian Boit, "Pufmon: Security monitoring of fpgas using physically unclonable functions", in *2017 IEEE 23rd International Symposium on On-Line Testing and Robust System Design (IOLTS)*. IEEE, 2017, pp. 186–191.
- [4] Chan-Kyung Kim, Bai-Sun Kong, Chil-Gee Lee, and Young-Hyun Jun, "Cmos temperature sensor with ring oscillator for mobile dram self-refresh control", in *2008 IEEE International Symposium on Circuits and Systems*. IEEE, 2008, pp. 3094–3097.
- [5] Mark Zhao and G Edward Suh, "Fpga-based remote power side-channel attacks", in *2018 IEEE Symposium on Security and Privacy (SP)*. IEEE, 2018, pp. 229–244.
- [6] O-X Standaert, Eric Peeters, Gaël Rouvroy, and J-J Quisquater, "An overview of power analysis attacks against field programmable gate arrays", *Proceedings of the IEEE*, vol. 94, no. 2, pp. 383–394, 2006.
- [7] Stefan Mangard, Elisabeth Oswald, and Thomas Popp, *Power analysis attacks: Revealing the secrets of smart cards*, vol. 31, Springer Science & Business Media, 2008.
- [8] P. Kocher, "Timing attacks on implementations of Diffie-Hellman, RSA, DSS, and other systems", in *CRYPTO '96*, N. Koblitz, Ed. 1996, vol. 1109 of LNCS, pp. 104–113, Springer.
- [9] Eric Brier, Christophe Clavier, and Francis Olivier, "Correlation power analysis with a leakage model", in *International workshop on cryptographic hardware and embedded systems*. Springer, 2004, pp. 16–29.
- [10] Dina Mahmoud and Mirjana Stojilović, "Timing violation induced faults in multi-tenant fpgas", in *2019 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2019, pp. 1745–1750.
- [11] Jonas Krautter, Dennis RE Gnad, and Mehdi B Tahoori, "Fpga-hammer: Remote voltage fault attacks on shared fpgas, suitable for dfa on aes", *IACR Transactions on Cryptographic Hardware and Embedded Systems*, pp. 44–68, 2018.
- [12] George Provelengios, Daniel Holcomb, and Russell Tessier, "Power distribution attacks in multitenant fpgas", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 12, pp. 2685–2698, 2020.
- [13] Md Mahbub Alam, Shahin Tajik, Fatemeh Ganji, Mark Tehranipoor, and Domenic Forte, "Ram-jam: Remote temperature and voltage fault attack on fpgas using memory collisions", in *2019 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC)*, 2019, pp. 48–55.
- [14] Eli Biham and Adi Shamir, "Differential fault analysis of secret key cryptosystems", in *Annual international cryptology conference*. Springer, 1997, pp. 513–525.
- [15] Thomas Fuhr, Eliane Jaulmes, Victor Lomné, and Adrian Thillard, "Fault attacks on aes with faulty ciphertexts only", in *2013 Workshop on Fault Diagnosis and Tolerance in Cryptography*. IEEE, 2013, pp. 108–118.
- [16] Yuan Yao and Patrick Schaumont, "A low-cost function call protection mechanism against instruction skip fault attacks", in *Proceedings of the 2018 Workshop on Attacks and Solutions in Hardware Security*, 2018, pp. 55–64.
- [17] Po-Chun Liu, Hsie-Chia Chang, and Chen-Yi Lee, "A low overhead dpa countermeasure circuit based on ring oscillators", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 7, pp. 546–550, 2010.
- [18] Jonas Krautter, Dennis R.E. Gnad, Falk Schellenberg, Amir Moradi, and Mehdi B. Tahoori, "Active fences against voltage-based side channels in multi-tenant fpgas", in *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2019, pp. 1–8.
- [19] Kenneth M Zick and John P Hayes, "Low-cost sensing with ring oscillator arrays for healthier reconfigurable systems", *ACM Transactions on Reconfigurable Technology and Systems (TRETs)*, vol. 5, no. 1, pp. 1–26, 2012.
- [20] Dennis R.E. Gnad, Fabian Oboril, Saman Kiamehr, and Mehdi B. Tahoori, "Analysis of transient voltage fluctuations in fpgas", in *2016 International Conference on Field-Programmable Technology (FPT)*, 2016, pp. 12–19.
- [21] Md Toufiq Hasan Anik, Mohammad Ebrahimabadi, Hamed Pirsivash, Jean-Luc Danger, Sylvain Guilley, and Naghmeh Karimi, "On-chip voltage and temperature digital sensor for security, reliability, and portability", in *2020 IEEE 38th International Conference on Computer Design (ICCD)*. IEEE, 2020, pp. 506–509.
- [22] Joseph Gravelier, Jean-Max Dutertre, Yannick Teglia, and Philippe Loubet-Moundi, "High-speed ring oscillator based sensors for remote side-channel attacks on fpgas", in *2019 International Conference on ReConfigurable Computing and FPGAs (ReConFig)*, 2019, pp. 1–8.
- [23] Noriyuki Miura, Zakaria Najm, Wei He, Shivam Bhasin, Xuan Thuy Ngo, Makoto Nagata, and Jean-Luc Danger, "Pll to the rescue: A novel em fault countermeasure", in *2016 53rd ACM/EDAC/IEEE Design Automation Conference (DAC)*, 2016, pp. 1–6.
- [24] Wei He, Jakub Breier, Shivam Bhasin, Noriyuki Miura, and Makoto Nagata, "Ring oscillator under laser: potential of pll-based countermeasure against laser fault injection", in *2016 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC)*. IEEE, 2016, pp. 102–113.
- [25] Xuehui Zhang and Mohammad Tehranipoor, "Ron: An on-chip ring oscillator network for hardware trojan detection", in *2011 Design, Automation & Test in Europe*. IEEE, 2011, pp. 1–6.
- [26] Stefan Tillich and Christoph Herbst, "Attacking state-of-the-art software countermeasures—a case study for aes", in *International Workshop on Cryptographic Hardware and Embedded Systems*. Springer, 2008, pp. 228–243.
- [27] Jean-Sébastien Coron and Ilya Kizhvatov, "Analysis and improvement of the random delay countermeasure of ches 2009", in *International Workshop on Cryptographic Hardware and Embedded Systems*. Springer, 2010, pp. 95–109.
- [28] Debayan Das, Shovan Maity, Saad Bin Nasir, Santosh Ghosh, Arijit Raychowdhury, and Shreyas Sen, "High efficiency power side-channel attack immunity using noise injection in attenuated signature domain", in *2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*. IEEE, 2017, pp. 62–67.
- [29] Po-Chun Liu, Hsie-Chia Chang, and Chen-Yi Lee, "A low overhead dpa countermeasure circuit based on ring oscillators", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 7, pp. 546–550, 2010.

- [30] Jonas Krautter, Dennis Gnad, and Mehdi Tahoori, "Cpamap: On the complexity of secure fpga virtualization, multi-tenancy, and physical design", *IACR Transactions on Cryptographic Hardware and Embedded Systems*, pp. 121–146, 2020.
- [31] Chong Hee Kim and Jean-Jacques Quisquater, "Faults, injection methods, and fault attacks", *IEEE Design & Test of Computers*, vol. 24, no. 6, pp. 544–545, 2007.
- [32] Dmitry Utyamishv and Inna Partin-Vaisband, "Real-time detection of power analysis attacks by machine learning of power supply variations on-chip", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 1, pp. 45–55, 2018.
- [33] Benjamin Jun Gilbert Goodwill, Josh Jaffe, Pankaj Rohatgi, et al., "A testing methodology for side-channel resistance validation", in *NIST non-invasive attack testing workshop*, 2011, vol. 7, pp. 115–136.
- [34] Shayan Moini, Xiang Li, Peter Stanwicks, George Provelengios, Wayne Burleson, Russell Tessier, and Daniel Holcomb, "Understanding and comparing the capabilities of on-chip voltage sensors against remote power attacks on fpgas", in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2020, pp. 941–944.
- [35] George Provelengios, Daniel Holcomb, and Russell Tessier, "Characterizing power distribution attacks in multi-user fpga environments", in *2019 29th International Conference on Field Programmable Logic and Applications (FPL)*. IEEE, 2019, pp. 194–201.
- [36] Mikhail Popovich, Andrey Mezhiba, and Eby G Friedman, *Power distribution networks with on-chip decoupling capacitors*, Springer Science & Business Media, 2007.
- [37] Marjan Ghodrati, Bilgiday Yuce, Surabhi Gujar, Chinmay Deshpande, Leyla Nazhandali, and Patrick Schaumont, "Inducing local timing fault through em injection", in *2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC)*, 2018, pp. 1–6.
- [38] F. Poucheret, K. Tobich, M. Lisarty, L. Chusseauz, B. Robissonx, and P. Maurine, "Local and direct em injection of power into cmos integrated circuits", in *2011 Workshop on Fault Diagnosis and Tolerance in Cryptography*, 2011, pp. 100–104.

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