Study of the MMC Circulating Current for Optimal Operation Mode in HVDC Applications

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Abstract

An exhaustive study on the circulating currents and their consequences in modular multilevel converters for HVDC applications is presented. The first part is a review of an analytical study of the converter, aimed to minimize the capacitors voltage ripple. In the second part the effects on the system efficiency are presented.

Introduction

Modular Multilevel Converter (M^2C), whose schematic representation is shown in Fig. 1, is today the standard voltage source converter in HVDC applications [1,2,3]. The reason is the simplicity in increasing the total DC link voltage V_{DC}, obtained only by increasing the number of its cells.

Typically, the number of cells in HVDC applications is very high, with V_{DC} higher than 100kV and good harmonic content in the AC side, minimizing the AC filter and in many cases eliminating the need of it.

In HVDC applications, maximizing efficiency and also minimizing capacitors voltage V_{cap} ripple is of main importance.

In the first part, this work reviews the analytical results of [4] indicating the influence of the circulating currents on the capacitor voltage ripple, and consequently gives the conditions minimizing the voltage ripple.

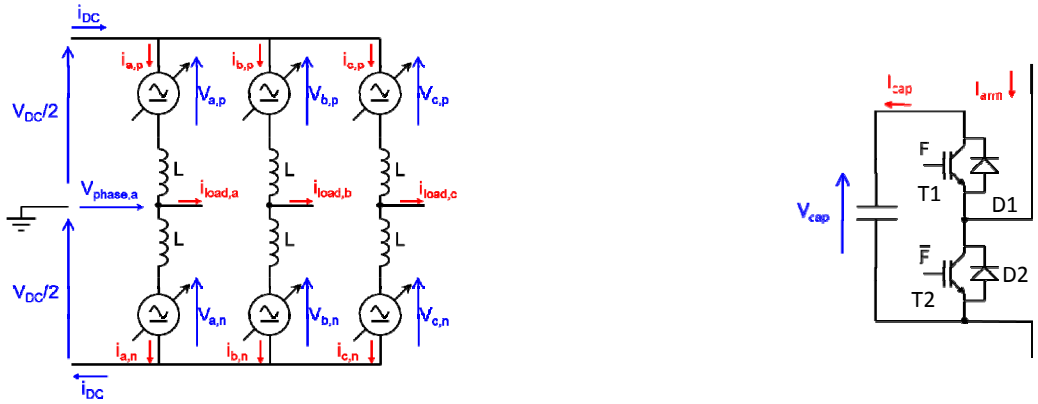

Fig. 1: Right: MMC voltages and currents definitions - Left: MMC cell, electrical scheme

In the second part, the conditions minimizing the voltage ripple, that, as shown in the next sections, increase the current flowing across the cells, are studied. The authors have verified how the current increment doesn't mean always an increase of the semiconductor losses, but implies a redistribution of the losses among the four devices, also decreasing the losses of the cell in some cases studied in the inverter and rectifier working modes.

Converter Analysis

Considering the converter, as shown in Fig. 1, having n cells per phase, the DC link voltage V_{DC} is given by (1), where V_{cap} is the capacitor voltage. In HVDC applications, in steady-state operations, the output voltage V_{phase} is close to a sinusoidal waveform as given by (2), where m is the modulation index. In general, it is possible to add a common mode voltage like the third order harmonic component, but the authors have shown previously [5] how this term has a minimal influence and so it is not considered in this paper.

$$V_{DC} = \frac{1}{2} n V_{cap} \tag{1}$$

$$V_{phase} = \frac{\mathrm{m}}{2} V_{DC} \sin(\omega t) + \sum_{k=1}^{\infty} v_{cm,k} \sin(k\omega t) \tag{2}$$

The load current, in steady-state conditions, can be considered sinusoidal (3), with amplitude i_l and power factor $cos\phi$:

$$i_{load} = i_l \sin(\omega t + \phi) \tag{3}$$

The converter is modulated with a PWM technique and the analytical analysis is carried out with the approximation of a high switching frequency, i.e., using the average model. The results obtained have been also verified with simulations where devices switch at low frequencies, equal to about 150 Hz, confirming the validity of the proposed approach.
In these conditions the output voltage of the converter is given by (4):

$$V_{phase} = \frac{m}{2} V_{DC} \sin(\omega t) \tag{4}$$

In [4] the authors have analyzed the system considering the first terms of the Taylor expansion for the leg currents $i_{leg,p(n)}$, as shown in (5) and (6); then, they have found the working conditions that minimize the capacitor energy ripple,

$$i_{leg,p}(t) = \sum_{k=-\infty}^{+\infty} \gamma_k e^{ik\omega t} \cong$$
$$i_l \left\{ \frac{1}{4} m \cos\phi + \frac{1}{2} \sin(\omega t + \phi) + i_2 \sin\left(2\omega t + \phi_2 + \phi - \frac{\pi}{2}\right) + i_4 \sin\left(4\omega t + \phi + \phi_2 + \phi_4 - \frac{\pi}{2}\right) \right\} \tag{5}$$

$$i_{leg,n}(t) = \sum_{k=-\infty}^{+\infty} \gamma_k e^{ik\omega t} \cong$$
$$i_l \left\{ \frac{1}{4} m \cos\phi - \frac{1}{2} \sin(\omega t + \phi) + i_2 \sin\left(2\omega t + \phi_2 + \phi - \frac{\pi}{2}\right) + i_4 \sin\left(4\omega t + \phi + \phi_2 + \phi_4 - \frac{\pi}{2}\right) \right\} \tag{6}$$

and consequently the cell capacitors voltage ripple. The optimal values are those with the terms given by (7), (8) and (9):

$$\phi_4 \to 0, i_4 \to \frac{100}{136 + \frac{225}{m^2}} i_2 \tag{7}$$

$$\phi_2 \to sin\,\phi_2 = \frac{1}{\left(\frac{5}{m^2} - 1\right)}\ sin(\phi_2 + 2\phi) \tag{8}$$

$$i_2 \to \frac{m}{900 + 1544m^2 + 560m^4} \{225 + 136m^2\} [(5 - m^2)\cos\phi_2 - m^2 \cos(2\phi + \phi_2)] \tag{9}$$

The optimal values of magnitude and phase for the second harmonic circulating current are depicted in Fig. 2.

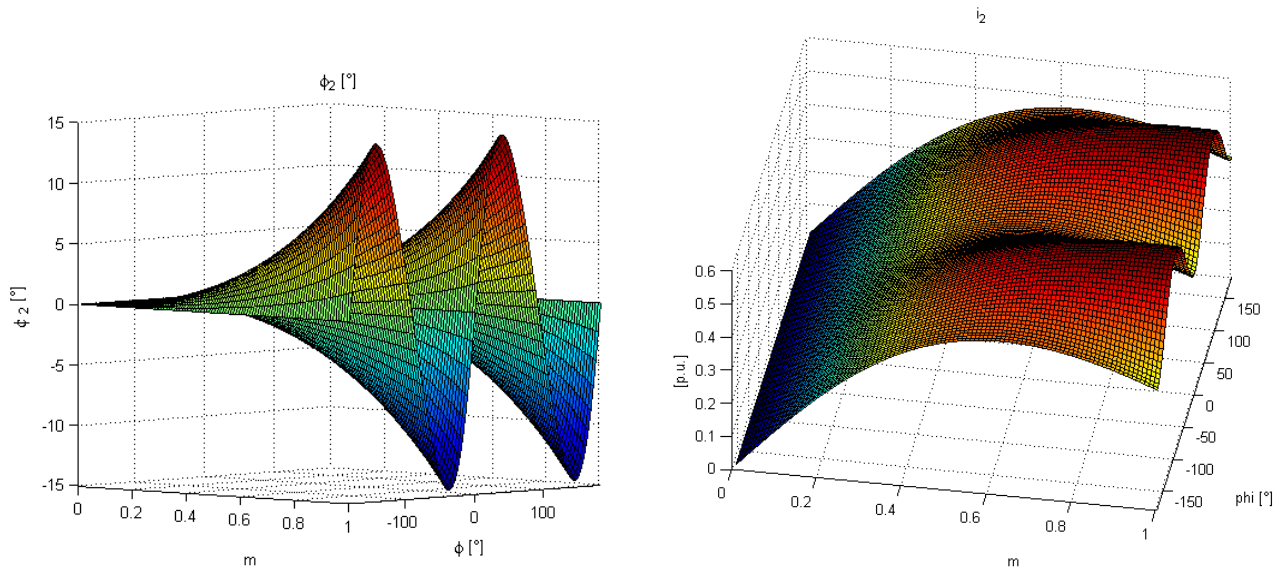

Fig. 2: Right: Optimal ϕ_2 as function of ϕ and m - Left: Optimal i_2 as function of ϕ and m

$$i_{circ} = \frac{1}{2}(i_{leg,p} + i_{leg,n}) \tag{10}$$

Let us define the circulating current as in (10); then, the capacitor energy ripple with only DC circulating current, i.e., in conventional working conditions, is shown in Fig. 3, as a function of the modulation index m and of the displacement phase angle ϕ. It can be appreciated how the maximum ripple is for low modulation index amplitudes, and for STATCOM working modes, i.e., $cos\phi = 0$. In Fig. 4 the ripple improvements, obtained with the injection of optimal 2^{nd} and 4^{th} harmonics and with only optimal 2^{nd} harmonic, are shown. It's interesting to note that the improvement due to the 4^{th} harmonic is very small, so in the next sections, only the second harmonic will be considered.

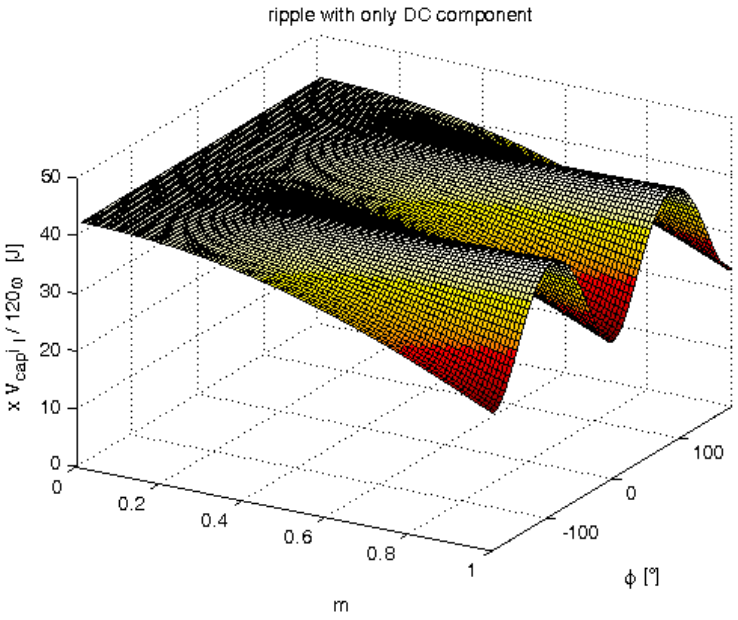

Fig. 3: Capacitor energy ripple with only DC circulating current

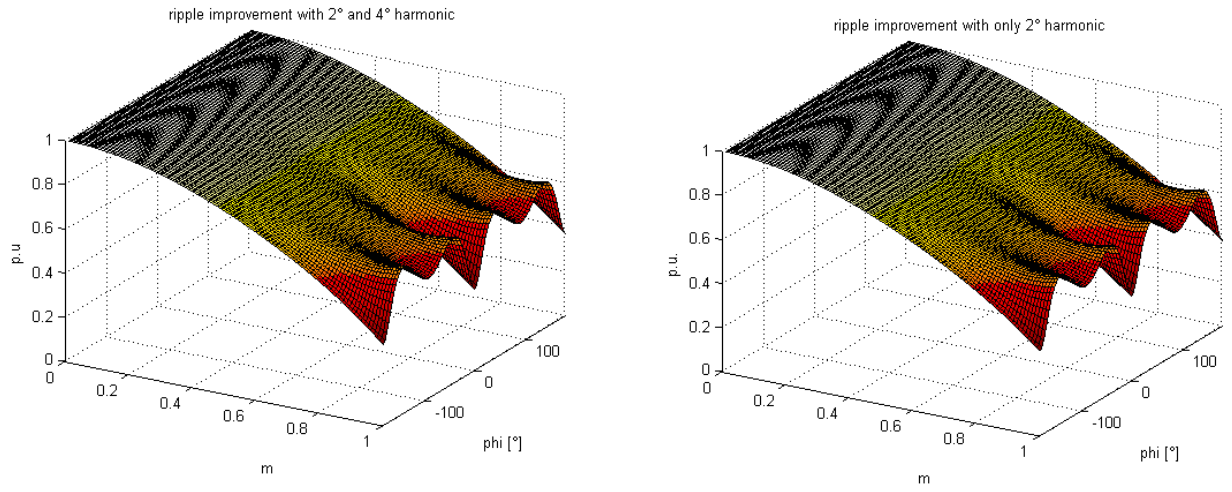

Fig. 4: Left: Capacitor energy ripple with 2^{nd} and 4^{th} optimal harmonic leg current - Right: Capacitor energy ripple with only 2^{nd} optimal harmonic leg current

Losses Analysis

In [5] the authors have presented some simulations of the converter with the addition of second order harmonic circulating current, finding how, in some conditions, the losses decrement when the current leg increments. In this section, these results are shown with greater detail, showing how this circumstance seems to be a general result, in particular studying two different cases, the first with power semiconductors having silicon buffers of 85 mm and I_{DC} equal to 1500 A, corresponding to a real plant and the second with 125 mm and I_{DC} equal to 3000 A, corresponding to a realistic plant.
In real plants, the modulation used can be either a low frequency asynchronous PWM or a staircase one. However, in order to show more clearly the mechanisms involved, the following results refer to simulations where a synchronous low frequency PWM is adopted. If a PWM is used in real plants, usually it is an asynchronous one, in order to equally share the power losses among all the cells; in fact, in this case, the switching instants are always different, thanks to the lack of synchronism. The synchronous modulation guarantees identical switching timing of all the semiconductor devices of each cell of the converter in all electrical cycles. The result will be the lack of an equal sharing in power losses among the cells of the converter, but synchronous modulation makes easier the understanding of the power losses variations seeing the currents waveforms of the cells. The correct sharing can be simulated, calculating the mean power losses of the converter, that correspond approximately to those that would be obtained with the asynchronous modulation. The modulation frequency used is 200 Hz with an output voltage frequency of 50 Hz.
In [5] the authors have shown how the injection of a second order harmonic circulating current in the STATCOM working modes increases always the losses of the converter, whereas in the inverter and rectifier working modes it can decrease them. For this reason, in the following study the attention is focused on the inverter and rectifier working modes.
The first case under study is the one indicated in Table I, with 85 mm diameter semiconductors in inverter working mode: *IEGT S6X06B* from Toshiba and diode *D1331SH* from Eupec.

Table I: First simulated MMC converter main ratings and parameters

Name	Value	Description
A	480 MVA	Nominal power of the AC grid
P_{DC}	480 MW	Nominal DC power
I_{DC}	1500 A	DC Link current
N	128	Number of sub-modules per arm
$f_{SW,cell}$	200Hz	Switching frequency of each sub-module
L	15mH	Arm inductance
C	7.2mF	Capacitance of each sub-module capacitor bank
V_{AC}	164 kV	AC voltage at the converter side of the transformer
V_{DC}	±160 kV	Total DC voltage (negative to positive pole)
Working Mode		Inverter mode, m = 0.85

The optimal value of the 2^{nd} harmonic circulating current injection, for the capacitor voltage ripple minimization, in this configuration is equal to $0.4248 i_l$, with a maximum capacitor voltage variation of 270V; unfortunately, in this case, the total losses of the converter increase and consequently this configuration is discarded; instead, with an injection of a 2^{nd} harmonic equal to $0.20 i_l$, the converter losses decrease and the maximum voltage variation becomes 305V, which is not the minimum possible but always lower than 402V, that is the value obtained without any harmonics injection and with greater converter losses.
In order to understand how an increase in the current leg, i.e., in the cell and consequently in the semiconductors devices leads to a decrease in the cell losses, the next figures show the total losses of the cells and the losses of each device of the cells in the synchronous case (solid lines) and in the asynchronous case (dashed lines). In Fig. 5, the left figure shows how the cell losses are mainly lower with the harmonic injection.
The analysis of all the devices losses states how all devices but T2 decrease their losses, so the current is redistributed among the four devices of the cell, and it concentrates in the lower IEGT T2. In Fig. 6 it's possible to appreciate the currents in all the devices and to verify how T2 (red current) is the device more stressed and has greater conduction losses in every condition (cell); however, the injection of the 2^{nd} harmonic not only increases the leg current but concentrates it in a smaller time interval, so in many cases the switching losses are smaller with the harmonic injection than without any injection.

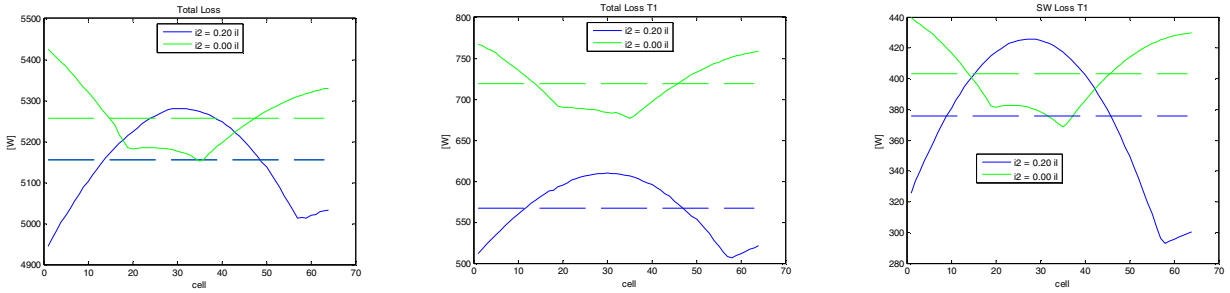

Fig. 5: Losses in each cell in four cases: modulation with only DC circulating current (green), with 2^{nd} harmonic injection (blue), asynchronous modulation (solid) and asynchronus (dashed) - Left: Total losses – Center: Total losses of upper IEGT T1 – Right: Switching losses of T1

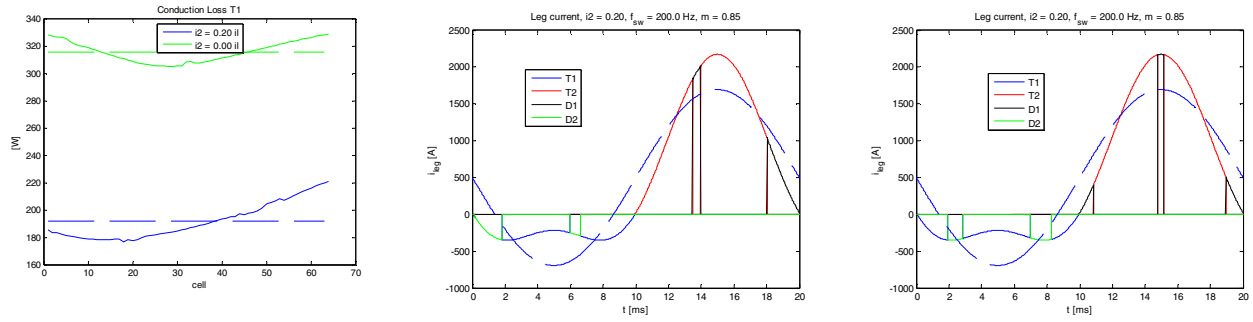

Fig. 6: Left: T1 Conduction losses - Center: Leg current flowing throw T1 (blue), T2 (red), D1(black), D2 (green) with 2^{nd} harmonic injection; in dashed blue the leg current with only DC circulating current, in the first cell - Left: Same quantities of center panel in cell n. 32

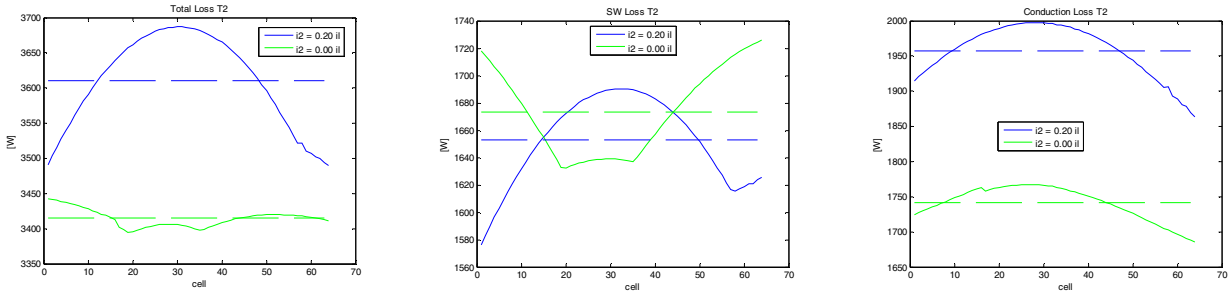

Fig. 7: Left: Total losses in T2 – Center: Switching losses in T2 – Right: Conduction losses in T2

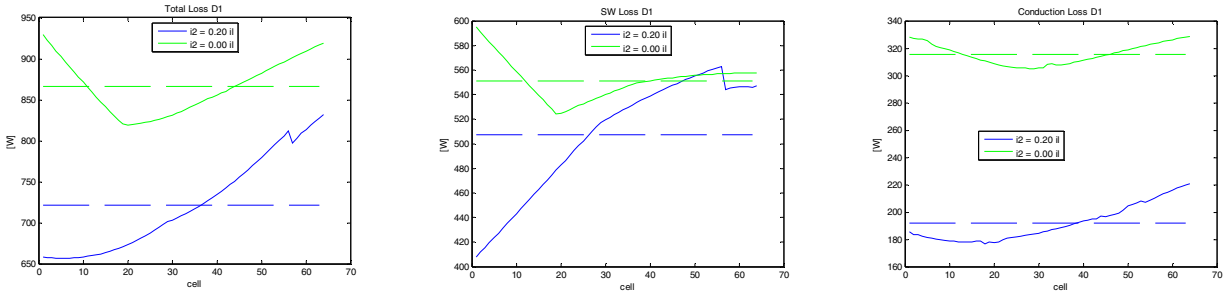

Fig. 8: Left: Total losses in D1 – Center: Switching losses in D1 – Right: Conduction losses in D1

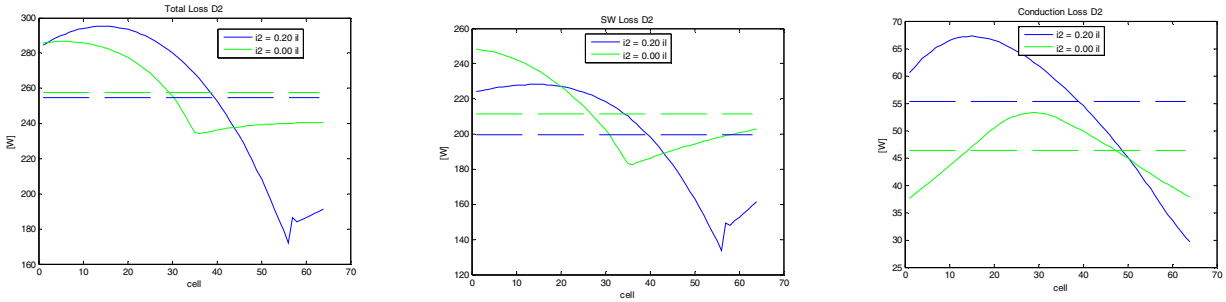

Fig. 9: Left: Total losses in D2 – Center: Switching losses in D2 – Right: Conduction losses in D2

Similar results have been obtained with a DC link current equal to 3000 A, with 125 mm diameter power semiconductors, IEGT ST2100 from Toshiba and diode D1821SH from Infineon. The results related to the asynchronous case are shown in Table II for the 85 mm devices and in Table III for the 125 mm devices. It can be appreciated the improvement (improv. in the Tables) in efficiency for each device of the cell considering the conduction losses (CL), the switching losses (SWL) and the total losses (TL) with the second harmonic circulating current i_2 injection. The results summarized in Table II and III show that the efficiency improvements in the inverter mode are obtained with both couples of semiconductors and are both low and depend on the semiconductor type, with variations of about 30% between the two types; in any case the cell losses improvements are always lower than 3%. Results show how the greater variations from the losses point of view are observed for T1, T2 and D1. The devices T1 and D1 show improvements for the conduction and switching losses, whereas in T2 and D2 the conduction losses are incremented and the switching ones are decremented. Unfortunately, in the inverter mode the more stressed device is T2 and, only for T2, the increment in the conduction losses is not compensated by the decrement in switching losses, as it can be observed for D2, the device with the lower stress. The last column of Table II and III shows the total absolute improvement related to each device and it's possible to appreciate how the greater variation refers to the most stressed device, i.e., to T2, and corresponds to an increment in the losses. This negative variation is compensated by the decrement of the losses in the two devices T1 and D1. The global losses variation of the cell is a decrement of the losses, which is lower than the decrement related to T1 or D1 and lower than 3% for the two couples of semiconductor studied.

In order to understand the mechanism involved in the losses devices sharing of the cell with the current second harmonic, it's important to analyse the behaviour of the three main components involved in the losses: T1, T2 and D1. In the central panel of Fig. 6, the current of the cell is shown in the better case, where the losses are lower with the injection of the second harmonic, as shown in the left panel of Fig. 5, corresponding to the first cell.

The main component involved in the losses is T2. From the conduction point of view, the current is incremented significantly, but the conducting time is slightly decremented, so the conduction losses are slightly increased, as shown in Table II and III. From the switching point of view, in the first cell, the first turn-off and turn-on switch higher currents with the second harmonic, but there is a compensation with the second turn-off, which switches lower current, and the second turn-on (not shown in the figure) which is present only without the second harmonic, thanks to the reduced conducting time, so in this cell the switching losses are reduced. In the cell n. 32 there are more switching events; considering for instance the switching event at t = 15ms, the increment of switched current is higher with respect to the first cell, so the switching losses for the cell n. 32 are worse with the second harmonic current. The central panel of Fig. 7

shows how, in average, the switching losses related to T2 are slightly lower with the second harmonic current.
It's important to note how the incremented losses of the more stressed device of the cell, T2, have a negative effect on the whole system: the current limit of the system is given by the maximum allowable junction temperature, so incrementing the losses of the more stressed device means that the thermic margin of the system is decremented. The simulations show how, with the asynchronous modulation, the maximum junction temperature is increased by about 2°C, considering a cooling system with water at 40°C, value that can be considered acceptable in the system considered, but in general this limit needs always to be taken into account.

Table II: Improvement in semiconductor losses with second harmonic circulating current i_2 injection with medium I_{dc} (Inverter mode - 85 mm diameter power semiconductors)

I_{dc} 1500A									
i_2	0			0.20					
	CL[W]	SWL[W]	TL[W]	CL[W]	improv.	SWL[W]	improv.	TL[W]	improv.
T1	316	404		189	40.2%	373	7.7%		158W
T2	1746	1666		1961	-2.3%	1639	1.6%		-188W
D1	315	542		219	30.5%	499	7.9%		139W
D2	46	210		54	-7.4%	193	8.1%		9W
Σ	2422	2821	5243	2423	0.0%	2705	4.1%	5128	2.2%

Table III: Improvement in semiconductor losses with second harmonic circulating current i_2 injection with high I_{dc} (Inverter mode - 125 mm diameter power semiconductors)

I_{dc} 3000A									
i_2	0			0.20					
	CL[W]	SWL[W]	TL[W]	CL[W]	improv.	SWL[W]	improv.	TL[W]	improv.
T1	618	797		370	40.1%	747	6.3%		298W
T2	3491	3353		3949	-13.1%	3315	1.1%		-420W
D1	843	869		580	31.2%	866	0.3%		266W
D2	122	227		140	-14.8%	187	17.6%		22W
Σ	5074	5246	10320	5039	0.7%	5115	2.5%	10154	1.6%

The second case under study is the one indicated in Table IV, with 125 mm diameter semiconductors, IEGT ST2100 from Toshiba and diode D1821SH from Infineon, working in rectifier mode.

Table IV: Second simulated MMC converter main ratings and parameters.

Name	Value	Description
A	960 MVA	Nominal power of the AC grid
P_{DC}	960 MW	Nominal DC power
I_{DC}	3000 A	DC Link current
N	128	Number of sub-modules per arm
$f_{SW,cell}$	200Hz	Switching frequency of each sub-module
L	15mH	Arm inductance
C	7.2mF	Capacitance of each sub-module capacitor bank
V_{AC}	164 kV	AC voltage at the converter side of the transformer
V_{DC}	±160 kV	Total DC voltage (negative to positive pole)
Working Mode		Rectifier mode, m = 0.85

The optimal value for the 2^{nd} harmonic circulating current injection, for the capacitor voltage ripple minimization, in this configuration is always $0.4248 i_l$, with a maximum capacitor voltage variation of 540V; unfortunately, the total losses of the converter increase as in the inverter mode and consequently this configuration is discarded; instead, with an injection of a 2^{nd} harmonic equal to $0.20 i_l$, the converter losses decrease and the maximum voltage variation becomes 610V, which is not the minimum possible, but it is always lower than 804V, that is the value obtained without any harmonics injection and with greater converter losses.

As in the inverter mode, in order to understand how an increase in the current leg, i.e., in the cell and consequently in the semiconductors devices leads to a decrease in the cell losses, the next figures show the total losses of the cells and the losses of each device of the cells in the synchronous case (solid lines) and in the asynchronous case (dashed lines). In Fig. 10, the left figure shows how the cell losses are mainly lower with the harmonic injection.

The analysis of all the devices losses states how all devices but D2 decreases their losses, so the current is redistributed among the four devices of the cell, and it concentrates in the lower diode D2. In Fig. 11 it's possible to appreciate the currents in all the devices and verify how D2 (green current) is the device more stressed and has a greater conduction losses in every condition (cell); however, the injection of the 2^{nd} harmonic not only increases the leg current but concentrates it in a smaller time interval, so in many cases the switching losses are smaller with the harmonic injection than without any injection.

Similar results have been obtained with a DC link current of 1500 A, with 85 mm diameter power semiconductors, IEGT S6X06B from Toshiba and diode D1331SH from Eupec. The results related to the asynchronous case are shown in table V, for the 85 mm devices and in Table VI for the 125 mm devices.

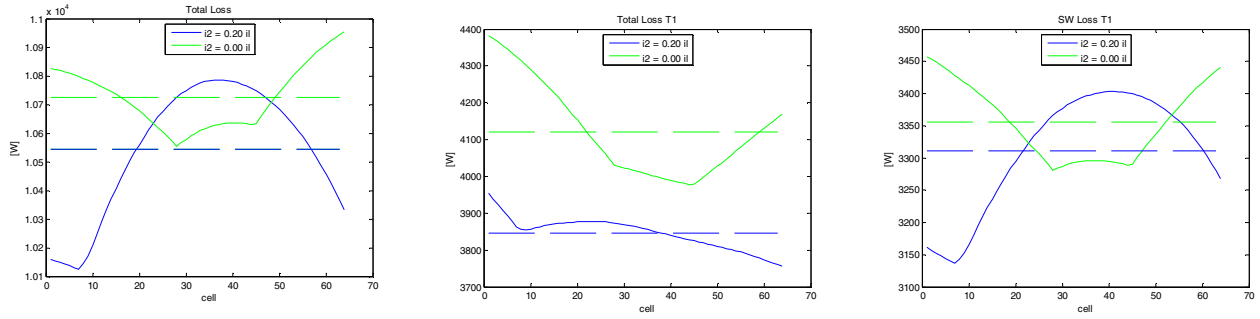

Fig. 10: Losses in each cell in four cases: modulation with only DC circulating current (green), with 2^{nd} harmonic injection (blue), asynchronous modulation (solid) and asynchronus (dashed) - Left: Total losses – Center: Total losses of upper IEGT T1 – Right: Switching losses of T1

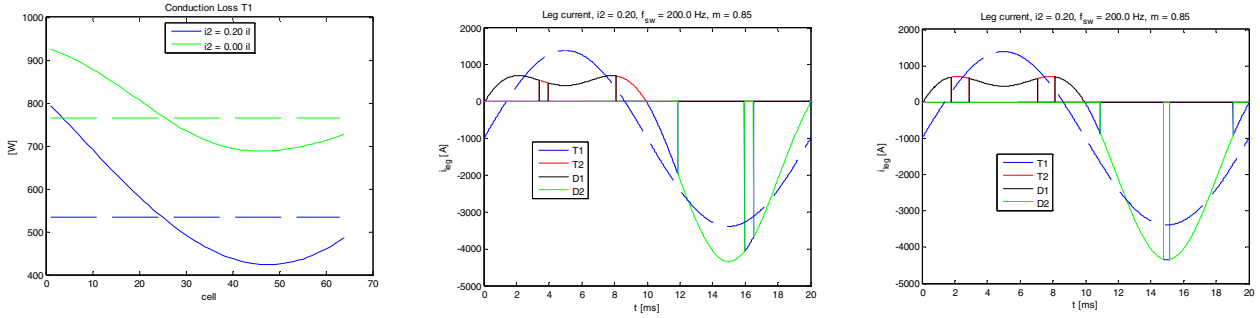

Fig. 11: Left: T1 Conduction losses - Center: Leg current flowing throw T1 (blue), T2 (red), D1(black), D2 (green) with 2^{nd} harmonic injection; in dashed blue the leg current with only DC circulating current, in the first cell - Left: Same quantities of center panel in cell n. 32

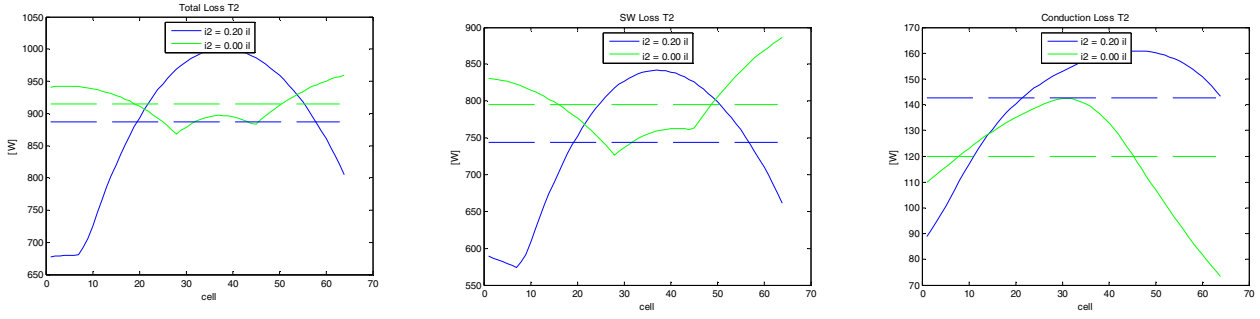

Fig. 12: Left: Total losses in T2 – Center: Switching losses in T2 – Right: Conduction losses in T2

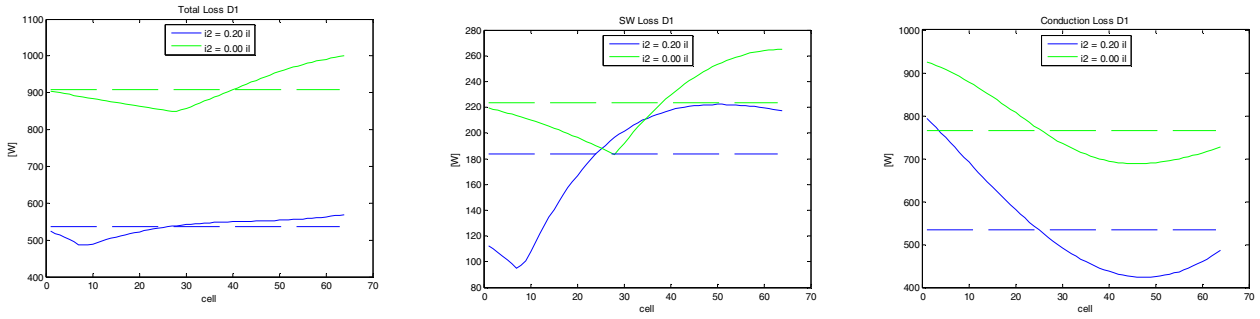

Fig. 13: Left: Total losses in D1 – Center: Switching losses in D1 – Right: Conduction losses in D1

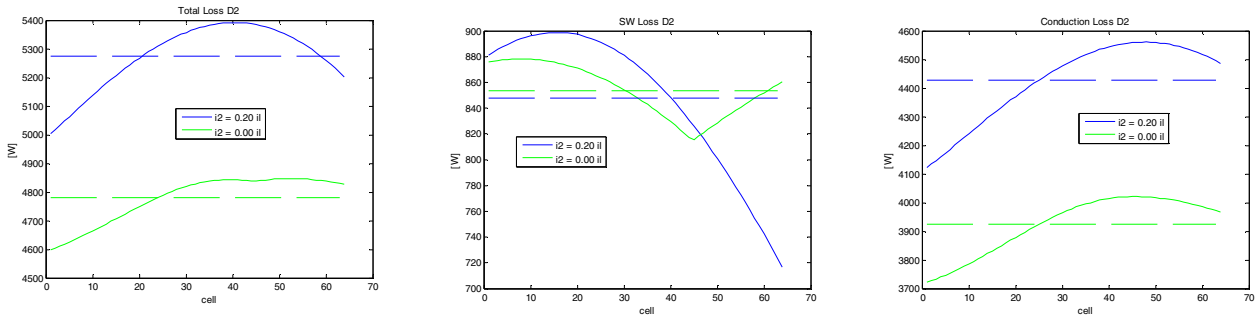

Fig. 14: Left: Total losses in D2 – Center: Switching losses in D2 – Right: Conduction losses in D2

It can be appreciated the improvement (improv. in the Tables) in efficiency for each device of the cell considering the conduction losses (CL), the switching losses (SWL) and the total losses (TL) with the second harmonic circulating current i_2 injection. The results summarized in Table V and VI show that the efficiency improvements in the rectifier mode are obtained with both couples of semiconductors and are both low and depend on the semiconductor type, with variations of about 50% between the two types; in any case the cell losses improvements are always lower than 4%. Results show how the greater variations from the losses point of view are observed for T1, D1 and D2. As in the inverter mode case, the devices T1 and D1 show improvements for the conduction and switching losses, whereas in T2 and D2 the conduction losses are incremented and the switching ones are decremented. Unfortunately, in the rectifier mode, the more stressed device is D2 and, only for D2, the increment in the conduction losses is not compensated by the decrement in switching losses, as it can be observed for T2, the device with the lower stress, in a specular mode as observed in the inverter mode. The last column of Table V and VI shows the total absolute improvement related to each device and it's possible to appreciate how the greater variation is in the case of 125 mm semiconductors, and refers to the most stressed device, i.e., to D2, and corresponds to an increment in the losses. This negative variation is compensated by the decrement of the losses in the two devices T1 and D1. The global losses variation of the cell is a decrement of the losses, which is lower than the decrement related to T1 or D1 and lower than 2%. With reference to the 85 mm semiconductor case, the situation is slightly different with respect to the inverter working mode; the greater loss variation is not related to D2, but to T1, so the cell losses improvement is higher and equal to about 3.3%, about twice with respect to the case with 85 mm semiconductors.

In order to understand the mechanism involved in the losses devices sharing of the cell with the current second harmonic, as in the inverter mode, it is important to analyse the behaviour of the three main components involved in the losses: T1, D1 and D2. In the central panel of Fig. 11, the current of the cell is shown in one of the better cases, where the losses are lower with the injection of the second harmonic, as shown in the left panel of Fig. 10, corresponding to the last cell.

The main component involved in the losses is D2. For the conduction point of view, the current is incremented significantly, but the conducting time is slightly decremented, so the conduction losses are slightly increased, as shown in Table V and VI. From the switching point of view, in the last cell, the first and only turn-off switches higher current with the second harmonic, but there is a compensation with the elimination of the turn-off event at t = 10 ms, which is an event present without the second harmonic, thanks to the reduced conducting time, so in this cell the switching losses are reduced. In the cell n. 32 there are more switching events; considering for instance the switching event at t = 15 ms, the increment of switched current is higher with respect to the last cell, so the switching losses for the cell n. 32 are worse with the

second harmonic current. The central panel of Fig. 14 shows how, in average, the switching losses related to D2 are slightly lower with the second harmonic current.
It is important to note, as in the inverter working mode, how the incremented losses of the more stressed device of the cell, D2, have a negative effect on the whole system: the current limit of the system is given by the maximum allowable junction temperature, so incrementing the losses of the more stressed device means that the thermic margin of the system is decremented. The simulations shows how, with the asynchronous modulation, the maximum junction temperature is increased, as in the inverter case, by about 2°C, value that can be considered acceptable in this case, but in general this limit needs always to be taken into account.

Table V: Improvement in semiconductor losses with second harmonic circulating current i_2 injection with medium I_{dc} (Rectifier mode - 85 mm diameter power semiconductors)

I_{dc} 1500A									
i_2	0			0.20					
	CL[W]	SWL[W]	TL[W]	CL[W]	improv.	SWL[W]	improv.	TL[W]	improv.
T1	381	1666		265	30.4%	1639	1.6%		143W
T2	59	403		71	-20.3%	372	7.7%		19W
D1	260	213		141	45.8%	207	2.8%		125W
D2	1451	536		1627	-12.1%	484	9.7%		-124W
Σ	2151	2818	4969	2104	2.2%	2702	4.1%	4806	3.3%

Table VI: Improvement in semiconductor losses with second harmonic circulating current i_2 injection with high I_{dc} (Rectifier mode - 125 mm diameter power semiconductors)

I_{dc} 3000A									
i_2	0			0.20					
	CL[W]	SWL[W]	TL[W]	CL[W]	improv.	SWL[W]	improv.	TL[W]	improv.
T1	766	3355		534	30.3%	3311	1.3%		276W
T2	120	795		143	-19.2%	744	6.4%		28W
D1	686	224		352	48.7%	184	17.9%		374W
D2	3925	854		4428	-12.8%	848	0.7%		-497W
Σ	5497	5228	10725	5457	0.7%	5087	2.7%	10544	1.7%

Conclusions

This paper presents evidence on how it is possible to decrement the cell capacitor voltage ripple of a MMC converter for HVDC applications, injecting a 2^{nd} harmonic circulating current, i.e., incrementing the current in the cell without increasing the total losses, but slightly decreasing them. The price to pay is the increment of the losses in the more stressed semiconductor device, the lower IEGT T2 in the inverter working mode or the lower diode D2 in the rectifier working mode, so decrementing the thermal margin of the converter. Simulations show how, in both cases, the junction temperature raises of about 2°C, value that can be considered acceptable in almost all applications, but that needs to be verified in the initial phase of the conversion system project.

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