A 2-kfps Sub-μW/pix Uncooled-PbSe Digital Imager with 10-bit DR Adjustment and FPN Correction for High-Speed and Low-Cost MWIR Applications

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Abstract

Mid-wavelength infrared (MWIR) thermography is an emerging technology with promising applications such as industrial monitoring, medicine and automotive, but its use in high-speed cameras is not yet widespread due to the lack of inexpensive sensor integration solutions and their common reliance on bulky cooling mechanisms. This work fills the gap by presenting a monolithic uncooled high-speed imager based on vapor-phase deposition lead selenide (VPD PbSe) photoconductors and a fully digital and configurable CMOS read-out integrated circuit (ROIC) to operate the MWIR imager. This ROIC features cancellation of PbSe dark current, compensation of its output capacitance and correction of the fixed pattern noise (FPN) caused by process non-uniformities in CMOS fabrication and detector deposition. The low-cost 80×80 imager has been integrated using 0.35 μm 2P4M standard CMOS technology and PbSe detector post-processing with 135 μm pixel pitch and 60 % fill factor values. Experimental opto-electrical performance exhibits 10-bit real-time FPN compensation and DR calibration over the entire focal plane operating at 2 kfps, sub-0.5 LSB inter-pixel crosstalk, sub-μW pixel power consumption, and an overall figure of merit of 55 mK×ms.

Index Terms

CMOS, imager, digital pixel sensor (DPS), fixed pattern noise (FPN), low-power, infrared, MWIR, PbSe, uncooled, high-speed, low-cost.

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I. Introduction

INFRARED (IR) has always been a spectral region of interest for imagers due to the capability of matter to self emit at this wavelength range, in contrast to the illumination required in the visible, and the thermal information obtained from observed objects. This interest is in agreement with the large number of IR imagers incorporated into strategic, industrial, scientific and medical equipments for a wide range of applications like surface analysis by thermography [1], automotive night vision [2], object tracking [3] and weather forecast [4].

From the detector viewpoint, two major technologies are in practice dominating the IR imaging market. On the one hand, microbolometers [5] are the common choice for thermal imaging in the long-wavelength IR (LWIR) range, showing very low-cost figures thanks to their CMOS technology compatibility and uncooled operation. Although pixel pitch is being steadily improved [6], [7], microbolometers intrinsically suffer from limited signal sensitivity and frame rate (below 100-fps). On the other hand, quantum-well IR photodetectors (QWIP) [8] can cover those fields demanding both high-speed and high-sensitivity, typically in the short-wavelength IR (SWIR) range, at the expense of higher costs and power consumption due to their hybrid packaging and cryogenic cooling, respectively. An interesting alternative to avoid this trade-off is the choice of lead selenide (PbSe) photoconductive technologies. These mid-wavelength IR (MWIR) detectors allow uncooled operation like microbolometers, but with the high-speed capabilities of their QWIP counterparts. Target applications include: automotive, metallurgy, glass and paper manufacturing, where process dynamics above the kHz play a crucial role; pollution monitoring, accordingly to the MWIR signature of carbon-based molecules; and transportation, as to prevent axis, wheel, motor overheating and malfunctioning combustion. A Noise Equivalent Temperature Difference (NETD) below 0.5 K is commonly required in these practical cases.

Classically, the severe drawbacks in terms of photoresponse uniformity and long term stability

of the chemical bath deposition (CBD) methods [9] used to build PbSe MWIR detectors have limited their use to linear imagers only. During last years, the introduction of PbSe technologies based on vapor phase deposition (VPD) [10] are enabling to overcome the previous CBD limitations, extending PbSe post-processing compatibility to CMOS technologies in order to obtain monolithic active focal plane arrays (FPAs) with high fill factors. In this sense, results from a 32×32 VPD PbSe CMOS MWIR imager prototype exceeding 1 kfps at room temperature have been reported [11].

From the CMOS circuit viewpoint, the use of PbSe detectors introduces specific design challenges both at FPA and at active pixel sensor (APS) levels of the imager. First, this type of IR detectors exhibits unitary dark-to-signal current ratios strongly higher than those from the rest of quantum light sensing technologies (typically orders of magnitude below unity). As a result, a direct cancellation mechanism of this PVT-dependent large offset current is needed inside each APS, which is not covered by the existing background suppression techniques [12], [13]. Second, the large parasitic capacitance of the post-processed PbSe detector can limit signal bandwidth in case of using it as the pixel integration capacitor. Hence, in-pixel capacitive transimpedance amplifiers (CTIAs) [14]–[17] are required in practice to exploit the high-speed capabilities of PbSe detectors. Third, due to the nature of the VPD post-processing, fixed pattern noise (FPN) plays an important role on the response of PbSe FPAs. In consequence, both offset (dark current) and gain (responsivity) corrections are also needed inside each APS. A solution for this double compensation is not addressed by the available FPN reduction approaches [14], [18]–[22]. Finally, very low-power operation is mandatory for the CMOS pixel circuits to minimize thermal effects on the uncooled MWIR detector stacked on top of the APS.

In order to achieve the above circuit design challenges, this paper proposes an imager architecture for VPD PbSe CMOS imagers with dynamic and digital programmability of both offset and

gain parameters for each individual pixel. The device takes advantage of a sub-μW truly digital pixel sensor (DPS) with CTIA-based integrator and built-in 10-bit analog-to-digital converter (ADC) to offer kfps uncooled imaging in the MWIR spectrum. The development of this high-speed imager was initially announced in [23], but no details about its design nor its experimental results were revealed. The present paper is organized as follows. General imager characteristics and read-out architecture are detailed in Sections II and IV, respectively. Section III reviews the uncooled MWIR detector technology. The monolithic PbSe CMOS integration of the resulting imager is described in Section V, while Section VI compiles all the experimental MWIR results. Finally, conclusions are summarized in Section VII.

II. Digital Imager Overview

Basically, the imager of Fig. 1 is constituted of a digital-only I/O focal plane of 80 fully independent rows of daisy chains of 80 DPS cells each. Oppositely to traditional image sensor architectures where pixel bias, digital control, row/column decoding and/or ADC is distributed outside the FPA [13], [14], [16], [18], [20], [22], our approach integrates all functionality locally inside each pixel avoiding any analog signal sharing between them. The PbSe quantum detector described in Section III is deposited on top of the CMOS array and performs photoconductive transduction of the incoming MWIR radiation. This input current is acquired, conditioned and converted to digital domain, at pixel level, in order to deliver high-SNR 10-bit output video frame sequences. To perform such tasks, every pixel offers individually programmable adjustment of both offset and gain parameters. Since imager pixels can be configured at the same time and resolution as the output frame code is read, both technology-dependent spatial noise and dynamic range on output images can be improved in real-time and without noticeable speed costs.

All pixels in the FPA are accessed by rows, and operated according to two iterative global modes: synchronous communication and asynchronous acquisition (Fig. 1(c)). During commu-

nication, the 10 bit/pix correction maps are serially written-in through the bus of row inputs, and translated to its corresponding in-pixel analog circuit configuration; meanwhile, the 10 bit/pix compensated frames are also serially read-out through the bus of row outputs. Offset and gain maps are entered in different programming-in/read-out time slots (e.g. alternate frames) at a variable refreshing frequency adjustable to system requirements. Over acquisition, all pixels in the FPA are set up to collect the detector currents and to asynchronously integrate their effective values to digital 10-bit words. The resulting data is stored in each pixel and read out in the next frame cycle. Both DAC and ADC are reset while in communication before and after D/A conversion, respectively. Fig. 1 also displays a practical scenario of complete offset and gain tuning with in-pixel FPN compensation. A frame set with no offset compensation and a common medium gain value usually exhibits the visual noise of Fig. 1(a), whereas appropriate individual pixel calibration significantly optimizes image generation as depicted in Fig. 1(b).

III. Uncooled MWIR PbSe Photoconductive Technology

Polycrystalline PbSe is a quantum photoconductor composed of a compact layer of PbSe microcrystals to provide detectivities up to 10^9 cm$\sqrt{\text{Hz}}$/W and μs-range response times in the MWIR spectrum range at room temperature. Such characteristics make PbSe a remarkable candidate for high-speed and low-cost uncooled IR detection. Standard polycrystalline PbSe films are produced by Chemical Bath Deposition method (CBD). Wet CBD imposes serious technological limitations on uniformity and reproducibility to manufacture medium and large-scale 2D detector arrays in monolithic devices. Primary reasons the incompatibility between wet processing and the multi-level metal substrates required in order to obtain good filling factors and low metal density at detector contacts. To overcome this deficiencies, an alternative procedure based on thermal evaporation of PbSe in vacuum followed by a specific sensitization method was developed [10]. As depicted in Fig. 2, the new VPD method deposits a thin layer of PbSe

on standard CMOS wafers that provide the read-out electronics, offering good yield in common 8-inch wafers and compatibility with complex monolithic multilayer structures like interference filters.

In order to integrate PbSe detectors and CMOS circuits in a single die, two key technological bottlenecks had to be saved: compatibility between detector and circuit materials at their interface, and CMOS operational drifts that PbSe sensitization treatments at high temperature could induce. For the former, PbSe was contacted by gold (Au) on top of a stacked metal layer to access each individual CMOS sensor. For the latter, a two-fold strategy was selected as follows: PbSe post-processing was redefined in order to lower the temperature and duration of each technological step, and design rules for high-stress environments were strictly observed according to foundry recommendations. All phases and masks were optimized to post-process standard 8-inch 0.35 μm 2P4M CMOS wafers. The obtained pixel stacked structure allows DPS fill factors to exceed 50 %. Unlike microbolometers, photoconductive PbSe detectors do not need to be operated in vacuum to minimize thermal conductivity effects from surrounding environment. Hence, the whole IR imager can be encapsulated in low-cost standard packages with sapphire window.

Fig. 3 shows the MWIR response of the post-processed PbSe detector at room temperature, which returns the typical triangular-shaped spectral profile of quantum detectors. When cooled, the detector peak sensitivity is shifted towards longer wavelengths (e.g. 4 μm at 253 K). Signal modulation bandwidth under uncooled operation extends up to 60 kHz, and reduces at lower temperatures with an approximate rate of 2.7 %/K. This behavior is driven by the influence of detector resistance on its internal RC product. The spectral properties of VPD PbSe were studied using the blackbody of Fig. 9 and f/1 aperture optics.

A common relevant metric used to characterize the performance of IR imaging systems is the noise equivalent temperature difference (NETD), which evaluates the response of such systems

in terms of thermal sensitivity. It is described by (1) as the temperature change ΔT, for incident radiation, that gives an output signal change ΔV_s equal to the RMS noise level V_n [24]

$$NETD = V_n \frac{\Delta T}{\Delta V_s} \tag{1}$$

Background radiation is usually the main source of noise in IR quantum detectors. Therefore, at the background limited performance (BLIP) conditions photon-induced shot noise dominates NETD, which can be approximated by the equation

$$NETD = \frac{1}{\tau_o C_{T\lambda} \eta_{BLIP} SNR_B} = \frac{1}{\tau_o C_{T\lambda} \eta_{BLIP} \sqrt{N_c}} \tag{2}$$

where τ_o stands for the optics transmission, $C_{T\lambda}$ is the thermal contrast, η_{BLIP} the percentage of BLIP (i.e. the ratio of photon shot noise to composite FPA noise), SNR_B the signal-to-noise ratio at background radiation and N_c is the number of photogenerated carriers collected for a given acquisition time T_{acq}. Because of the high resistive (typically around 1 MΩ) nature of PbSe detectors, current read-out at constant voltage bias is preferred over voltage read-out at constant current strategies. In practice, PbSe exhibits both noticeable background photogeneration mean and deviation due to uncooled operation and the amorphous nature of its structure, respectively. The latter can lead to signal-to-dark current ratios close to unity under common radiation scenarios (e.g. 1 μA for a 1-V biasing). The measured parameters of the VPD PbSe photoconductor are summarized in Table I. NETD performance was measured at a blackbody temperature of 600 K, accordingly to the MWIR spectral range of the imager.

IV. Fully FPN-Compensated DPS-Based Read-out Architecture

When assessing the performance of APS-based imagers, the NETD figure of (2) is extended to include noise contributions of the read-out circuitry itself. Considering all major noise sources uncorrelated, the percentage of BLIP in integrating topologies can be described as

$$\eta_{BLIP_{APS}} = \left(1+\frac{\sigma^2_{ROIC}}{\sigma^2_{photon}}\right)^{-1/2} \simeq \sqrt{N_c}\left(N_c+\sigma^2_{det}+\sigma^2_{samp}+\sigma^2_{integ,ir}+\sigma^2_{drv,ir}+\sigma^2_{MUX,ir}+\sigma^2_{ADC,ir}\right)^{-1/2} \quad (3)$$

where σ^2_{photon} is the shot noise power of photon background in carriers and σ^2_{ROIC} stands for the sum of all ROIC noise contributions, mainly: composite dark current, thermal and flicker detector noise (σ^2_{det}), kTC noise of the sample-and-hold stage (σ^2_{samp}), and the input-referred noises of integrator ($\sigma^2_{integ,ir}$), line driver ($\sigma^2_{drv,ir}$), multiplexer ($\sigma^2_{MUX,ir}$) and ADC ($\sigma^2_{ADC,ir}$).

In order to improve signal integrity and grant high-speed operation at low-power figures, the proposed read-out architecture of Fig. 1 implements a fully digital I/O interface with massive pixel-parallel asynchronous A/D conversion. First point to note in this figure is the absence of any analog bus. As a result, $\sigma^2_{MUX,ir}$ and $\sigma^2_{drv,ir}$ contributions are automatically removed from (3). Second, in-pixel ADC allows to reduce the sampling ratio (so equivalent noise bandwidth) proportionally to the FPA number of rows (M) and/or columns (N) as to external or column/row-wise ADC, respectively. In consequence, and supposing the ADC is thermal noise limited, $\sigma^2_{ADC,ir}$ can be downscaled up to $\sigma^2_{ADC,ir}/MN$ at the cost of even stronger power and area circuit design constrains. For this purpose, asynchronous integrate-and-fire modulation [25], [26] and in-situ digital low-pass filtering are chosen for the in-pixel ADC. The resulting ADC architecture opens the possibility of pixel area optimization against kTC noise, since both capacitance of the analog integrator and capacity of the digital integrator play an equivalent role.

Compared with other kfps DPS-based CMOS implementations like [27], our design combines the aforementioned pulse-density modulation with all-digital and local-only signaling to curtail crosstalk in critical analog nodes of the layout. Both spike-counting and local interconnectivity avoid tracing pulsating signal paths throughout the focal plane, with the latter also allowing to drastically optimize pixel digital output buffers in terms of power; local biasing provides

additional noise immunity by cutting off coupling noise on power supply lines. To further avoid the presence of switching perturbation along integration, acquisition and communication are separated in two well-differentiated phases as described in Section II: no clock is generated while performing A/D conversion. Switching noise mainly arises in the substrate and propagates through circuit asymmetries over the pixel sensor [28]. The presence of perturbations on power supply nodes, either at routing or substrate level, are reflected in higher $\sigma^2_{integ,ir}$ and $\sigma^2_{ADC,ir}$ values. They are specially noticeable in the quantizer stage as comparator jitter noise and can severely limit the performance of the system in terms of NETD. Last but not least, every DPS cell includes a built-in DAC to configure both offset-cancellation and gain tuning at individual pixels. Apart from attenuating detector and CMOS FPN along the focal plane, offset programming circuitry allows to boost the number of effective photogenerated carriers integrated in acquisition, and provides additional NETD enhancement according to (2). Under this scheme, offset-correction σ^2_{offs} and integrator $\sigma^2_{integ,ir}$ noises become key ROIC contributors during acquisition. The former adds to σ^2_{det} in (4) as input noise current σ^2_{offs}:

$$\eta_{BLIP_{DPS}} \simeq \sqrt{N_c}\left(N_c + \sigma^2_{det} + \sigma^2_{offs} + \sigma^2_{integ,ir} + \sigma^2_{ADC,ir}\right)^{-1/2} \tag{4}$$

The DPS circuits used in the present imager are based on the nanopower topologies introduced by authors in [29]. This implementation is adapted to the particular operating conditions of the PbSe detector and to increase the yield of its monolithic integration. Layout is compacted to a pitch of 135 μm for a low-cost 0.35 μm 2P4M CMOS technology. Every pixel cell shown in Fig. 4(a) includes its own analog reference and bias generator, and DAC for FPN suppression. Furthermore, and in order to avoid input bandwidth limitations due to the detector capacitance values of Table I, an specific circuit for input capacitance compensation is also incorporated.

As depicted in Fig. 4(b), only 5 control signals are needed to operate all the DPSs of the focal plane and, by extension, the entire read-out integrated circuit (ROIC): `cal` is used to select

between offset or gain programming, `edac` to enable the former offset/gain configuration and define its resolution, `count` to select between acquisition or communication mode, `ninit` to initialize acquisition and `clk` to synchronize digital program-in/read-out communications. All DPSs follow the two global communication and acquisition modes previously described. In the first case, offset and gain FPN corrections can be serially programmed at every other frame as V_{prog} through the 10-bit switched-capacitor DAC of Fig. 4(a) and the chronogram of Fig. 4(b) according to the equation

$$V_{prog} = V_{DD}\frac{1-2^{-N_{bit}}}{2^{N_{bit}}-1}\mathtt{d_{in}} \doteq G_{DAC}\mathtt{d_{in}} \tag{5}$$

where G_{DAC} and N_{bit} stand for the DAC conversion gain and the number of effective bits used for programming, respectively. Even under ideally null FPN conditions, ADC gain tunability offers an additional mechanism to dynamically change the DPS contrast and, consequently, to adapt image DR by regions according to instantaneous illumination conditions. Fig. 5 details the circuit implementation for offset and gain tuning. A non-overlapping clock is mandatory to provide proper isolation between sample and hold capacitances along programming. In order to minimize undesired injection to C_{samp}, charge in this node is added or removed through the direct path composed by minimum-size M1-M2 transistors. These devices are controlled by the corresponding logical function between each serially programmed code $\mathtt{p_i}$, as well as the non-overlapped sample clock `clks` and enable `edac` signals. The charge stored in C_{samp} is then recombined with C_{hold} through dummy-switch devices so as to compensate for both clock feedthrough and charge injection effects. To keep the desired linear response of (5), DAC capacitances were cautiously matched and shielded from neighboring nodes.

Depending on `count` state, the resulting V_{ref} analog value is either stored in M3 as comparator threshold reference voltage or combined again in C_{offset} as an M4 biasing gate voltage for I_{dark} generation. Thus, the $\mathrm{M_{offset}}$ device of Fig. 4(a) acts as a programmable DC current source

constituted, in practice, by M4 and M5 in Fig. 5. The lower 1/f noise of pFET stages facilitates to keep this phenomena below what is the dominant detector noise component. In this sense, M4a and M4b were accurately sized and paired to exhibit low flicker levels, as well as to cover its large (up to 5 μA) dark current excursion. The cascode device M5 was also included to safeguard offset cancellation from channel modulation and coupling distortion.

Back to Fig. 4(a), in acquisition mode the MWIR detector current I_{sens} is read through M_{in}: its local OpAmp control supplies a low enough input resistance to compensate for detector parasitic capacitance and set the differential biasing of PbSe photoconductor at 1 V. I_{dark} offset is then subtracted, and low-frequency components of the outcoming effective current are integrated by the CTIA. The resulting voltage ramp V_{int} is quantified at 1 bit by the comparator according to the ADC gain V_{ref} retained in C_{gain}. All generated events are fed back to reset the CTIA block, resulting at `event` in the asynchronous current-to-frequency conversion of the IR-radiation reliant value. Over an acquisition time of hundreds of μs, the digital module acts as a 10-bit ripple counter and completes the time-domain A/D conversion by low-pass filtering the asynchronous pulse-density modulated (PDM) stream. In the communication phase of the next frame, event generation is disabled and the 10-bit internal binary memory is reconfigured to provide a serial scanning path along the 80 DPS in every row of the focal plane, as depicted in Fig. 4(b). Considering CTIA reset times, the closed-loop operation of the previous circuitry generates a spiking signal of frequency

$$f_{event} = \frac{1}{T_{reset} + \frac{C_{int}V_{ref}}{(I_{sens} - I_{dark})}} \tag{6}$$

which corresponds to a digital inter-frame counted word of value

$$\mathtt{d_{out}} = \frac{f_{event}}{f_{acq}} = \frac{T_{acq}}{T_{reset} + \frac{C_{int}V_{ref}}{(I_{sens} - I_{dark})}} \tag{7}$$

Fig. 6 draws the detailed schematic employed for pulse-density modulation. M1 and $C_{int/CDS}$

constitute the class-AB CTIA stage, whose flicker contributions are canceled at reset by its particular correlated double sampling (CDS) triple-switch scheme. Along event duration, M1 noise is integrated in the same $C_{int/CDS}$ and removed from the effective noise charge. Previous input compensation also allows to reduce the influence of the detector capacitance over the integrator response. Together with the posterior low-pass filtering provided by the counter, $C_{int/CDS}$ can be compacted to 500 fF while keeping both kTC contributions to $\sigma^2_{integ,ir}$ in (4) and CTIA noise transfer gain at acceptable levels. V_{int} is quantized at the specified V_{ref} voltage by the high input/output-range comparator M2-M11. This topology is designed to deliver fast reset times at low-power operation by means of the dynamic biasing supplied by the positive feedback M13-M14 during threshold reach. All I_{bias} sources are optimized for sub-100nA static low-current consumption.

V. Monolithic PbSe-CMOS Integration

Fig. 7 shows the proposed 80×80 pixel imager after being integrated, together with other 32×32 pixel designs, over 8-inch wafers with standard 0.35μm 2P4M CMOS technology and the PbSe post-processing steps described in Section III. The 135 μm pixel size was selected according to pitch limitations imposed by the Au contact lithography itself. As shown in Fig. 7(c), metal 4 was mainly reserved to access the IR detector. Control lines were routed horizontally using metal 3, also employed to shield the in-pixel switched-capacitor DAC. Inside the FPA, pixels were arranged in alternate left-right row I/O directionality to allow for external concatenation. The fabricated imager occupied a total area of 14×14 mm^2 with 196 pads distributed along the four sides of the die. The succeeding low-cost packaging procedure included the following steps: Firstly, a rectangular sapphire glass was used in order to coat and protect the FPA from damaging external contamination or scratch. Wafers were then diced by laser and all pads of the ROIC were wire-bonded to the custom chip-carrier PCB of Fig. 8. The board accesses the

focal plane in 5-row groups, with an equivalent 16-bit I/O bus, matching standard 64-pin leaded chip-carrier (LCC) sockets. Is this external serialization which, in practice, limits the maximum frame rate of the imager to an equivalent 480x480-pixel FPA parallel-access time. Packaging was finally sheltered using standard dam and fill techniques.

VI. Experimental Results

The integrated imager was electro-optically tested after on-wafer screening using the setup shown in Fig. 9. This test bench was composed of a CI Systems SR-200 high-emissivity IR blackbody with mechanical chopping, a National Instruments (NI) PXI-1042 8-slot digital measurement system and a Pegasus S200 semi-automatic 200-mm probe station from Wentworth Laboratories. Custom NI Labview-based interfaces were developed for both on-wafer and in-package testing, which included the generation of the operational chronogram of Fig. 4(b).

Fig. 10 shows the experimental tuning response of 24 different DPS cells to both offset and gain parameters. Measurements were taken without IR illumination. In the first case, all gain programming codes (i.e. $\mathtt{d}_{\mathtt{gain}}$) were fixed to 226 LSB. The full 10-bit range of the in-pixel DAC depicted in Fig. 4 is devoted to match the dark current I_{dark} dispersion exhibited by PbSe detectors according to the $\mathtt{d}_{\mathtt{offset}}$ tuning curve of Fig. 10(a) and equation (7). Gain programming was performed after individual pixel offset calibration so that all outputs are aligned at half full scale for the same gain code of 226 LSB. As it can be clearly seen in Fig. 10(b), digital output reading follows the expected $1/x$ law also predicted by (7). Under negligible reset times, substituting V_{ref} by (5) in the previous equation results in the tuning characteristic

$$\mathtt{d}_{\mathtt{out}} = \frac{T_{acq}}{C_{int} G_{DAC} \mathtt{d}_{\mathtt{gain}}} (I_{sens} - I_{dark}) \tag{8}$$

inversely proportional to the input gain programming code. Integral non-linearities arise mainly from capacitive mismatching at both sample and hold nodes, and residual change injection and

clock feedthrough effects at DAC switches. In practice, there is a lower boundary at which the reference voltage for the comparator of Fig. 4 is no longer operative. Higher values are not effective either, as the transfer curve saturates beyond the MSB gain code. Thus, V_{ref} is programmed within a 9-bit span in order to compensate variations on both detector sensitivity and ADC conversion gain. The statistical results of Fig. 11 were obtained applying the same programming codes to the whole set of 6400 pixels of the focal plane, and corroborate the necessity of the included FPN correction mechanisms at pixel level.

Experimental results of the built-in FPN cancellation capabilities are presented in Fig. 12 to 14. All characteristics reported in this section were obtained setting the clock frequency to 10 MHz during communication phase except for the final 10 clock periods devoted to in-pixel DAC operation, when it was scaled down to 3 MHz. To generate large and uniform illumination, a 1173 K IR dark body was placed 10.75 cm away from the imager of Fig. 8, and signal strength was regulated by using 8 different apertures. Integration time was 500 μs for an operating frame rate of 1.1 kfps. No optics were used in these measurements.

The raw image shown in Fig. 12(a) corresponds to the digital read-out with null IR illumination when flat FPN code maps are programmed in all active pixels. On-chip frame equalization is achieved in Fig. 12(b) after applying offset and gain correction. Both maps are previously computed by an automatic calibration routine running in the NI-PXI system, configured in this case for the decimal output reading code 200 LSB, but reducible down to 50 LSB for the target DR extension of 60 dB. FPN calibration fingerprints are stored in the same system and recomputed only in case of severe temperature drifts. Fig. 13 shows pixel-to-pixel, row-to-row and column-to-column FPN statistics, expressed in percentages over full scale (1023 LSB), for the entire focal plane. Non-uniformities in the imager arise at row level in the direction of power line routing. Calibration of the image sensor manages to reduce all FPN values under 5 % full

scale. FPN decays in the right side of the figure are caused by saturation of pixel digital counts. Pre and post-equalization imager read-out codes evolve as described in (7), with good linearity up to the frequency limit imposed by T_{reset}, as reported in Fig. 14.

Concerning temporal noise, the NETD results of Fig. 15 were measured throughout the 49 dices that compose a full wafer. NETD improves with temperature according to the higher irradiance of hotter surfaces, displaying variances below 10 $\%$. Instantaneous read-out noise was measured 4 LSB for an acquisition time of 200 μs. Thanks to the operational flexibility of the imager, the predominant thermal contributions of $\sigma^2_{integ,ir}$ and σ^2_{offs} in (4) can be filtered out below the single-bit threshold by scaling T_{acq}, with a rate close to the square-root of cut-off frequency scaling, to a frame speed below 300 fps. Moreover, because the equivalent integrated signal increases proportionally to exposure time, SNR may be simultaneously risen by tuning each pixel gain in order to avoid saturation.

Fig. 16 presents dynamic captures of the MWIR imager, under uncooled operation, to a 330-Hz pulsing bright spot generated by mechanical chopping. Dark body temperature is in this case 773 K, placed at a distance of 40 cm from the FPA, using 3-cm focal length and f/1 aperture optics. The resulting digital frame sequence read at 1650 fps ratifies the speed capabilities of the imager. In the same figure, the ignition sequence of a lighter is also given as a practical high-speed application example. In proof of image uniformity and sensitivity, Fig. 17 shows two raw photograms acquired at this same rate from different scenes and devices. The absence of inter-pixel crosstalk evinces from the spatial acuity of disk slots in Fig. 17(a), even with the small array size and current detector pitch constraints of the imager. Fig. 17(b) displays effective temperature screening for a fast-moving flame. In terms of production yield, the total amount of operative pixels exceeds the 99.9 $\%$ of every FPA. Dead pixels are essentially sparse and can be easily interpolated though posterior post-processing.

Table II summarizes performance compared to state-of-art uncooled IR imagers. Even implementing the full A/D conversion and dual FPN compensation inside each active pixel, the imager keeps static power consumption below 1 μW/pix. The compact pitch reported in [7] is achieved at the cost of having analog pixel output, which may be prone to inter-pixel crosstalk and to extra FPN added at column or row levels, compared to all-digital I/O active pixels. Since the area of the DPS circuit proposed here is dominated by the digital block, pixel pitch can be reduced by downscaling the target CMOS technology. To the best of our knowledge this is the only uncooled IR imager operating at 2 kfps and supplying independent digital offset and gain tuning capabilities for FPN cancellation and DR adjustment at every pixel. The proposed architecture features an overall figure of merit NETD$\times\tau_{\text{imager}}$ of 55 mK$\times$ms, nearly one order of magnitude beyond the latest microbolometer frame-based imagers [7].

VII. Conclusions

An 80$\times$80 pixel MWIR PbSe imager has been integrated in standard 0.35 μm 2P4M CMOS technology. It is the first high-speed IR quantum image sensor monolithically fabricated in a standard VLSI CMOS technology and operates without any need of external cooling nor packaging in vacuum. The resulting low-cost imager has a fill factor of 60 $\%$ and it is capable of delivering frame rates up to 2 kfps with on-the-fly offset and gain FPN digital compensation at pixel level, 10-bit read-out and sub-μW/pix of static power consumption. Exhaustive electro-optical results prove the architectural efficacy of the read-out circuitry, which performs an FPN lower than 5 $\%$ and a FOM of 55 mK$\times$ms.

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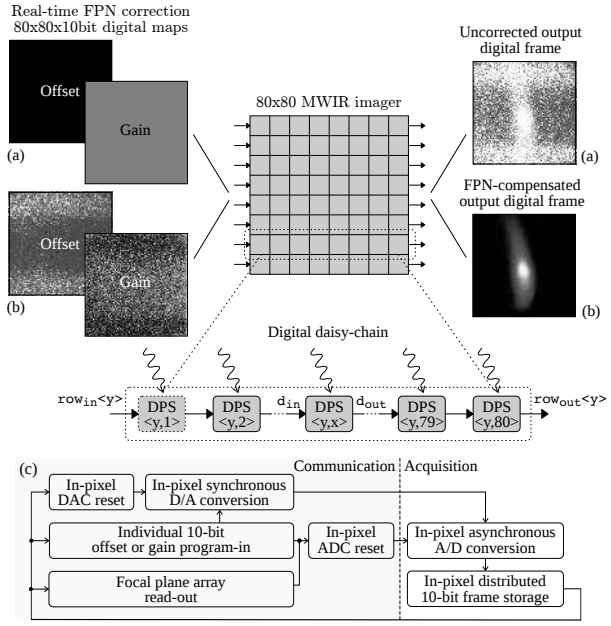
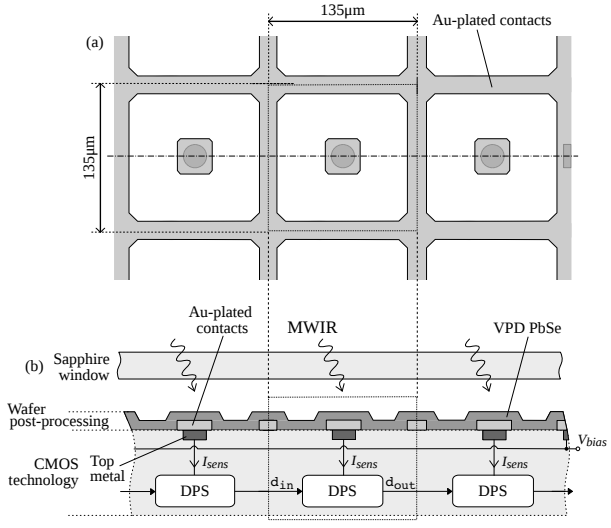


Figure 1. FPN-compensated digital I/O imager architecture. Practical examples of raw imaging under no compensation (a) and in-pixel FPN-corrected acquisition (b). Basic imager operation scheme (c). Figure not in scale.



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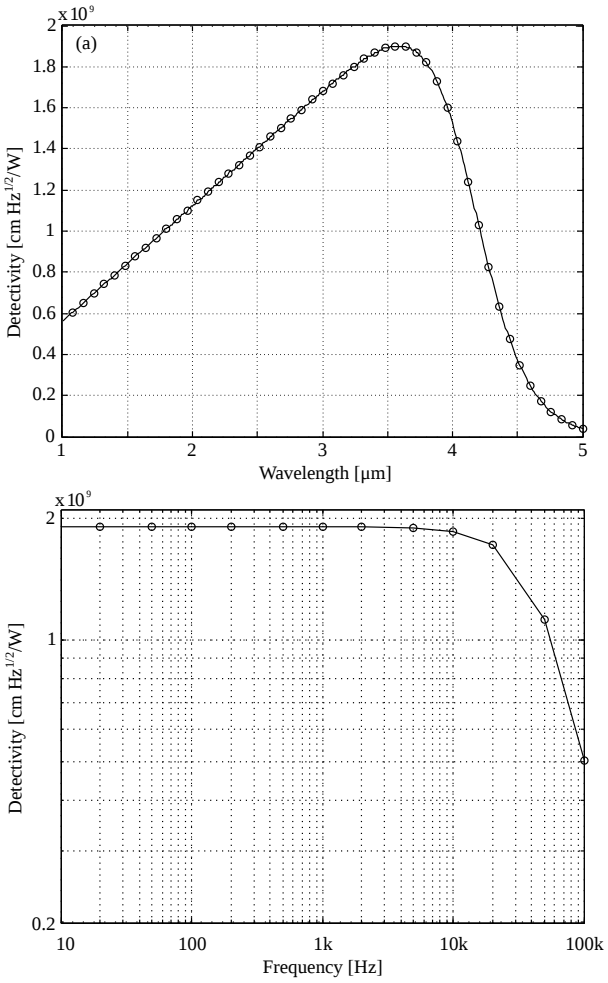

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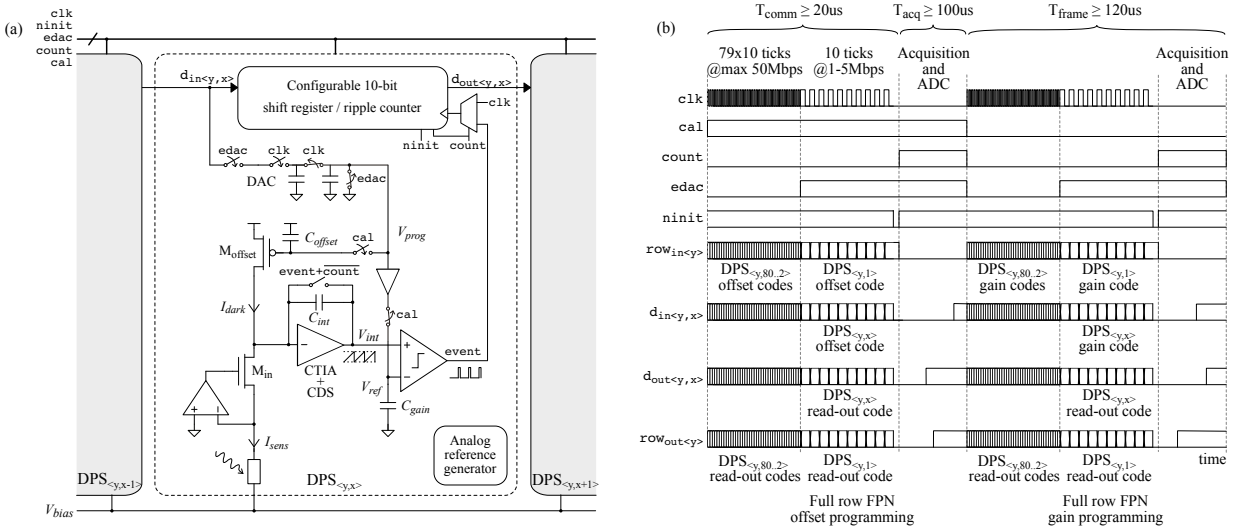

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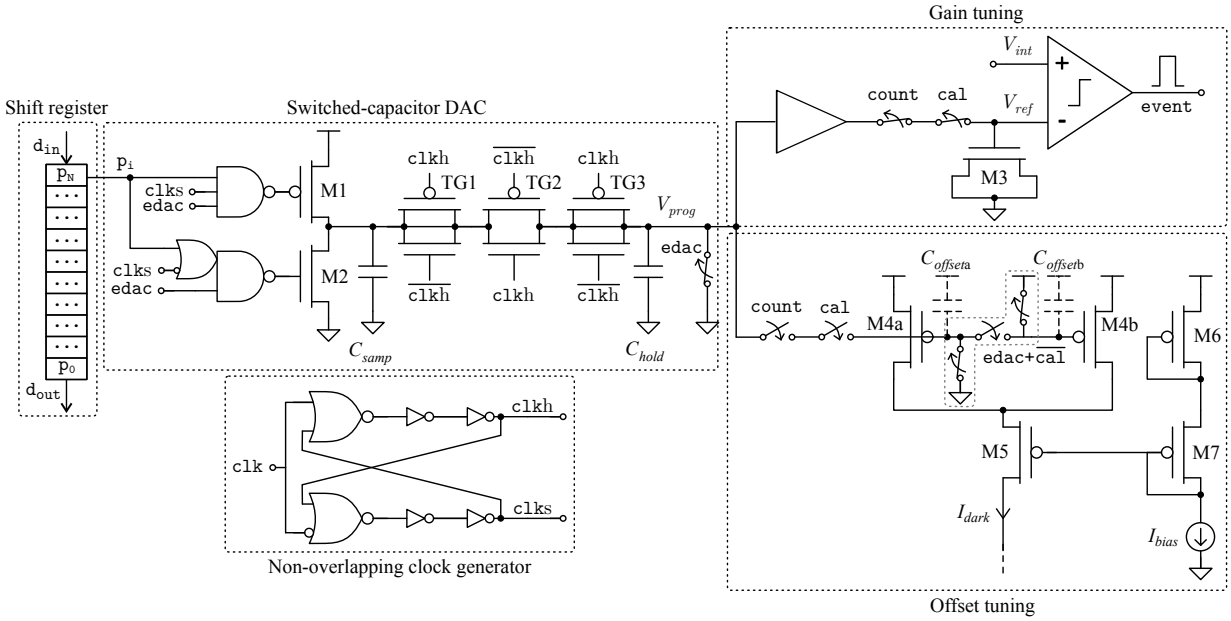

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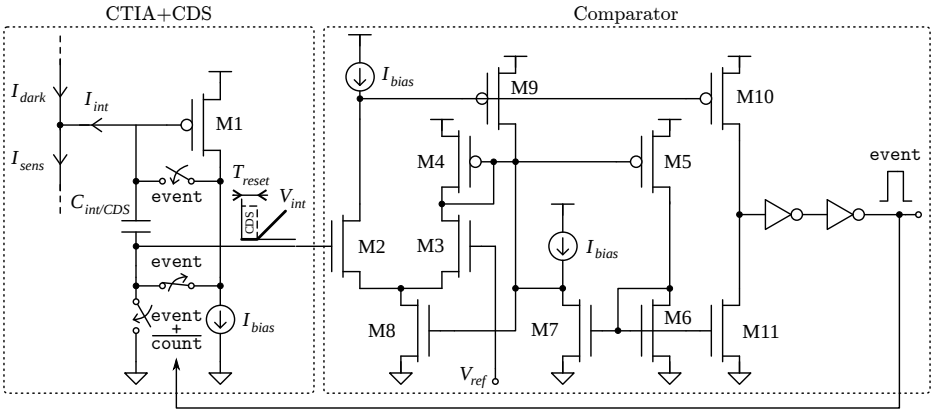

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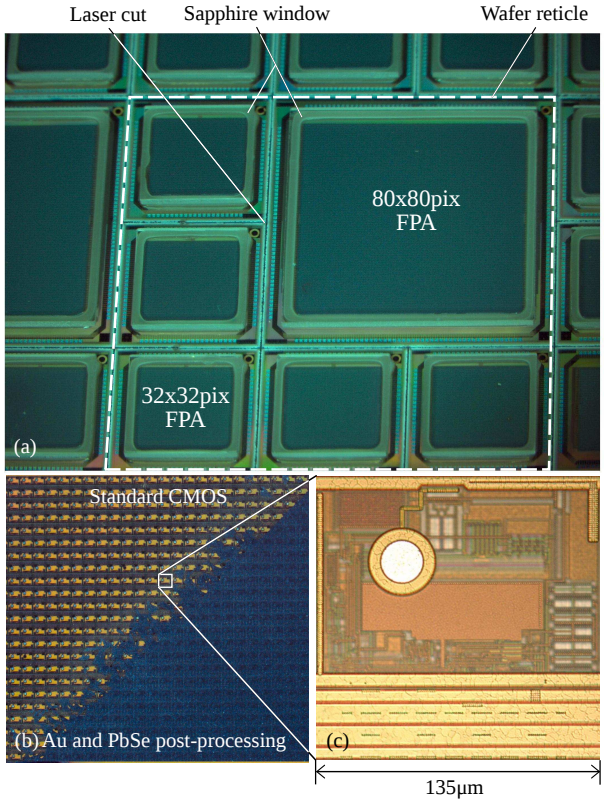

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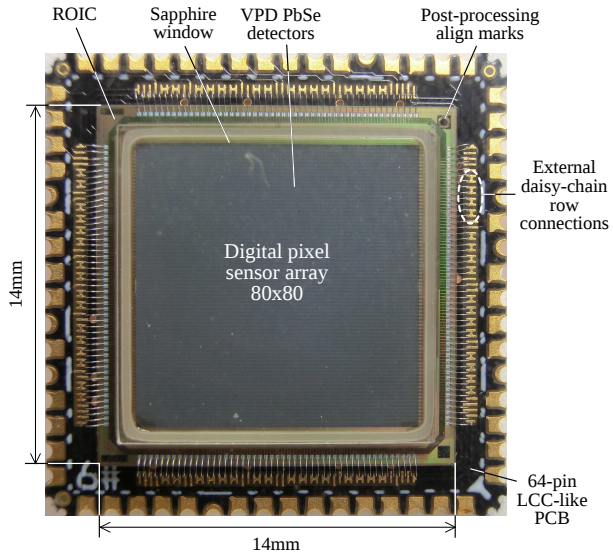

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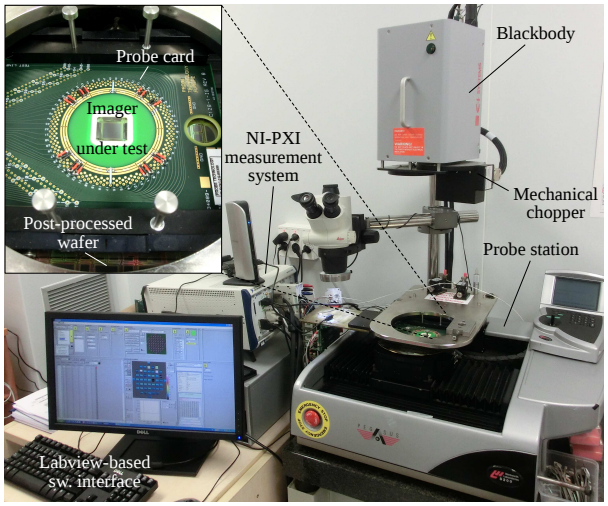

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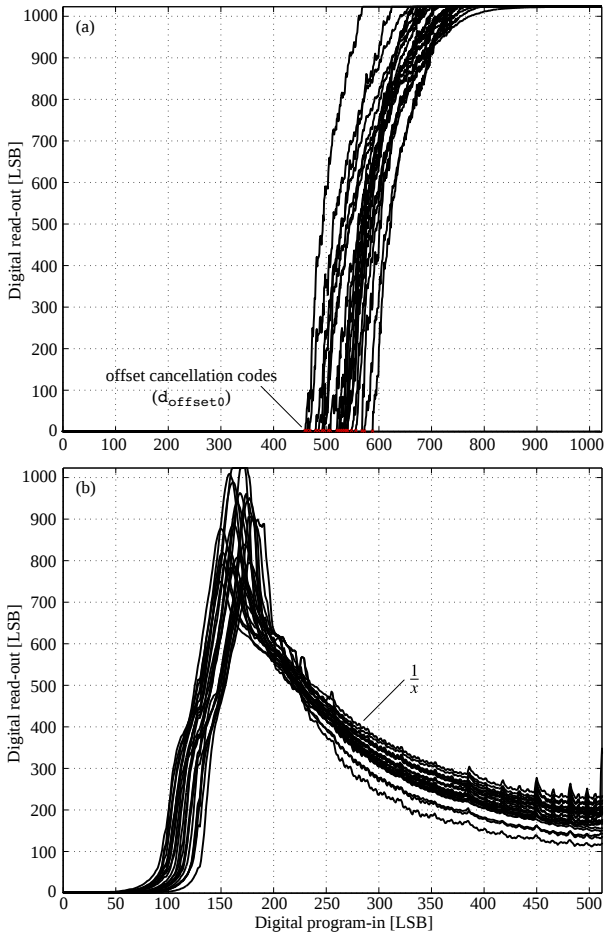

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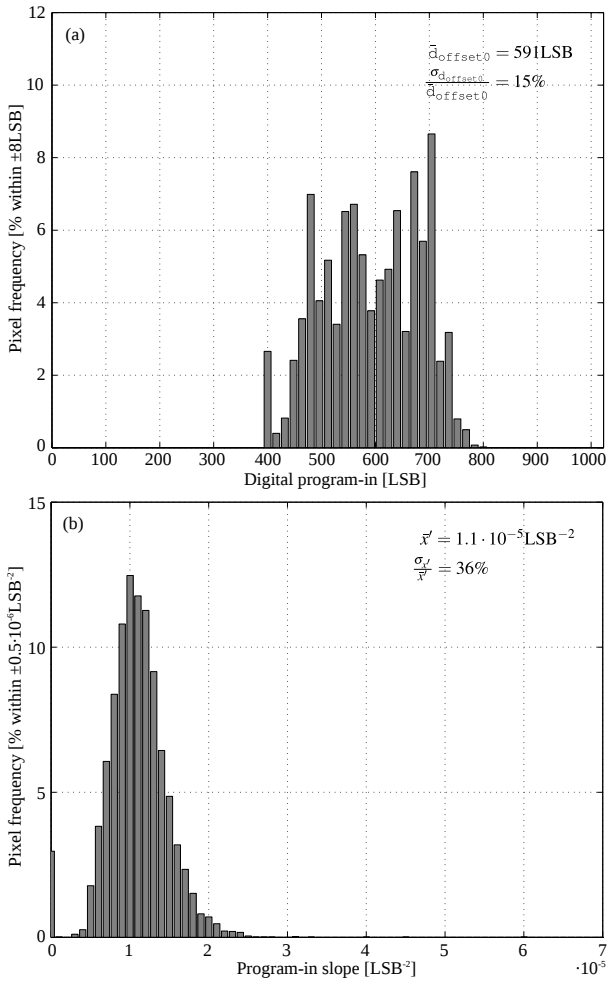

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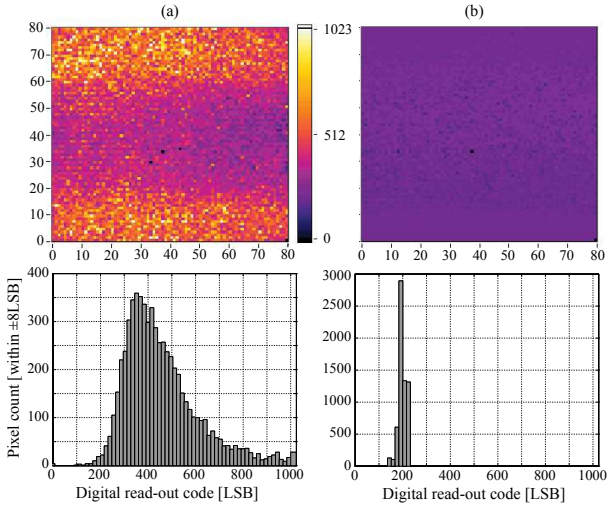

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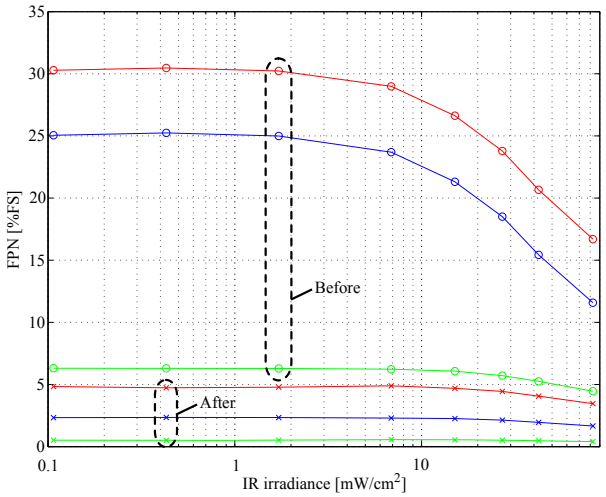

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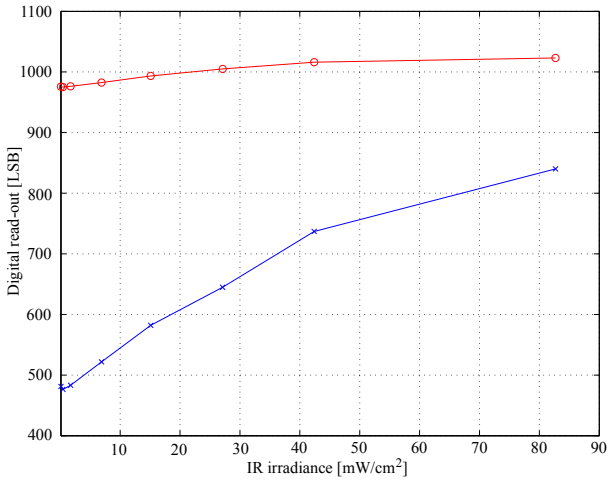

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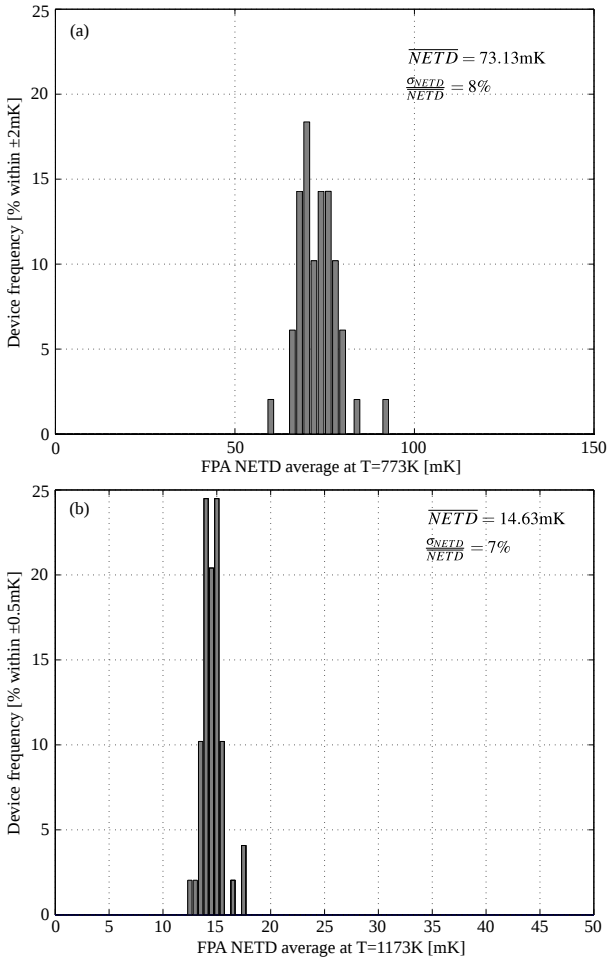

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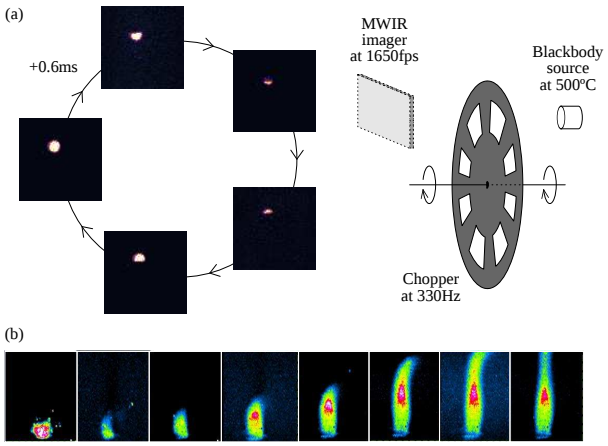

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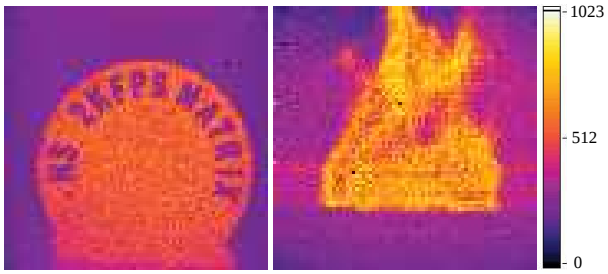

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Table I
TYPICAL PARAMETERS OF THE INTEGRATED VPD PBSE PHOTOCONDUCTOR AT ROOM TEMPERATURE.

Parameter	Value	Units
Array pitch	135	μm
Spectral range at -3dB	1.7 to 4.3	μm
Peak detection wavelength	3.6	μm
Peak detectivity	1.9×10^9	cm$\sqrt{\text{Hz}}$/W
Corner frequency (f_c)	60	kHz
NETD at 600K	125	mK
Dark resistance at V_{bias}=1V	1$\pm$20%	MΩ
Dark current at V_{bias}=1V	1$\pm$20%	μA
Output capacitance	200	fF

Table II
PERFORMANCE COMPARISON BETWEEN UNCOOLED IR IMAGERS.

	Posch et al. [5]	Dupont et al. [7]	This work
CMOS technology	0.35μm 2P4M	0.18μm 1P6M	0.35μm 2P4M
IR sensing technology	LWIR a-Si μbolometers	LWIR a-Si μbolometers	MWIR VPD PbSe photocon-ductor
Pixel array	64$\times$64	640$\times$480	80$\times$80
Pixel pitch	50μm	17μm	135μm
Fill factor	69%	N.A.	60%
Max. frame rate	30fps	60fps	2000fps
Pixel output	Digital AER	Analog	Digital 10bit
Built-in-pixel FPN cancellation	None	Offset only	Offset and Gain
NETD$\times\tau_{\text{imager}}$	N.A.	400mK$\times$ms at 300K	55mK$\times$ms at 600K
Supply voltage	3.3V	4V	3.3V
Static power consumption	<1μW	<1μW	<1μW