## Security of Cloud FPGAs: A Survey

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Integrating Field Programmable Gate Arrays (FPGAs) with cloud computing instances is a rapidly emerging trend on commercial cloud computing platforms such as Amazon Web Services (AWS), Huawei cloud, and Alibaba cloud. Cloud FPGAs allow cloud users to build hardware accelerators to speed up the computation in the cloud. However, since the cloud FPGA technology is still in its infancy, the security implications of this integration of FPGAs in the cloud are not clear. In this paper, we survey the emerging field of cloud FPGA security, providing a comprehensive overview of the security issues related to cloud FPGAs, and highlighting future challenges in this research area.

## CCS Concepts: • Computer systems organization $\rightarrow$ Cloud computing; • Hardware $\rightarrow$ Reconfigurable logic and FPGAs; • Security and privacy $\rightarrow$ Systems security.

Additional Key Words and Phrases: Cloud FPGAs, FPGAs in Data Centers, Cloud FPGA Security

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### 1 INTRODUCTION

The last few decades have witnessed tremendous growth in the need for high-speed computation in the clouds. Solely using CPUs and GPUs can no longer meet the increasing performance demand, in terms of latency, throughput, and efficiency. Due to this, FPGAs have been integrated into cloud computation platforms to allow users to customize their hardware accelerators (to accelerate computationally intensive tasks) in the clouds. Many commercial cloud providers have already integrated or are integrating FPGAs in their cloud services platforms, e.g., Amazon [7], Huawei [67], Alibaba [6], Microsoft [15], and Texas Advanced Computer Center [123]. Intel predicted in 2016 that one-third of the cloud computing instances would have an FPGA by 2020 [76]. Users can use these cloud FPGAs to accelerate computationally intensive workloads like artificial intelligence tasks, software-defined networking, big data analytics, genomics, electronic design automation, and image and video processing [7, 92].

Comparing with traditional CPU-based or GPU-based cloud computation, FPGAs offer unique advantages. In particular, FPGAs are an ideal platform to perform *parallel* computation with *flexible* 

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Table 1. Comparison of cloud FPGA providers. The specifications and prices are based on [5–7, 15, 67, 97] as of March 2020, and the prices have been converted into US dollars for easy comparison. \*Microsoft Azure provides cloud FPGAs as hardware accelerators only for machine learning.

Provider	# FPGAs/instance	# virtual CPUs/instance	Memory (GB)	SSD (GB)	Price/hour
Amazon	1/2/8 (Xilinx VU9P)	8/16/64	122/244/976	470/940/3760	\$0.76 +
Huawei	1/2/4/8 (Xilinx VU9P)	8/32/64	88/224/352/448/708	N/A	\$0.98 +
Alibaba	1/2/4 (Intel Arria 10 GX 1150 or Xilinx VU9P)	4/8/16/28/32/56/64	16/32/60/64/112/120/128/224/256	N/A	\$0.14 +
Nimbix	1 (Xilinx Alevo U50/U200/U250/U280)	16/32/64	128	N/A	\$3.00 +
Azure ML*	1/2/4 (Intel Arria 10)	N/A	112/224/448	N/A	\$0.33 +

datapath and control. Thus, they can speed up computation with high efficiency. We explain these features in detail below.

- FPGAs can support *massive parallelism* in computation. For example, each FPGA on Amazon cloud (Xilinx UltraScale+ VU9P) has more than two million customer-accessible FPGA programmable logic cells [101], and they can all run in parallel to accelerate computation. For example, the instances on Amazon cloud accelerate the computing time by up to 100× [7].
- FPGAs are highly *flexible* in building a datapath with arbitrary width; e.g., if an application needs a 9-bit integer, the user can configure the datapath to exact 9 bits without underutilizing any computational resources, while in a CPU, it would require two bytes to store 9 bits. Moreover, it is easier to use FPGAs to build a customized state machine to control the computation on FPGAs, which is more efficient than using software for fine-grained controls.

In addition to these advantages, the cost of general-purpose commercial FPGA-based cloud computing instances is meager: one Amazon *EC2 f1.2xlarge* instance, which has one FPGA board, can cost as low as \$0.76 per hour [7], and one basic Huawei FP1 instance costs about \$0.98 per hour [67]. Table 1 presents a summary of the platforms provided by leading FPGA cloud providers. Users can choose proper specifications (e.g., the number and vendor of their FPGAs, the number of CPU cores, and the size of memory) for their cloud computation.

FPGA-accelerated clouds can be beneficial to a large variety of sectors. Deep learning technology has a wide range of applications. FPGA accelerators can boost the performance of deep learning technology, and thus accelerate numerous applications and services ranging from database management to artificial intelligence [59, 140]. Microsoft Brainwave project has developed a deep neural network architecture that can be synthesized on FPGAs to achieve ten to over thirty-five teraflops [41, 91]. Also, FPGA accelerators can help speed up heavy computation tasks on video classification and genome analysis, as these algorithms have a tremendous amount of parallelism that can be exploited [31, 119, 130]. FPGA accelerators that provide over ten times speedup in genome sequencing analysis are deployed on Amazon AWS F1 instances by Edico Genome [42]. FPGAs can also enhance database management systems. In particular, set-oriented queries in database systems are suitable for FPGA computation, as a high degree of parallelism exists in set data queries [95]. More complex analytic operations of data have been accelerated by FPGA platforms tremendously [121]. *Bing* is currently powered by FPGA accelerators, which offer a 50% improvement in throughput and a 25% reduction in latency [92].

Table 2.	Comparison	between clo	ud security,	FPGA :	security, ar	nd cloud I	FPGA secu	rity.
					12			

	Assets Under Attacks	Threat Models	Physical Accesses	Programmable Hardware
Cloud Security	Data	Cloud & Clients	N	N
FPGA Security	Data & H/W Design	H/W Users & H/W Design Supply Chain	Y	Y
Cloud FPGA Security	Data & H/W Design	Cloud & Clients & H/W Design Supply Chain	N	Y

Building programmable hardware in the clouds improves the performance of cloud-hosted services significantly. However, this integration opens a new attack surface from an attacker's perspective. This is because FPGAs allow users to implement custom logic on them, unlike CPUs, and GPUs. A variety of attacks have been demonstrated in recent research papers [115, 142], and researchers are developing countermeasures to thwart the attacks on cloud FPGAs [81, 105]. This paper surveys the broad landscape of cloud FPGA security research. It summarizes the state-of-the-art research and points out future research directions.

We organize the whole paper in a way that it answers four fundamental research questions in cloud FPGA security research one by one:

- (1) What are the security threats when FPGAs are introduced in a cloud platform?
- (2) In what different ways can a malicious user attack an FPGA in the cloud?
- (3) How to defend against such attacks on cloud FPGAs?
- (4) How can we use FPGAs as a tool to enhance cloud security?

To better understand the differences between cloud security, FPGA security, and cloud FPGA security, we create Table 2 to show the comparison. Most importantly, the threat models of these three security research areas are different, and cloud FPGAs have the largest attack surface. In general, in the scenarios of cloud computing (cloud security and cloud FPGA security), we do not assume that users (either attackers or victims) have physical access to the computation resources. Additionally, traditional cloud security research does not assume that the underlying hardware can be maliciously altered by attackers (except the case of hardware Trojans). But with programmable hardware in the clouds, an attacker can create a hardware foothold in the system to launch attacks that were not possible before, e.g., side-channel attacks. In terms of the assets that defenders need to protect, hardware designs on FPGAs are valuable targets for FPGA security and cloud FPGA security attackers, in addition to the data that is computed or stored on the devices.

**Organization.** We introduce the background knowledge and the threat models of cloud FPGAs in Section 2 and Section 3, respectively. We survey the literature on attacks for a variety of threat models in Section 4. As there is a vast amount of research on power-based side-channel attacks and ring oscillator (RO) design variants, we provide the two case studies in Section 5. We discuss the countermeasures against the above attacks in Section 6. Researchers have introduced various methods to use FPGAs to enhance system security (i.e., the security of cloud computation), which is presented in Section 7. The recent related surveys and the differences between our paper and other surveys are discussed in Section 8. We share our thoughts on future challenges and provide concluding remarks in Section 9. We categorize existing research on attacking or protecting cloud FPGAs in Table 3 as a systematic review.

### 2 BACKGROUND

### 2.1 Field Programmable Gate Arrays

FPGAs are integrated circuits composed of programmable blocks, allowing a user to program the circuit functionality as needed even after fabrication. Fig. 1 shows a typical architecture of an FPGA. The architecture includes an array of configuration logic blocks (CLBs), switch boxes (SBs), and input/output pins. CLBs are composed of lookup tables (LUTs), flip-flops, and multiplexers. Each CLB can be programmed to implement any Boolean function with *n* or fewer inputs, where *n* is the input size of the LUT. The SBs in an FPGA can be configured to connect CLBs, so multiple CLBs can jointly construct a larger circuit and thus perform more complex computation. Input/output pins connect an FPGA with the outside world, such as power supply, clock signals, and other peripherals.

			Threat model				Attack class							
												acks		
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	ks	Ises	ls	nan	vid	toc	t da	ft	tan	chai	inje	l-ol	Iam	t cf
	tac	efer	onc	o-te	prc	GA	rec	the	gic	de-c	ult-	enia	Hwe	Iove
Papers	A	Ď	0	Ŭ	П	FF	Ď	Ы	Lc	Si	Fa	Ď	Rc	Ŭ
Huffmire et al. [68]		$\checkmark$		$\checkmark$	$\checkmark$		$\checkmark$			$\checkmark$				$\checkmark$
Note <i>et al.</i> [98]	$\checkmark$		$\checkmark$					$\checkmark$						
Endo <i>et al.</i> [38]		$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$						$\checkmark$			
Benz <i>et al.</i> [21]	$\checkmark$		$\checkmark$					$\checkmark$						
Gnad <i>et al.</i> [55]	$\checkmark$			$\checkmark$								$\checkmark$		
Schellenberg et al. [115]	$\checkmark$			$\checkmark$						$\checkmark$				
Gnad <i>et al.</i> [56]		$\checkmark$		$\checkmark$	$\checkmark$					$\checkmark$	$\checkmark$	$\checkmark$		$\checkmark$
Schellenberg <i>et al.</i> [116]	$\checkmark$			$\checkmark$						$\checkmark$				
Hategekimana <i>et al.</i> [63]		$\checkmark$		$\checkmark$			$\checkmark$							
Yazdanshenas et al. [139]		$\checkmark$		$\checkmark$			$\checkmark$							
Zhao <i>et al.</i> [142]	$\checkmark$			$\checkmark$						$\checkmark$				
Krautter <i>et al.</i> [83]	$\checkmark$			$\checkmark$							$\checkmark$			
Ramesh <i>et al.</i> [107]	$\checkmark$			$\checkmark$	$\checkmark$					$\checkmark$				$\checkmark$
Bag <i>et al.</i> [16]		$\checkmark$	$\checkmark$					$\checkmark$						
Provelengios et al. [105]		$\checkmark$		$\checkmark$							$\checkmark$	$\checkmark$		
Tian <i>et al.</i> [124]	$\checkmark$				$\checkmark$									$\checkmark$
Sugawara <i>et al.</i> [120]	$\checkmark$			$\checkmark$	$\checkmark$					$\checkmark$	$\checkmark$	$\checkmark$		$\checkmark$
Alam <i>et al.</i> [3]	$\checkmark$			$\checkmark$							$\checkmark$			
Weissman <i>et al.</i> [131]	$\checkmark$			$\checkmark$									$\checkmark$	
Krautter <i>et al.</i> [81]		$\checkmark$		$\checkmark$	$\checkmark$					$\checkmark$	$\checkmark$	$\checkmark$		$\checkmark$
Krautter <i>et al.</i> [82]		$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$					$\checkmark$				$\checkmark$
Mahmoud <i>et al.</i> [87]	$\checkmark$			$\checkmark$							$\checkmark$			
Gnad <i>et al.</i> [54]	$\checkmark$				$\checkmark$									$\checkmark$
Elnaggar <i>et al.</i> [37]	$\checkmark$	$\checkmark$		$\checkmark$			$\checkmark$		$\checkmark$					
Gravellier <i>et al.</i> [57]	$\checkmark$			$\checkmark$						$\checkmark$				
Provelengios et al. [106]	$\checkmark$				$\checkmark$									$\checkmark$
Giechaskiel <i>et al.</i> [49]	$\checkmark$				$\checkmark$									$\checkmark$
Giechaskiel <i>et al.</i> [48]	$\checkmark$				√									√
Giechaskiel <i>et al.</i> [52]	$\checkmark$				$\checkmark$									$\checkmark$
Luo <i>et al.</i> [86]		~			$\checkmark$									√
Matas <i>et al.</i> [90]	√	$\checkmark$		$\checkmark$	,					$\checkmark$	$\checkmark$	$\checkmark$		√
Giechaskiel et al. [50]	$\checkmark$				$\checkmark$									√
Giechaskiel <i>et al.</i> [51]	~				$\checkmark$									$\checkmark$
Glamocanin <i>et al.</i> [53]	√			$\checkmark$					,	$\checkmark$				
Krieg <i>et al.</i> [84]	$\checkmark$					$\checkmark$			$\checkmark$					$\checkmark$

# Table 3. Categorization of cloud FPGA literature based on (1) threat model, (2) attack class, and(3) whether the study is about attack or defense or both.



Fig. 1. An FPGA has Configuration Logic Blocks (CLB), switch-boxes (SB), and input/output cells. Each CLB consists of a Look-Up Table (LUT), a flip-flop (FF), and a MUX.

### 2.2 FPGA Design Flow

Fig. 2 shows the typical FPGA design flow. A designer designs the target system in terms of Hardware Description Language (HDL) codes, e.g., Verilog HDL or VHDL. After the HDL codes have been simulated and verified for correctness, they are synthesized and translated to a netlist by FPGA synthesis tools (e.g., Xilinx Vivado [135] or Xilinx ISE [134]). The netlist describes how the hardware components, such as LUTs and registers, are connected. The FPGA synthesis tool then maps the component are optimized to meet the timing constraints and other physical constraints given by the user. The end goal of the design process is a bitstream file, which is a string of 0s and 1s. After the bitstream file is loaded onto an FPGA, the FPGA will function as intended by the user.

To reduce the design time and the verification efforts, a designer can specify the design using a high-level language (e.g., C or MATLAB). This also allows a developer, who does not have



Fig. 2. FPGA design flow: The yellow box indicates that the step inside that box is optional. The blue box shows the steps which give a HDL code as an output. The grey box indicates synthesis of the HDL code and its translation. The red box shows the mapping of the logic to LUTs, the placement and routing of LUTs, and the timing analysis step. The purple box indicates the steps to generate the final bitstream followed by programming the FPGA.

the required expertise in writing HDL codes, to use FPGAs for his/her need. This alternative is called High-Level Synthesis (HLS), and it can compile high-level programming language code to a functionally equivalent HDL code. Xilinx Vivado HLS [135] and Intel High-level synthesis compiler [70] are examples of tools which provide this functionality. The FPGA synthesis tool processes the HDL code and creates a bitstream file used to program the FPGA.

The above two programming methods are available to the users of cloud FPGAs. So the users can either submit their hardware design as HDL codes or as a high-level language program. A user, even without much knowledge of hardware design, can start from a high-level language and run an HLS tool locally to create HDL codes for uploading to the clouds. The cloud service provider takes the source codes of user designs and integrates user logic with their IP cores (called shell on Amazon platforms) to build a bitstream file. This bitstream file is then loaded on an FPGA. In the current commercial setting, the cloud provider has full control over the compilation and deployment of user logic as it has to happen in an Amazon cloud node [13].

### 2.3 Architecture of FPGA clouds

Fig. 3 depicts a typical architecture of a cloud platform with FPGAs. FPGA boards are connected with the servers using PCIe wires. PCIe wires are the de facto standard for the communication between a server and the FPGA in commercial FPGA clouds [101]. The cloud service providers divide the programmable resources on an FPGA into two parts: (1) the area for implementing the shell, and (2) the area where users can implement customized logic. The shell includes Peripheral Component Interconnect Express (PCIe) modules, DDR4 DRAM controllers, and control modules, to enable the communication with the servers and DRAM. In Amazon EC2 F1 instances, one out of



Fig. 3. Architecture of an FPGA in the cloud. The four different threat models considered in this paper are (1) malicious cloud providers, (2) malicious co-tenants, (3) malicious IP providers, and (4) malicious FGPA toolchain. These are indicated in the figure by devil icons in the shell (PCIe module and IP core), user 1's logic, 3rd party IP core, and the FPGA design flow, respectively.

four DDR4 DRAM controllers is implemented in the shell, and the other three can be implemented in the customized logic [14]. Typically, the cloud provider's logic (shell) interacts with user logic via Advanced eXtensible Interface (AXI) protocols [14]. On the CPU side, the software development kit provides the application programming interfaces (APIs), so the users with little FPGA experiences can still interact with FPGAs easily [12]. In the modern commercial clouds like Amazon EC2 F1, an FPGA is not allowed to be shared by multiple users due to security concerns [18]. However, researchers envision that multi-tenant cloud FPGAs will be realized soon, as it is more cost-effective for both the cloud providers and the users to share resources. Also, the security of multi-tenant cloud FPGAs is an active research area. Thus we will survey recent works on the attacks and defenses on multi-tenant FPGAs as well.

### **3 THREAT MODELS**

To understand the possible threats posed to the cloud FPGA users, we categorize the threat models into four types: (1) malicious cloud providers, (2) malicious cloud users/co-tenants, (3) malicious IP providers, and (4) malicious toolchains. Fig. 3 illustrates where the threats reside in the architecture of an FPGA cloud.

**Malicious cloud providers.** In the early days of cloud security research, one of the leading security concerns of users was the privacy of their data stored/processed in the clouds [9, 27]. In traditional threat models of cloud security, the cloud service providers are generally assumed to be untrustworthy, so a user needs to implement his/her security measures to protect him/herself in the clouds. Additionally, the users on the same cloud platform can be a threat to other users, too. However, a malicious cloud model is stricter than the malicious user model because a cloud provider has all the privileges to the platform, including physical access and full control of the computation resources. A typical defense against malicious cloud providers is the use of fully-homomorphic encryption [46, 128].

Fully-homomorphic encryption allows computation on encrypted data. Users can encrypt their private data on their computers and send the encrypted data to the cloud. Computation on the encrypted data is performed in the cloud. After the computation, the cloud sends the result back, still in the encrypted form. The user decrypts the encrypted result and gets the result of the computation on his/her private data. As the computation on the cloud is performed completely on encrypted data, the cloud provider is unable to extract any secrets in the user data. Fully-homomorphic encryption is a good way to eliminate the requirement of a trusted cloud. However, it is computationally intensive, and it can take hundreds or even thousands of seconds to complete the bootstrapping operation, which is the most important operation to realize fully-homomorphic encryption schemes [47, 109]. Researchers are developing new encryption [17, 26, 47]. Also, people have incorporated the homomorphic encryption techniques into secure processor architecture designs as well [127].

**Malicious co-tenants.** Besides the security threats from a malicious cloud provider, threats from malicious users/co-tenants need to be considered. The basic principle of cloud computing is that all the users can dynamically have a share of the large computation resource pool. Due to this, a victim user can be allocated close to a malicious user. Moreover, the victim and the malicious user might even share some computation resources. Although, in general, the computation resources used by different users are logically isolated, the computation resources are likely to be physically connected due to the shared hardware platform. Attackers can leverage such a shared hardware platform to perform a variety of attacks such as side-channel attacks, fault-injection attacks, and establishment of covert channels, which are discussed in the following sections of the paper.

Moreover, the business model of cloud computing pushes the economically-motivated cloud service providers not to act maliciously. Thus, a modern trend in cloud computing research is to consider cloud providers as partners of the users [2]. These providers help protect the security of their customers. For example, cloud providers can apply moving target defense strategies to actively migrate virtual machines within their computing infrastructures [94]. This bounds the side-channel information leakage as the attacker has to find the new location of the victim before it can carry on the side-channel attack.

**Malicious IP providers.** The modern hardware design process is very complicated and timeconsuming. Practitioners need to integrate 3rd-party intellectual property (3PIP) cores to speed up the development process. This gives attackers a leeway to introduce malicious IPs, and the IPs can be exploited later to leak information, e.g., via covert channels [48, 49, 51, 54, 124]. This threat requires the attacker or the attacker's logic to be present in the proximity of the target FPGA fabric. Thus, the attacker can collect leaked information. So, either the cloud provider or a cloud co-tenant has to be malicious as well. However, the vulnerabilities are introduced in the design phase of the victim system, so we consider it as a separate security threat. This security threat is similar to those in the untrusted supply chain of electronics [58, 111] and Trojan insertions in pre-silicon hardware [62, 77]. Due to this, the usual countermeasures, such as hardware Trojan detection tools [61, 114], can be implemented to detect malicious hardware design and IP cores which leak information through their digital output channels. However, novel covert channel communications enabled by a cloud FPGA environment require the immediate attention of the cloud providers and customers. Such covert channel communications are discussed in more detail in Section 4.

**Malicious FPGA tools.** Adversaries can reverse-engineer commercial FPGA design tools and embed malicious functionalities in the toolchain. This way, malicious tools can alter the compiled hardware design. Under this threat model, the adversary can inject Trojans in a design. This maliciously-altered design behaves functionally and formally equivalent to the original design throughout the design flow until the tool writes the design as a bitstream configuration file [84].

### 4 ATTACKS

Having explained the threat models in the context of cloud FPGAs, we turn our attention to different attacks proposed by researchers. These attacks are grouped according to their threat models.

### 4.1 Malicious Cloud Providers

**Direct sensitive data leakage.** In a cloud without programmable hardware, all the computation and the data are contained in one container (virtual machine). Each container is isolated from another in the hypervisor layer. In the case of a cloud with programmable hardware attached, an attacker with system privilege can tamper with the logic or tap the communication between the FPGA fabric and the processor. This can enable him/her to steal the secret data. In current commercial FPGA-enabled clouds, the FPGA boards connect to the processors via the PCIe protocol. Thus, the cloud provider can intercept the communication between the FPGA boards and the processors with ease.

**Intellectual property theft [21, 98].** The most common use of cloud FPGAs is to implement hardware accelerators for specific computation tasks. The IP of such an accelerator developed and owned by a developer should be protected. Since the developer hands over the bitstream files of the IP cores to the cloud providers, a malicious cloud provider can access the RTL design of the IP core. Bitstream reverse engineering techniques can enable this [21, 98]. Thus, a malicious provider can steal the design IP and replicate the accelerator on another FPGA.



Fig. 4. Remote power analysis attack for a multi-tenant FPGA [115]. The side-channel analysis (SCA) is performed through the power distribution network (PDN) in spite of the logical isolation between the victim logic and the sensor.

**Tampering with user logic**. A malicious cloud provider can access the user's RTL design. So, during the integration of the user's design with the shell in the cloud FPGA, the providers can introduce malicious modifications in the design. This security threat is also known as hardware Trojans that have been studied for decades [132]. On cloud FPGAs, the Trojans can leak sensitive information, which has been protected by other schemes in traditional cloud computing platforms. Also, the Trojans can sometimes be inserted automatically [74]. One of the future challenges is to provide a remote attestation feature which allows a remote user to verify the integrity and authenticity of his/her designs in a cloud FPGA. This feature might be similar to the remote attestation provided by Intel SGX [33].

### 4.2 Malicious Co-Tenants

In a multi-tenant FPGA model, many users, including potential adversaries, will share the same FPGA fabric. As the multi-tenant model allows a malicious user to implement his/her design close to a victim, recent research has focused on the security concerns in multi-tenant FPGAs. In particular, remote side-channel attacks [115, 142] and remote fault-injection attacks [3, 87] have been demonstrated. In this subsection, we survey the existing works on how a malicious co-tenant can use the programmable logic on a cloud FPGA to launch attacks. Note that an adversary can launch these attacks without any administrative privileges.

**Side-channel attacks.** The attack methods that exfiltrate information that is not leaked through standard digital output channels are called side-channel attacks. Power side-channel [79, 89], timing side-channel [28, 78], electromagnetic side-channel [29, 43], and photonic-emission side-channel [80, 117] are a few examples of side-channels. An attacker must collect the side-channel information of victim devices in these attacks. Hence, researchers have believed for a long time that the side-channel attacks can be launched only by the attackers with physical access to the devices. However, the ability to program the hardware deployed in the cloud is similar to having physical access to the device. This allows the attackers to monitor the side-channel information remotely in the physical environment, as shown in Fig. 4. The power consumption of a victim logic disturbs the power distribution network on the FPGA, and measuring this disturbance allows the attacker to

estimate the power consumption of the victim. Remote power-based side-channel attacks have been demonstrated in the literature [115, 142]. Moreover, crosstalk between FPGA *long* wires (a specific type of routing resource on FPGAs) can also serve as a method to leak information [107]. Since this is an active research area, we provide a detailed survey on side-channel attacks in Section 5.

**Fault-injection attacks.** In fault-injection attacks, an attacker injects faults in the execution process of a computation task. Thus, the device produces wrong outputs at the output ports. This problem can have severe implications in a cryptographic system. In such a system, faulty outputs can lead to a successful recovery of the secret key in the system [60]. Traditionally, an attacker injects faults by manipulating power or clock signals, or by electromagnetic pulses. These methods require physical access to the target device. However, using FPGAs shared with a victim, an attacker can build an on-chip fault injector and tamper with the computation of the victim.

To demonstrate a successful fault-injection attack on multi-tenant FPGAs, Krautter *et al.* implemented a large number of ROs and program them to oscillate at a very high frequency [83]. Because the power distribution network is shared among all tenants on the same FPGA fabric, by toggling the ROs, the attacker can manipulate the propagation delay in the whole chip. Thus, timing violations can occur in the circuit, causing faulty results in the computation. By triggering timing violation on the FPGA, Krautter *et al.* injected faults in an AES process running on the same chip. Note that this does not require any physical or logical connection to the attacker's circuit [83]. Since the high oscillation rate may increase the power consumption drastically, the chip may have to be shut down due to excessive heating. This problem can be addressed, as explained next.

Mahmoud *et al.* improved the fault-injection attack by proposing a delay-sensing circuit. This delay-sensing circuit fine-tuned the parameters of the ROs such that the ROs draw enough power to slow down the target circuit, but not so much that the chip shuts down [87].

Building ROs is not the only way to generate huge power consumption on an FPGA. Alam *et al.* introduced a new way to inject faults in multi-tenant FPGAs remotely. By repeatedly triggering memory writing collision (writing to the same address simultaneously in a dual-port RAM with opposite values), the attacker can create short circuits in the RAM [3]. This results in massive power consumption in the chip. By exploiting this phenomenon, one can launch a fault-injection attack on an FPGA chip. This attack is stealthier than RO-based attacks because the memory collision can be created during runtime. Such mechanisms, which trigger faults during runtime with unsuspicious circuits, cannot be detected by a bitstream analysis tool, unlike RO based methods, because bitstream analysis tools can detect ROs. Moreover, a dual-port RAM is a common design component in modern hardware system design, which makes the attack more powerful.

**Denial-of-service attacks.** One property of concern for both the cloud providers and the users is the availability of the cloud platform. Denial-of-service (DoS) attackers target the availability of this platform. On an FPGA+CPU heterogeneous cloud, an attacker can launch a remote DoS attack on the FPGA [55]. By programming a malicious circuit that switches on and off frequently, a significant voltage drop is created on the FPGA, and the FPGA shuts down to protect itself. An FPGA shut down by voltage emergency requires manual power-cycling of the device.

Matas *et al.* further optimized the RO-based DoS attack by showing how to find the shortest path on an FPGA to form malicious (fastest oscillating) ROs [90]. They used GoAHEAD, a tool for implementing partial reconfiguration of FPGAs, to search for the optimal paths [20]. The attack, when implemented on a Xilinx Alevo U200 datacenter card with 1.182 million LUTs, can potentially waste over 2kW power, which is way beyond the power budget of any FPGA [90].

**RowHammer attacks.** Interestingly, in an FPGA+CPU heterogeneous system, the FPGA has a unique privilege to access the DRAM without being detected by any monitoring mechanism in the



Fig. 5. An illustration of power covert channels among CPU, GPU, and FPGAs that share the same power supply unit [50]. Note that this attack does not even require the components to share the same power distribution network.

CPU. Also, the FPGA can bypass the cache in the processor and launch a rowhammer attack (i.e., flipping the bits in DRAM by repeated accesses) twice as fast as the traditional rowhammer attack launched by a CPU [131]. Consequently, the rowhammer from an FPGA to a DRAM can trigger four times as many bit-flips as the CPU initiated attacks. By exploiting this vulnerability, one can tamper with the data and possibly the control flow of the program in the system.

### 4.3 Malicious IP Providers

To design a complex modern system, designers usually need to integrate third-party IP cores into their systems. While these third-party IP cores can provide excellent performance and reduce the time to market, they can be security threats to the system. If a malicious IP is introduced in the system, it can leak information or tamper with the computation and the data in the system. Researchers have studied this topic for decades as hardware Trojans. Interested readers can read other survey papers focusing on hardware Trojans [23, 77, 132]. The unique challenge for exploiting Trojans in the cloud FPGAs is how to leak the information stealthily, which is also called covert channel communication. In the remainder of this subsection, we present how a Trojan circuit can generate side-channel information to send out secrets to a malicious listener. In particular, we show how one transmit over power, crosstalk in *long* wires, and thermal channels.

**Power covert channels.** The idea of voltage manipulations used in power side-channel attacks can be extended to establish covert channels on multi-tenant FPGAs. An example of this is the work done by Gnad *et al.* in [54]. They have demonstrated high-speed covert-channel (8MBit/s) communication. The transmitter of the covert channel uses ROs to generate measurable voltage spikes according to the secret data to be transmitted. The receiver, which is another tenant on the same FPGA chip, uses another set of ROs to measure the voltage spikes. The attacker designs both the transmitter and the receiver. This enables the attacker to modulate the transmitted signal leading to robust communication, which can work in the presence of environmental noise introduced by other tenants on the same FPGA fabric.

Establishing such power covert channels can be challenging if the receiver and the transmitter are on separate dies. However, Giechaskiel *et al.* demonstrated such an attack on cloud FPGAs in [49]. They established a power covert channel on cloud FPGAs that are on separate dies. They use Xilinx UltraScale+ FPGAs for this. UltraScale+ FPGAs used by cloud providers like Amazon and Huawei have three distinct dies that are connected and powered through a silicon interposer. Thus, even though the receiver and the transmitter are on separate dies, they still share the same power supply through the silicon interposer. A successful covert channel, operating at more than 4.6Mbps



Fig. 6. Establishment of a communication channel using *long* wires in Xilinx FPGAs [51]. The H and the L on the receiver stand for high and low delay values respectively.

with an accuracy of over 97.6%, is established in such a setup. Moreover, they showed that the channel is present for all combinations of the three dies as receiver and transmitter.

Sharing a power supply unit in a computing system (e.g., one cloud computing instance), as shown in Fig. 5, allows malicious attackers to create a covert channel between FPGA boards, and even from a CPU or a GPU to an FPGA [50]. The authors demonstrated that by creating fluctuations in the supply voltage provided by a shared power supply unit, an attacker can send information stealthily to a sink FPGA, which is actively monitoring its voltage by using ROs. The attacker used high power consumption of the source device (FPGA/CPU/GPU) to indicate a logic 1, and low power consumption to represent a logic 0. However, one cannot simply use the absolute RO frequency on the sink FPGA to find out the message sent from the source reliably. This is because the power supply units and voltage regulators on the sink board can tolerate voltage fluctuations to some extent. To solve this problem, Giechaskiel *et al.* implemented stressor ROs on the sink FPGA to drain extra power, so the voltage change in the supply voltage can be more measurable on the sink FPGA. Also, the authors introduced a new metric to detect the power consumption changes on the source device more reliably. According to an evaluation on Artix 7 boards, this covert channel can achieve a bandwidth of 6.1bps with over 90% accuracy. Similarly, a CPU or a GPU can switch between high and low workload to send bits over the same covert channel to an FPGA.

Crosstalk in long wires. Crosstalk phenomenon in long wires can be exploited to launch covertchannel communication as well [51]. The attacker is assumed to have a malicious IP core as a part of the victim logic. It is also assumed that the attacker's logic is on the same FPGA fabric and is placed close to the victim's logic. Since the adversary is the designer of the IP core, he/she can define the internal placement and routing of his/her blocks. Thus, the attacker can force his/her cores to use specific routing resources, in particular long wires. The attack, illustrated in Fig. 6, exploits the phenomenon that the delay of FPGA long wires depends on the logical state of nearby wires. In particular, when the transmitter wire (the long wire in the victim design) carries a logic 1, the delay of the nearby receiving wire (the *long* wire in the attacker's design) is lower than it would be if the transmitter wire carried a logic 0. An RO involving the receiver long wire can measure the delay of the receiver wire. This reveals the logic state of the nearby transmitter long wire. Thus, a covert-channel is created for attackers to leak sensitive information from a victim hardware design. This covert channel can work effectively, even in the presence of power and temperature fluctuations. More importantly, the malicious IP core in the victim's logic provides legitimate functionality while acting as a Trojan, and it does not contain additional logic. This makes it challenging to detect such a Trojan using current Trojan detection tools [61, 114]. It is worth noting that this attack mechanism does not depend on the rate at which the signals switch.



Fig. 7. Establishment of thermal covert channel on cloud FPGA [124]. The transmitter uses 4 FPGAs simultaneously and sends the binary string 0101 in this example. The orange color of the FPGAs after the heating period represents high temperature. The yellow color of the FPGAs after the reconfiguration period on the receiver side represents a temperature higher than the un-heated FPGAs, but lower than the heated FPGAs.

In fact, even when the signal in the transmitter wire is static, the attacker can differentiate between a logic 0/1 on the wire.

Giechaskiel *et al.* extended the idea of [51] in [48]. They investigated a setup with multiple transmitters and a single receiver in detail. They considered two configurations of the relative placement of the transmitters and the receiver: (1) the two transmitters are on the same side of the receiver (RTT) and (2) the receiver is sandwiched between the transmitters (TRT). In RTT, the transmitter closest to the receiver affects the RO frequency on the receiver. In the TRT configuration, both the transmitters have a roughly equal effect on the RO frequency of the receiver. An attacker can use the TRT configuration to increase the bandwidth or to reduce errors in transmissions.

The effect of crosstalk in *long* wires was characterized in [106]. To perform this characterization, the authors proposed a new metric to capture the difference in the periods of the RO for the cases when the transmitter value is 0 and when it is 1. This helps remove the variability in the individual ROs. Experiments showed that this new metric is successful in removing the dependence of the characterization metric on the RO frequency. Hence, it can characterize the leakage more accurately.

A similar characterization effort for cloud FPGAs was made in [52]. The main challenge in performing this analysis on the cloud FPGAs is the restriction imposed by some cloud providers on the users' designs. Providers like Amazon prohibit combinatorial loops [8]. To bypass this checking on the Amazon cloud, researchers introduced two RO designs in [52]. These RO designs are described in Section 5.2.

**Thermal covert channel.** Most of the covert channels in the literature require the designs of attackers and victims to be present on the same FPGA chip, i.e., a multi-tenant FPGA setup. However, cloud providers have not adopted the multi-tenant FPGA model yet. There exists a covert channel on the cloud FPGAs which does not require a multi-tenant setup. The covert channel described by Tian *et al.* in [124] is an example. It exploits the temporal sharing of a single FPGA. This channel can transmit data stealthily on a single-tenant cloud FPGA. The transmitter heats an FPGA by operating many ROs. Then, the transmitter turns off the ROs, leaves the cloud, and the receiver uses the same FPGA. The receiver can measure the temperature of that FPGA with ROs. This is possible because the frequency of an RO depends on the temperature of the FPGA.

of such a thermal covert-channel depends on the number of FPGAs used simultaneously. Fig. 7 illustrates how a binary string can be transmitted and received by the temporal sharing of four cloud FPGAs simultaneously. This covert channel was demonstrated on the cloud FPGAs in Texas Advanced Computing Center in [124].

### 4.4 Malicious FPGA Tools

Users expect that a legitimate vendor provides the FPGA design tools. However, if an attacker can inject malicious functionalities into the toolchain, a malicious bitstream and hence, malicious hardware can be built on the cloud FPGAs [84]. The malicious modification in the compiled design does not show up in the output until the bitstream is generated. Hence, the intermediate output files, such as post-place simulation netlists are formally equivalent to the original design. The attacker activates the malicious functionality only when the bitstream is being generated. The malicious FPGA tool first replaces the functional blocks with their malicious counterparts. Then, in the bitstream generation process, the design tool looks for these special malicious LUTs. If the tool finds these malicious LUTs, it reconfigures them to activate the Trojan. The authors demonstrate a privilege escalation attack using this malicious design flow on the free and open-source Lattice iCE40 design flow [84].

#### 5 CASE STUDIES

In this section, we detail the recent research on two popular topics: (1) remote power side-channel attacks on cloud FPGA systems and (2) variants of RO designs on FPGAs, as a building block in many attacks, to bypass the design restrictions enforced by cloud providers.

#### Remote power side-channel attacks 5.1

Security researchers have studied power side-channel attacks extensively in the past decade [79, 89]. An attacker can exploit the fact that the data that the system processes affects the dynamic power consumption of the system [79]. So, by observing the power consumption of the circuit, the attacker can infer the secret key in the cryptographic hardware. This attack requires side-channel information to be collected from the hardware. Consequently, it was believed that such attacks could be carried out only if the attacker had physical proximity to the target system. However, in the context of cloud FPGAs, a malicious user does not have physical access to the target FPGA. Hence, all previous techniques would not work. This leads to recent works on remote power analysis. We discuss those in this sub-section.

Threat model. In general, remote power analysis attacks assume that the adversary's logic and the victim's logic are on the same remote FPGA fabric [115, 142]. So, the adversary has access to some of the LUTs in the remote FPGA. In other words, the attacker can implement his/her logic on some part of the shared multi-tenant remote FPGA. Although currently, the cloud FPGA providers do not allow sharing of an FPGA by multiple users, as explained in Section 2, it is envisioned that multi-tenant FPGAs will be realized soon for better efficiency in terms of cost and utilization.

Key idea. To launch a remote power analysis attack, an attacker has to implement a power monitor on the FPGA fabric shared with the victim. For example, the attacker can monitor the power consumption of a victim process by using time-to-digital converter (TDC) sensors. Using the power traces collected by the on-chip power monitors, the attacker can perform a power side-channel attack.

Attack method. A key component in the attack is the power distribution network (PDN) on FPGA chips. The PDN handles the distribution of power to all the components on the FPGA [10]. The PDN



Fig. 8. Illustration of a TDC sensor that uses a chain of buffers with latches to measure delay.

spans across different abstraction levels, from printed circuit board level to individual transistors on the FPGA. The PDN consists of resistive, capacitive, and inductive elements in the form of a power mesh. The power consumption of an FPGA chip at any instant depends on the logic that is being operated at that time. The changes in logic values affect the voltage and current drawn by the transistors in FPGA. These voltage fluctuations affect the delays of the other logic circuits implemented on the same FPGA due to the shared PDN. Hence, measuring delays in one part of the FPGA reveals information about power consumption in a different part of the FPGA. In particular, the higher the fluctuations in the voltage, the higher is the change in the delays. So, the attacker can monitor the power fluctuations on the FPGA by implementing appropriate delay sensors.

To this end, the attacker can implement a TDC, illustrated in Fig. 8, on the shared FPGA as a delay sensor [115]. As the delays of the buffers in the TDC depend on the supply voltage, the change in delays can be monitored as a proxy for voltage fluctuations. When a victim process becomes active in a different region of a multi-tenant FPGA, it disturbs the PDN. This results in a change in the delay values of the TDC sensor. Thus, the attacker can create a mapping between the power traces and the delay values. This mapping can then be used to perform a standard Correlation Power Analysis (CPA) attack. Such an attack was demonstrated in [115]. The proof of concept for this attack was demonstrated on a victim AES core operating at 24MHz on a Xilinx Spartan-6 FPGA. Two scenarios were considered: (1) when the sensor is placed close to the victim AES logic, with a gap of just 4 FPGA slices, and (2) when the sensor is placed far from the AES core. In both cases, the attacker can recover the AES key.

Alternate power sensors. As a different approach, Zhao *et al.* used ROs as power sensors to monitor the power consumption on the FPGA [142]. They translated the frequencies of ROs into the power traces based on a linear relationship. A remote power side-channel attack was shown to be successful using this RO sensor setup.

Attacking the processor system. In an FPGA+CPU heterogeneous chip, like a Xilinx Zynq system, an ARM processor system (PS) shares the PDN with the FPGA fabric (programmable logic or PL). Zhao *et al.* demonstrated an attack that uses the PL to monitor the power consumption of the PS [142]. By doing so, they recovered the control flow of the program in the PS. This vulnerability made a simple power analysis on RSA possible. Similarly, an FPGA-to-processor correlation power analysis has been demonstrated in [57]. The authors used a TDC on the FPGA to measure the power traces of the processor. Using that, they attacked an AES core running on the processor with 111k to 127k power traces.

**Cross-chip attacks.** Using the remote power side-channel attack, an attacker can not only attack the victim who is on the same chip as the attacker, but he/she can also launch a cross-chip attack. This cross-chip attack works as long as two FPGA chips are sharing the same power supply on the same board [116]. Due to the victim being on a separate chip, the attack is more challenging.



Fig. 9. Classical RO design (a), and its variants (b) and (c) [52].



Fig. 10. High switching activity components [81]: These designs are potential replacements for classical ROs in fault injection attacks since they incur high power consumption as well. The inverter and the XNOR gates in the grey boxes in (a) are preserved to add delay and generate clock glitches for the flip-flop. The circuit in (b) performs switching by using a high-frequency signal from the Phase-locked loop (PLL) as the clock of the flip-flop.

The number of traces required for this attack on AES is  $40 \times$  the number of traces required for the attack in [115].

**Experiments on Amazon clouds.** In DATE'20, Glamocanin *et al.* published their results on launching remote power side-channel attacks on AWS EC2 F1 instances [53]. They chose to use TDC sensors for measuring power consumption on a cloud FPGA, and the results showed that they could successfully break the secret keys of all 16 bytes of an open-source AES-128 core with  $5 \times 10^5$  traces. This result validated the feasibility of remote power side-channel attacks on a commercial cloud platform, so this research area raises serious concerns.

*Long* wire leakage. Ramesh *et al.* showed that it is possible to exploit the crosstalk phenomenon in *long* wires to extract a secret from a victim logic passively [107]. In the attack, the authors targeted an automatically placed-and-routed AES core. They identified a vulnerable *long* wire in the victim design, which carries secret information. This vulnerable *long* wire would act as the transmitter. The attacker is assumed to manually place-and-route a *long* wire in the receiver RO such that it is adjacent to the vulnerable (i.e., transmitter) *long* wire. After that, a side-channel attack based on the *long* wire leakage is conducted successfully. In this attack, the attacker does not need to modify the routing constraints of the victim logic. However, a successful attack relies on the fact that the FPGA tool has created a vulnerable design.

### 5.2 Ring Oscillator Designs and their Variants.

ROs are a crucial component in a variety of attacks [48, 51, 106, 107, 142]. So, we survey different RO designs and their variants that exist in the current literature.

Typically, an RO is composed of a self-looped chain of an odd number of inverters. Each inverter can be instantiated on a LUT in an FPGA, as shown in Fig 9. The reason why a variety of attacks rely on ROs is the sensitivity of the RO frequency to voltage and temperature fluctuations. However, due to the possible use of ROs in attacks, AWS implements a netlist checking tool and blocks users from implementing combinational loops (i.e., typical ROs) on their FPGAs. So, the basic design of

an RO has been extended to designs that use a latch or a flip-flop as a transparent component like a buffer [52]. Such designs are illustrated in Fig. 9 (b) and (c). An advantage of having sequential elements in ROs is that it can fool a bitstream or netlist checking tool into believing that the design does not contain a combinational loop. So, this technique can be used to hide the existence of combinational ROs in the design from the checking tools, as demonstrated in [52].

The above-mentioned RO design variants can be used to replace classical ROs in both sidechannel and fault injection attacks. Researchers have come up with different designs that can incur high switching activity, and thus imply a high power consumption [81]. These designs are shown in Fig. 10, and they can be used in fault injection attacks as power wasters. These designs have the oscillation property of an RO, but they are sequential circuits since a flip-flop is involved in the loop. The main design principle of high switching activity components is to toggle values as fast as possible. In the first design in Fig. 10, a self-clocked flip-flop is used, and the clock signal is generated by an XNOR gate which generates glitches. The second design in Fig. 10 uses a phase-locked loop (PLL) at its highest frequency to generate a high-speed clock. On an iCE40-HX8K FPGA, the current generated by 6000 combinational ROs and 6000 PLL based sequential oscillators in Fig. 10 (b) is measured to be 291.3 mA, and 240.9 mA, respectively [81]. Note that the sequential oscillator cannot consume as much power as combinational ROs because it cannot run as fast as a combinational RO. Still, the sequential design is powerful enough to launch fault attacks on FPGAs.

### 6 COUNTERMEASURES

Several researchers have proposed methods to counter the attacks mentioned in the previous sections [56, 81, 82, 105]. These methods can be classified broadly into two categories: defenses implemented by a tenant and defenses implemented by a cloud provider.

### 6.1 Untrusted Clouds

**Bitstream encryption.** One way to prevent bitstream reverse engineering is to encrypt the bitstream [133]. The encrypted bitstream is decrypted only on the FPGA. Many commercial FPGAs support this feature. However, so far, to the best of our knowledge, commercial heterogeneous cloud providers (e.g., Amazon EC2 F1) require users to submit RTL designs in plaintext [13]. The platform provider then integrates such a design with the shell (i.e., the PCIe modules and the control modules for communicating with the servers). Before the generated bitstream file is loaded onto an FPGA, the cloud platform providers check the design for prohibited design patterns like combinational loops. Thus, commercial clouds do not support bitstream encryption. Apart from this method, there are no perfect solutions to prevent bitstream reverse engineering.

Following the line of bitstream encryption, Bag et al. proposed a key management system to manage the bitstream decryption process on FPGA [16]. They combined the concept of "bring your own key" (BYOK) and key aggregate cryptosystem [100]. This way, the tenants can use their secret keys for encrypting their bitstreams locally and securely transfer the keys to the cloud FPGAs for decryption. A master public key provided by the FPGA vendor encrypts the encryption keys used by each tenant. The master private key is embedded in the FPGAs and can decrypt the secret keys of the users. These decrypted keys are then used for decrypting the corresponding encrypted bitstream files. A malicious cloud provider does not have access to the secret keys without using the FPGA, because the decryption for the individual secret keys occurs in the FPGA.

**IP watermarking.** IP watermarking is a technique that adds special modules into a hardware design (IP core). It should be difficult for an attacker to detect and remove the embedded watermarks. Moreover, the watermarks should be embedded such that the owner can prove the ownership of the design when an IP dispute occurs. For example, [85] encodes watermarks in the unused

LUTs in an FPGA, and the design is placed and routed around the watermark. As the location of the watermark is known only to the designers, an attacker cannot detect which LUTs contain the watermark bits. Some watermarking techniques incur extra area overhead to the design [85]. However, zero-overhead watermarking schemes exist. For example, one can modify the delay of non-critical paths in the hardware design through routing, such that the delay information can be considered as the unique watermark of the IP core [71]. Since this technique does not add any hardware components, it has no additional hardware area overhead.

**Traditional side-channel attacks and fault-injection protections.** When the cloud provider is untrustworthy, it is difficult for the user to protect him/herself against the cloud and the other malicious tenants. This is because the user has no control over and no idea about who and what will be sharing their FPGA, and he/she has to assume everyone else is potentially malicious to him/her. One conservative method to design a secure system against side-channel attacks and fault injection attacks is to follow the traditional security practices and assume that the attackers have physical access to the device. Researchers have studied side-channel attacks and fault-injection attacks for decades. We generally understand how to secure a hardware design against side-channel attacks (e.g., using masking or hiding principles [89]) and fault-injections (e.g., using fault-injection defections [38, 60]). However, to defend against such a strong physical adversary, the area and the performance overheads of the design are typically very high. Thus, these kinds of countermeasures may be an overkill for the scenario of cloud FPGAs, where the attackers may not be able to precisely measure the side-channel information and inject faults using the on-board malicious circuits. We are still seeking more efficient ways to secure the designs on cloud FPGAs, while not relying on the trustworthiness of the cloud providers.

### 6.2 Trusted Clouds

**Bitstream checkers.** If a cloud provider is trustworthy, a non-malicious user can be at an advantage, since the cloud provider can use the unique insights it observes from the whole platform to implement more powerful countermeasures. For example, the provider can implement a bitstream checker before programming an FPGA. This bitstream checker can identify malicious circuit structures and raise a red flag if any such structures are found. The provider can use this method of checking the bitstream to defend against side-channel attacks and fault-injection attacks. For instance, AWS does not allow a user to deploy ROs and combinational loops on their FPGAs [8].

Being one of the pioneers in this research direction, Gnad *et al.* built the first bitstream checker called *FPGA antivirus* [56]. It checks for the known patterns of malicious circuits. They identified one typical pattern for fault injectors and two different patterns for the sensor designs used in side-channel attacks. Previous research has demonstrated that a fault can be injected by voltage or current fluctuations on the FPGA fabric [83, 87].

Gnad *et al.* identified two characteristics of an on-board fault injector: (1) a large number of combinational loops, where the "largeness" threshold is determined empirically; (2) a common input to these combinational loops to synchronously toggle the behavior of the loop. The rationals behind these two characteristics are: (1) to launch a fault-injection attack, the attacker has to be able to control a circuit that can incur high switching activities and extremely high power consumption; (2) the large circuit has to be synchronically controlled, otherwise, the large power consumption will be flattened, so the current will not surge beyond the current limit of the FPGA.

There are two ways to launch power side-channel attacks on multi-tenant FPGAs. One uses ROs as sensors, and the other uses a time-to-digital converter (TDC) as a sensor [115]. Gnad *et al.* suggested two types of characteristics to identify the on-board sensors from bitstream files. To identify the RO sensors, they looked for combinational loops with output ports. To identify the

TDC sensors, they checked for timing violations on every wire. These checks for timing violations apply to other sensors that exploit timing violations as well. Even if a single bit is unstable during a voltage fluctuation, an attacker can use that bit to measure the delay on the FPGA.

Based on the patterns of malicious circuits mentioned above, one can catch all malicious circuits known by then. However, as the authors in [56] have noted, potentially, there are more ways to launch side-channel and fault attacks on-board. So, this pattern-based approach needs to be updated frequently to catch up with new attacks [56].

Soon after the original FPGA antivirus was built, Krautter et al. proposed new attack variants that can evade the detection of the original *FPGA antivirus* [81]. These new attacks rely on novel RO structures designed using sequential circuits [120], so analysis tools that look only for combinational loops cannot detect such RO structures. To keep FPGA antivirus up to date, Krautter et al. reformulated the necessary characteristics of potentially malicious circuits that can launch fault-injection attacks and side-channel attacks [81]. They concluded that to detect side-channel attacks, a bitstream checker needs to look for sensors that can detect delay changes on board. Thus, they identified three unique patterns of malicious circuits for side-channel attacks: (1) paths with timing violations; (2) unusual data to clock connections; and (3) ROs. Likewise, they also summarized the characteristics of malicious fault-injectors: (1) high current variation runtime behaviors; (2) a large number of synchronized elements; (3) hardware primitives which can oscillate, e.g., ROs. They combine static analysis and dynamic analysis in the new FPGA antivirus design. The static analysis checks the structural properties of the design, and the dynamic analysis looks for possible timing violation and estimates the power consumption based on real or random input stimuli. The updated FPGA antivirus, when evaluated on Lattice FPGA, can detect all known malicious circuits that can inject faults or observe side-channel information [81].

Similarly, Matas *et al.* presented another bitstream checker called *FPGADefender* [90]. *FPGADe-fender* relies on static analysis of bitstream. It looks for structural signatures of malicious circuits. This includes combinational loops with/without transparent latches, short circuits, antennas, large fan-outs, disallowed port and path usage, and latches.

To counter the security threats from malicious FPGA tools, the authors in [84] suggested using equivalence checking. This equivalence checking would reveal manipulations in the bitstream file. However, as bitstream formats are not publicly documented, it is hard for third-party verification tool vendors to offer solutions that prove equivalence. Thus, a call for open and publicly documented bitstream formats was made in [84]. However, even if the bitstream formats are publicly documented, as the design complexity increases, more sophisticated equivalence checking methods are needed.

One drawback of the bitstream checking approach is that the users need to rely on the cloud providers to check the bitstreams. If the providers can check the bitstreams, they can reverse engineer the designs submitted by users. This forces the users to trust the cloud providers.

Access control. On a trustworthy cloud, the provider can implement several defenses. For example, the provider can enforce proper access control policies between a processor and its hardware peripherals on an FPGA. Elnaggar *et al.* introduced a new security threat on a partially reconfigurable FPGA. They assume that the reconfiguration manager and the internal/processor configuration access port (ICAP/PCAP) are compromised [37]. This leads to three new attack scenarios: (1) malicious or unregistered bitstream files can be loaded to the FPGAs; (2) unauthorized software can access user logic; (3) attackers can redirect messages between a software application and its custom logic to a malicious application.

To defend against a compromised reconfiguration manager and ICAP/PCAP, [37] suggested adding a secure authentication module (SAM), a task/application loading module, and a secure task database into the system. The SAM distributes a shared secret key to users and asks them to embed



Fig. 11. Physical isolation by blocking the adjacent wires upto a distance of 3 from the potential transmitter wire [51].

the key in their applications and hardware modules. By actively running a challenge-response protocol between a software application and its hardware task modules, the SAM can verify the authenticity of applications and tasks, and the applications and tasks can mutually verify the authenticity of each other. Also, the issue of running an unregistered hardware task (or task hiding in [37]) can be remedied by introducing a secure task database and enforcing every authorized user to register her tasks in the database.

The authors in [63, 139] introduced access control policies or an encryption core to secure the communication between the processors and the hardware accelerators on the FPGA. However, they overlook the threat of a malicious co-tenant on the same FPGA who can launch side-channel [115, 142] and fault-injection attacks [83].

**Physical isolation.** The most effective method to prevent *long* wire crosstalk effect-based attacks is physical isolation. Huffmire *et al.* proposed the concept of physical moats on FPGAs to isolate the hardware cores of different users [68]. The moats are implemented using disabled switchboxes (SBs) surrounding each hardware core. The width of the moats (the number of disabled SBs) depends on the number of SBs that can be skipped in routing a *long* wire on the FPGA. In practice, as it is suggested in [51], minimum width of three, as depicted in Fig. 11, should be enforced to minimize *long* wire crosstalk. Also, if the location of the attacker on the FPGA can be known and constrained, then one can use the FPGA Trust Zone technique proposed in [75] to avoid the FPGA regions adjacent to the attacker.

As the first step in automating secure routing to mitigate the crosstalk effect in *long* wires, Seifoori *et al.* extended an existing open-source FPGA routing tool, PathFinder, to build a routing tool to prevent crosstalk-based side-channel leakage [118]. To use the proposed tool, users need to annotate the trusted IP cores and sensitive FPGA nets (e.g., the ones carrying secret keys). In the proposed tool, Seifoori *et al.* proposed four routing strategies. (1) Block-2NN, meaning that no net is allowed to use the nearest and the second nearest *long* wires of a sensitive net; (2) Block-NN, meaning the nearest *long* wires of a sensitive net will not be occupied; (3) Block-Untrusted, no nets from an untrusted IP module can be allocated adjacent to a sensitive net; (4) Lock-NN, meaning the nearest *long* wires of a sensitive net can only be occupied by the nets originating from the same module as the sensitive net. Using the Verilog-to-Routing benchmark [110], they found that the four strategies incur 1.91% to 7.69% overhead in channel width on average with respect to the baseline, and secure routing introduces 0.12% to 1.18% increase in critical path delay on average.

An automatic hardware isolation framework, HILL, was presented in [86]. Given a list of securitycritical net names in a design by the designers, HILL can automatically generate a constraint file for an FPGA tool (e.g., Vivado or Xilinx ISE) to place the critical instances (e.g., LUTs) in the middle of the hardware design and route all the other instances in a spiral manner around the critical instances. Thus, the critical instances are protected by the non-critical instances in the protected design from an attacker who is placed outside of the design. If the width of the surrounding non-critical instances is sufficient, the attacker cannot exploit the crosstalk phenomenon to leak information from critical instances. Moreover, for some *long* wires which cannot be placed in the middle of a design, like IO buffers, the authors suggested adding two dummy *long* wires to be adjacent to the vulnerable *long* wires to obfuscate the observation of an attacker.

**Runtime monitors.** Runtime monitoring is a general defense methodology that deploys performance monitors on the FPGAs to detect suspicious behaviors during runtime. Without compromising the users' privacy in the hardware designs, the cloud provider can deploy runtime monitors on the FPGAs to monitor the running status of the FPGAs. For example, ROs were proposed to check the delay variations [24, 143], and TDC was introduced in [144] for sensing nanosecond-scale voltage variations. These sensor designs were all proposed before the first remote side-channel attacks on FPGAs were conducted.

To take one step further in this direction, Provelengios *et al.* characterized the behavior of a power distribution network on an FPGA under a power-based fault-injection attack [105]. In particular, they studied the geographic distribution of a voltage drop around a power waster (the source of attacks, e.g., ROs). Essentially, the closer a circuit is to the power waster, the more voltage drop it experiences. Based on this finding, one can build a distributed voltage monitor network on an FPGA to identify, in real-time, the location of the malicious circuit. Then, the cloud provider can move the suspicious user's circuit to another single-tenant FPGA or remove the user from the cloud.

One drawback of using a runtime monitoring approach is that it can only detect active attacks like fault-injections. The existing runtime monitors can not check whether there exists an attacker in the chip who is monitoring the system quietly.

Active defenses. To counter the passive attacks, like side-channel attacks, a user can actively inject noise into the power traces [82]. This paper introduced active fences between the victim circuits and power side-channel attack circuits, as shown in Fig. 12. The fences are composed of ROs, and these ROs can be activated by two approaches following the principles of hiding and masking, respectively. To hide the secret information in the power traces, the active fences try to consume power by operating the ROs appropriately, such that the overall power consumption is flat. To this end, the active fences are controlled by an on-chip RO-based power sensor. For instance, if the power sensor detects that the power consumption increases, the active fences is to use a pseudorandom number generator (PRNG). This approach follows the principle of masking, and it creates a noisy power profile for the attacker to measure. Experiments showed that by deploying active fences, the number of required power traces for a successful attack increases by 2 to 3 orders of magnitude. The authors also noted that the power sensor-activated fences using hiding principles are more effective in defenses.

### 7 SECURING CLOUD COMPUTATION USING FPGAS

On traditional cloud computation platforms, users can not control the underlying hardware that executes the computation. So, the users have to trust the cloud providers to handle their data properly and securely. Since the introduction of Intel SGX [33], the users do not have to trust the cloud provides. They need to trust only the manufacturers of the processors, i.e., Intel. This bottom-up trust model shows that one can minimize the trusted computing base to a trusted hardware like a processor. Cloud FPGAs, as programmable hardware in the clouds, can be used to construct an alternate trusted computing base for users when the processors are not trustworthy. We can use them as security monitors to check the behavior of the processor or an application. For example, a user can extract hardware fingerprints of cloud service instances and recover the



Fig. 12. Active injection of noise into power traces by activating an appropriate number of ROs [82].

architecture of the cloud infrastructures [125]. Looking into the future, different architectures of FPGA clouds can emerge. For example, IBM Zurich is working on the *cloudFPGA* project and proposing architectures for network-attached FPGAs [1]. This architecture allows the FPGA to access the network directly and process network packets independent of the processors.

### 7.1 Architectural Supports

In 2012, Eguro and others envisioned an FPGA-based cloud computing platform [36]. In this platform, the computation and data are sent to the cloud FPGA as encrypted data and an encrypted bitstream. In the cloud FPGA, the FPGA manufacturer pre-loads a secure bootstrapper bitstream. The secure bootstrapper shares a secret key with cloud clients and decrypts the data and bitstream files. After that, the data is computed using the hardware design described by the bitstream. Before the final results leave the cloud, they are encrypted again. This way, the client receives encrypted results, which he/she can decrypt locally.

To extend the idea of FPGA-based trusted computing in the cloud, Arasu *et al.* proposed to use the above methodology for building an FPGA-based trusted co-processor, Cipherbase [11]. It aims at securing database operations. In the system architecture of Cipherbase, the whole database is encrypted, and the key is known to Cipherbase. Any expression evaluations are outsourced to Cipherbase. Because Cipherbase knows the secret keys, it can decrypt the data and evaluate the requested expression on the plaintext data easily. This architecture makes sure that the untrusted server which manages the database can have access only to the encrypted database, and the co-processor can assist the server in performing typical database operations efficiently.

Xu *et al.* [137] proposed a similar idea as [36] to enable efficient privacy-preserving computation in the cloud. [137] considered FPGAs as security containers and decrypts the data at the entry point of the cloud FPGA. Then, the data is encrypted again upon leaving the FPGAs. The main innovation in [137] is that the authors introduce proxy re-encryption to reduce the burden of key management in [36]. The concept of proxy re-encryption allows users to use their own keys for encryption. Moreover, the ciphertext encrypted by a user's key can be converted to a ciphertext of the same content encrypted by an FPGA's key without decrypting the ciphertext. This allows the user and the FPGA to exchange encrypted data without exchanging keys.

### 7.2 Cryptographic Accelerators

The original purpose of introducing FPGAs into clouds was to enable the deployment of hardware accelerators to speed up the computation. Naturally, complex cryptographic operations need to be accelerated by hardware to satisfy the performance requirement in practice. In the rest of this subsection, we review two categories of cryptographic algorithms that demand to be implemented in hardware to improve their performance. The first one is fully/somewhat-homomorphic encryption [39, 46, 128], which was originally designed to allow computation over encrypted data in clouds. The second type of algorithms that needs hardware acceleration extensively is post-quantum cryptographic algorithms. These algorithms are the future direction of the cryptography for when quantum computers will be realized [22, 30]. The third type is the privacy-preserving computation, such as garbled circuit evaluation [138], which allows clouds to compute on user's program without leaking secrets.

Many hardware accelerator architectures of homomorphic encryption have been proposed and implemented on FPGAs. For example, [104] proposed an architecture to accelerate the homomorphic encryption scheme YASHE. The hardware accelerator was able to provide roughly two orders of magnitude speedup compared with a software implementation of the same scheme by then. However, YASHE is no longer considered secure after an attack proposed in [4]. FV somewhat homomorphic encryption scheme [39] was implemented in [112], which requires 26.67 seconds for one homomorphic multiplication. Of the 26.67 seconds, only 3.36 seconds are used for actual computation, and the rest is the data access overhead due to the usage of a large parameter set. In fact, the large parameter size in secure homomorphic encryption schemes is the performance bottleneck on data transfers, as observed in [104, 112, 113]. With a smaller parameter setting, one recent work on accelerating the FV scheme shows 13 times performance improvement over a highly optimized software implementation of the FV scheme [113]. Also, researchers have addressed other performance bottlenecks as well. For instance, [32, 35] proposed new multiplier architectures, and an improved Chinese Remainder Transformation accelerator was introduced in [34].

Although the NIST standardization competition of post-quantum cryptography is ongoing, the hardware accelerators of the proposed signature schemes and key encapsulation schemes are being investigated in [19, 129]. [129] presents a full FPGA implementation of a Niederreiter cryptosystem based on Binary Goppa Codes. This design achieves three orders of magnitude speedup compared to state-of-the-art software implementation. This shows a high potential of hardware accelerators for post-quantum cryptographic algorithms. More efforts have been presented in [19], which evaluate the potential performance gains of FPGA hardware implementations of NIST post-quantum competition candidates. The authors used HLS (High-level synthesis) tools for faster design-space exploration, and the results can be considered as a strong indicator of the hardware performance in the selection process of the NIST competition.

In addition, researchers have been implementing FPGA accelerators for privacy-preserving techniques, e.g., Garbled Circuits [138], on the cloud. Garbled circuits, or secure function evaluation, is a technique that allows secure two-party computation. Using this, two mutually untrusted parties can jointly evaluate one function on their private inputs. MAXelerator was introduced as an FPGA accelerator on clouds for privacy-preserving machine learning in a garbled circuit form [69]. The authors noticed that most of the privacy-sensitive computation in machine learning applications could be boiled down to multiply-accumulate operations, so they specifically used FPGAs to accelerate the multiply-accumulate garbled circuit computation. Overall, they achieved up to 57 times throughput improvement compared to the state-of-the-art software garbled circuit framework. A general-purpose FPGA accelerator for one party (garbler) in a two-party garbled circuit protocol was built by Huang *et al.* in [66]. They also implemented and demonstrated the

FPGA accelerator on AWS instances, and they showed a 15 times speedup in garbler computation compared to a software-based garbled circuit framework.

### 7.3 FPGA-based Security Primitives

Having programmable hardware in clouds allows users to construct their security primitives in the clouds. For example, they can build their own physical unclonable functions (PUFs) [44, 65] to identify individual FPGA chips. Many FPGA-based PUF designs were proposed and open-sourced online for fostering future research. As the first cryptographically secure PUF, LPN-based PUF [64] was implemented on a Zynq FPGA in a software/hardware co-design style, which perfectly fits the model of cloud FPGAs attached to a server [72]. The current state-of-the-art lightweight PUF design, interpose PUF (iPUF), which can resist all known attacks, was implemented in FPGAs as well [96]. One can extend PUFs to construct more security applications. For example, a PUF can be used for proof of execution in the cloud, which proves the identity of the device which runs the requested computation [45]. Tian *et al.* instantiated decay-based DRAM PUFs [136] in AWS F1 instances, and thus they can fingerprint each instance in AWS cloud [125]. Using these unique fingerprints of cloud instances, they experimentally figured out the probability of renting the same FPGA instance more than once, which provides unique insights for an attacker to launch further attacks.

Besides PUFs, true random number generators (TRNGs) can also be built on cloud FPGAs as an alternative to generating reliable randomness sources [102]. Most of the FPGA-based TRNG designs take ROs as a core building block [40], but, unfortunately, ROs, being combinational loops, are prohibited in the AWS clouds. One alternative approach is to exploit the metastability as a random source. For example, [88] presents a programmable delay line based TRNG design. This design does not require an RO as its building block. This demonstrates the possibility of building private and reliable TRNGs in the cloud.

### 8 RELATED RECENT SURVEYS

We acknowledge recent surveys on (cloud) FPGA security. [141] surveyed attacks and defenses on FPGAs in general and did not focus on the unique characteristics of cloud FPGAs. [93] focused on the security issues of cloud FPGAs, but the scope was narrowed down to only the side-channel attacks on cloud FPGAs, which is narrower than the scope of this paper. Similarly, [90] provided an excellent resource to study side-channel and fault injection attacks, but cloud FPGAs are facing more security issues than what they mentioned. [126] in 2017 presented a high-level overview of the security issues in cloud FPGAs or FPGAs in data centers. However, as the security research on cloud FPGAs is evolving rapidly, remote side-channel attacks, fault-injections, and covert channels were not known by then, and therefore not covered in their paper. Nonetheless, some of the visionary countermeasures mentioned in [126] are shown to be effective in later research, e.g., the bitstream checkers and runtime monitoring. Last but not least, universities have started teaching courses on cloud FPGAs.

Our paper not only presents recent work on cloud FPGA security in a comprehensive and timely manner but also surveys the related work on FPGAs to secure cloud computing. Thus, this survey covers the security issues beyond the attacks and defenses of FPGA security in clouds.

### 9 CONCLUSIONS AND FUTURE CHALLENGES

Cloud FPGA is an emerging trend with several security-related open problems awaiting exploration. From an attacker's point of view, we believe that the current known attacks in Section 4 are still an incomplete list of possible attacks on cloud FPGAs. More attacks are likely to be proposed in

the future, such as side-channel attacks exploiting other side-channel leakage sources. Also, using known information leakage sources, more information may be inferred. Notice that researchers have implemented a power-based instruction disassembler on a microprocessor [99]. This means that allowing attackers to observe the power consumption of the processor from the connected FPGA fabric can potentially reveal more information than what has been demonstrated in [57, 142].

In the system model, we demand strong security measures that can be used by cloud clients so that the clients do not need to trust the cloud providers. Ideally, the clients should be able to remotely verify some security properties (e.g., integrity) of their logic in the clouds. In addition, the clients may want to remotely verify the size of memory space using proof of space [108], the authenticity of the platform using remote attestation [33], the aliveness of the program using proof of aliveness [73], or the physical location of the data storage [25]. All of these traditional security issues in cloud computing need to be extended to include the FPGA platform as well.

In a multi-tenant FPGA setting, more security mechanisms need to be in place to protect cloud users from other malicious users. How to efficiently defend against existing side-channel attacks and fault injection attacks without compromising the privacy of the user's design is still an open problem. Existing countermeasures fail to satisfy at least one of three requirements: low overhead, protection against known attacks, and the privacy of users. Traditional countermeasures provide strong security guarantees, but they incur significant hardware overhead. Bitstream checkers can detect malicious circuit designs given the list of known attacks. However, this requires access to cloud users' hardware designs. Passive online detection and active defenses require their deployment by the cloud providers and joint use to defend against side-channel and fault attacks.

We can redesign the architecture of FPGA clouds in such a way that the FPGA can support the security features of the clouds and the FPGAs. For example, FPGAs can be used to support the secure boot of computing systems [103]. Moreover, new FPGA cloud architectures can potentially limit the capability of malicious cloud providers. [37, 63, 139] have effectively demonstrated new architectures by enforcing access control policy between processors and FPGA logic, or encrypting the messages transmitted between processors and FPGA logic. However, these mechanisms all require the cloud providers to deploy such a method by themselves, so it still requires some trust in the cloud providers. At least, trust in the infrastructure designers and manufacturers is needed if these mechanisms are built in the infrastructure hardware.

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