International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

# Seven Level Inverter

Abhil T Balakrishnan, Alan James,
Jibson Thomas Job,Ayona Thomas
Eight Semester Electrical and Electronics Engineering
Bachelor of Technology In Electrical And Electronics Engineering
Mahatma Gandhi University.
Kottayam

***Abstract* - Multilevel inverters have been widely accepted for high-power high-voltage applications. Here,reverse voltage topology is used. This topology requires fewer components compared to existing inverters and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels.This topology requires less number of components compared to conventional topologies. Output voltage is separated into two parts,level generation part and polarity generation part. Level generation part uses high frequency switches to generate different levels and polarity generation part is responsible for generating the polarity of the output voltage. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter. Finally, a prototype of the seven-level topology is built and tested to show the performance of the inverter by experimental results.**

## CHAPTER 1
## INTRODUCTION

Multilevel power conversion was rest introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic pro le, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller size, and lower EMI, all of which make them cheaper, lighter, and more compact.

One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in the multilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated volt-age sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing. To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices.

In general, three main types of multilevel inverters, i.e. diode clamp, flying-capacitor, and cascade inverter with separated dc sources, have been developed. Recent research has involved the introduction of novel converter topologies and unique modulation strategies. However, the most recently used inverter topologies, which are mainly ad-dressed as applicable multilevel inverters, are cascade converter, neutral-point clamped (NPC) inverter, and flying capacitor inverter. There are also some combinations of the mentioned topologies as series combination of a two-level converter with a three-level NPC converter which is named cascade 3/2 multilevel inverter . There is also a series combination of a three-level cascade converter with a seven-level NPC converter which is named cascade 5/3 multilevel inverter .

The multilevel output is generated with a multi winding transformer. However, the design and manufacturing of a multi winding transformer are difficult and costly for high-power
applications. The topology is a symmetrical topology since all the values of all voltage sources are equal. However, there are asymmetrical topologies which require different voltage sources. This criterion needs to arrange dc power sup-plies according to a specific relation between the supplies. Difference in ratings of the switches in the topology is also a major drawback of the topology. This problem also happens in similar topologies, while some of the high-frequency switches should approximately withstand the maximum overall voltage which makes its application limited for high-voltage products. A new approach has been proposed that decreases the number of required dc supplies and inserting transformer instead. The main disadvantage of the approach is adding so many transformer windings which will add up to the overall volume and cost of the inverter.

Here, another topology named reverse voltage topology is used. This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter. Two switches are re-moved from and the required topology with reduced switches is obtained. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

*1.1 Inverter*

A dc-to-ac converter whose output is of desired output voltage and frequency is called an inverter. Based on their operation the inverters can be broadly classified into

- Voltage Source Inverters(VSI)
- Current Source Inverters(CSI)

A voltage source inverter is one where the independently controlled ac output is a voltage waveform. A current source inverter is one where the independently controlled ac output is a current waveform. On the basis of connections of semiconductor devices, inverters are classified as

- Bridge inverters
- Series inverters
- Parallel inverters

Some industrial applications of inverters are for adjustable-speed ac drives, induction heating, stand by air-craft power supplies, UPS(uninterruptible power supplies) for computers, hvdc transmission lines etc.

*1.2 Merit and Demerit of Multilevel Inverter*

Obviously, in recent years multilevel inverter has gained an attention from many areas due to its advantages over the conventional inverters. The ability of the multilevel inverter to utilize a large number of dc sources is one of the merits that it holds. This makes multilevel inverters able to generate high voltages and thus high power ratings. Due to this, the use of bulky and expensive transformers to produces high voltages with conventional 12, 24 and 48-pulse inverter can be abandoned. Another advantage of multilevel inverter is that it has a reduced Total Harmonic Distortion (THD) with low switching frequencies. Furthermore, due to its lower voltage steps, the value of EMI is lesser and because of its capability to utilize multiple levels on the dc bus, the multilevel inverters able to trim down the voltage stress on each power devices. Additionally, multilevel inverters have higher efficiency because the devices can be switched at low frequency. Nevertheless, there is still a pitfalls on everything created in this world including multilevel inverter. One of the demerits of multilevel inverters is the isolated power supplies required for each one of the multiconverter. Furthermore, number of components is increased in multilevel inverter compared to traditional inverters. The idea of having larger number of components also means the probability of a device failure will increase.

*1.3. The Switching*

There are many ways and techniques have been developed to control multilevel inverter switching, from the very basic fundamental switching up to the most advance space vector pulse width modulation switching scheme. But, the most famous and applied by industries out there is the PWM switching control scheme. PWM switching control scheme comes with advantages over the traditional multilevel fundamental switching scheme. One benefit of PWM methods employing much higher switching frequencies concerns harmonics. The harmonics filtering exercise is much easier and cheaper due to the fact that the undesirable harmonics occur at much higher switching frequencies. Also, the produced harmonics might be above the bandwidth of some actual system. This means that there is no power dissipation caused by the harmonics. On the contrary, multilevel fundamental switching scheme creates harmonics at lower switching frequencies and this increased the complexity of the filtering activity.

*1.4. Control Techniques*

Multilevel inverter parameter quality such as switching losses and harmonic reduction are basically depends on the modulation strategies applied to the inverter. Several modulation and control techniques have been developed for multilevel inverters. Control technique for the multilevel inverter cab be classifiedinto PWM, Selective Harmonic Elimination PWM (SHEPWM) and Optimized Harmonics Stepped Waveform (OHSM). PWM can be classified to open loop and closed loop. For this research, open loop modulation is proposed which will focus on Sinusoidal PWM (SPWM).

## CHAPTER 2
## LITERATURE SURVEY

Jang-Hwan Kim et. al proposed a carrier-based PWM method for a multilevel four-leg PWM VSI along with introducing a novel o set voltage. This is a method with optimal switching sequence. The proposed o set voltage makes it possible for the switching sequence of all the legs to be optimized for minimizing the harmonic distortion of the output voltage irrespective of the number of inverter levels and lower certain electro-magnetic influence in output voltage. This PWM method is based on digital signal processors is implemented and tested by using a prototype three-level four-leg VSI. But this topology has many disadvantages. One of the disadvantage is that it has in-creased number of switches. Moreover it uses a complicated PWM method and also it is associated with voltage balancing problem at the neutral point.

S. Sreekanthan et.al proposed the inverter topology which rely on split-capacitor configurations in order to achieve different voltage levels. Due to various reasons like unequal capacitance leakage currents, asymmetrical tracking of current, unequal delays in semiconductor devices, the presence of dc components in the neutral current, etc., the capacitor voltages drift away from the reference values, degrading the performance of the inverter. A simple technique of carrier-based error control has been suggested for the inverter-chopper circuit in order to correct the capacitor voltage imbalances. The main

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

disadvantage is that the chopper current is discontinuous because of the appropriate frequency chosen.

Leon M. Tolbert et.al[] proposed two multilevel inverter control schemes where devices are switched only at the fundamental frequency and the inverter output line voltage THD is 5 percent. In addition, a control scheme was demonstrated in the multilevel diode clamped converter that obtains well balanced voltages across the dc link capacitors. the disadvantage is that active control of the dc bus voltage by the converter or a larger capacitance is required for the dc voltage levels if the motor speed is going to change fairly rapidly and less variation in the overall dc bus voltage is desired.

Yun XU et.al proposed a novel composite cascade multilevel converter based on the series-connection of a +ve level diode-clamp converter and several identical three level H-bridge converters with equal dc bus voltage, and the output waveform is synthesized by adding of each converter output voltage. With the hybrid control strategy pro-posed in this paper, the new power inverter topology permits faster devices and high voltage devices operating in synergism. Analysis of power was carried out, and the GTO modules do not feed the power into the IGBT module. So available redundancy and easy extensibility can be provided by the modular structure of the converter.

Ehsan Naja et.al proposed a new topology with a reversing-voltage component is proposed to improve the multilevel performance. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels. The output voltage is separated into two parts: level generation and polarity generation part. Thus all the switches are not working at high frequency. Compared to the other topologies, this requires half the conventional carriers for SPWM controller.

## CHAPTER 3
## PULSE MODULATION SCHEMES

### *3.1 Pulse Amplitude Modulation*

Pulse Amplitude Modulation refers to a method of carrying information on a train of pulses, the information being encoded in the amplitude of pulses. In other words the pulse amplitude is modulated according to the varying amplitude of analog signal.

### *3.2 Pulse Width Modulation*

Pulse Width Modulation refers to a method of carrying information on a train of pulses, the information being encoded in the width of the pulses. The pulses have constant amplitude but their duration varies in direct proportion to the amplitude of analog signal.

### *3.3 Pulse Position Modulation*

The amplitude and width of the pulse is kept constant in the system. The position of each pulse, in relation to the position of a recurrent reference pulse, is varied by each instantaneous sampled value of the modulating wave. PPM has the advantage of requiring constant transmitter power since the pulses are of constant amplitude and duration.

### 3.4 PULSE CODE MODULATION

To obtain PCM from an analog waveform at the source (transmitter), the analog signal amplitude is sampled at regular time intervals. The sampling rate (number of samples per second), is several times the maximum frequency of the analog waveform. The amplitude of the analog signal at each sample is rounded off to the nearest binary level (quantization).

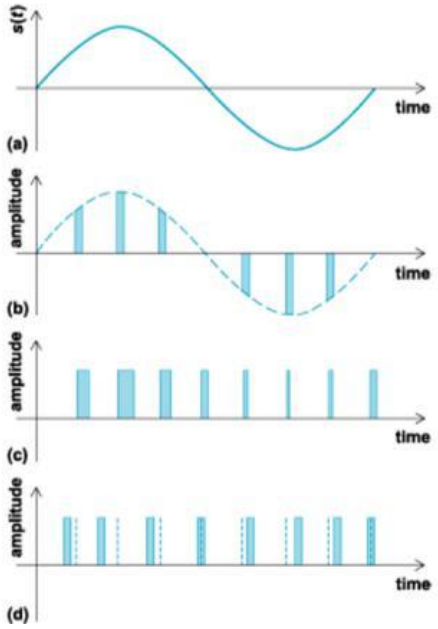



Figure 3.1*(a)* Analog signal S(t) (*b*) Pulse-amplitude modulation (c)Pulse-width modulation(d) Pulse position modulation

Number of levels is always a power of 2 (4, 8, 16, 32, 64, ...). These numbers can be represented by two, three, four, five, six or more binary digits.

PCM is a general scheme for transmitting analog data in a digital and binary way, independent of the complexity of the analog waveform. With PCM all forms of analog data like video, voice, music and telemetry can be transferred.

### *3.5 Advantages Of Pwm*

- The output voltage control is easier with PWM than other schemes and can be achieved without any additional components.
- The lower order harmonics are either minimized or eliminated altogether.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

- The filtering requirements are minimized as lower order harmonics are eliminated and higher order harmonics are filtered easily.
- It has very low power consumption.
- The entire control circuit can be digitized which reduces the susceptibility of the circuit to interference.

## CHAPTER 4
## SEVEN LEVEL INVERTER

### *4.1.Reverse Voltage Topology*

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the reverse voltage topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output.

In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities. The RV topology in seven levels is shown in Figure 4.1. As can be seen, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Figure 4.1 generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output volt-age. This part, which is named polarity generation, transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity. It can also be applied for three-phase applications with the same principle. This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. This topology is well suited for a 3 phase system.

This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient. The reason is that, according to Figure 4.1, the multilevel converter works only in positive polarity and does not generate negative polarities. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. It is also comparable to single-carrier modulation, while this topology requires the same number of signals for PWM. However, this topology needs one modulation signal which is easier to generate as opposed to the single-carrier modulation method
which needs several modulation signals. Another disadvantage of this topology is that all switches should be selected from fast switches, while the proposed topology does not need fast switches for the polarity generation part. In the following sections, the superiority of this topology with respect to PWM switching and number of components is discussed.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

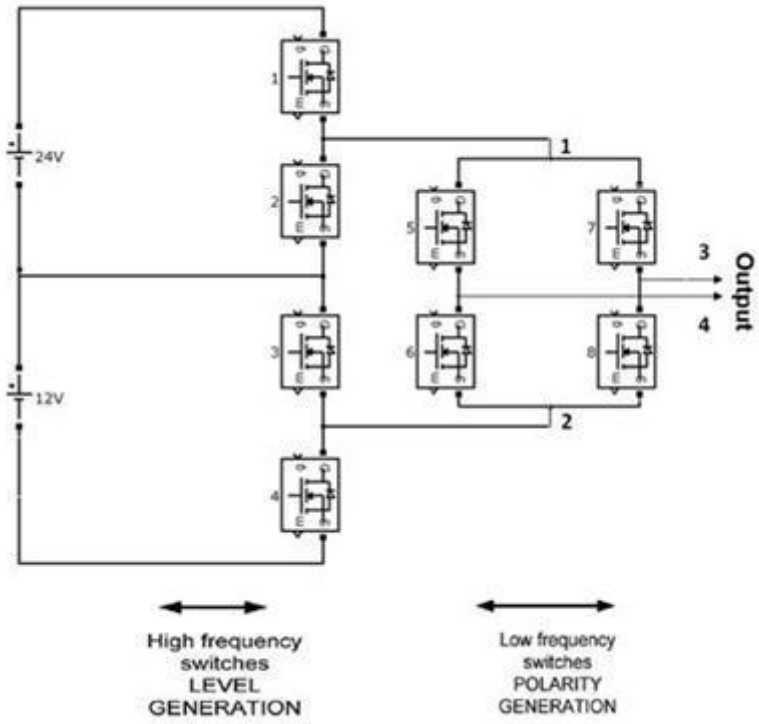



Fig.4.1:Schematic of a seven-level inverter in single phase

*4.1.1 Switching Sequences*

Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements.

The sequences of switches (2-3), (2-4), (1-3), and (1, 4) are chosen for levels 0,1,2 and 3 respectively. As can be observed from Figure4.2 to figure 4.4, the output voltage levels are generated by appropriate switching sequences. The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown in Fig. 4. In this paper, PD SPWM is adopted for its simplicity. Carriers in this method do not have any coincidence, and they have definite o set from each other. They are also in phase with each other.

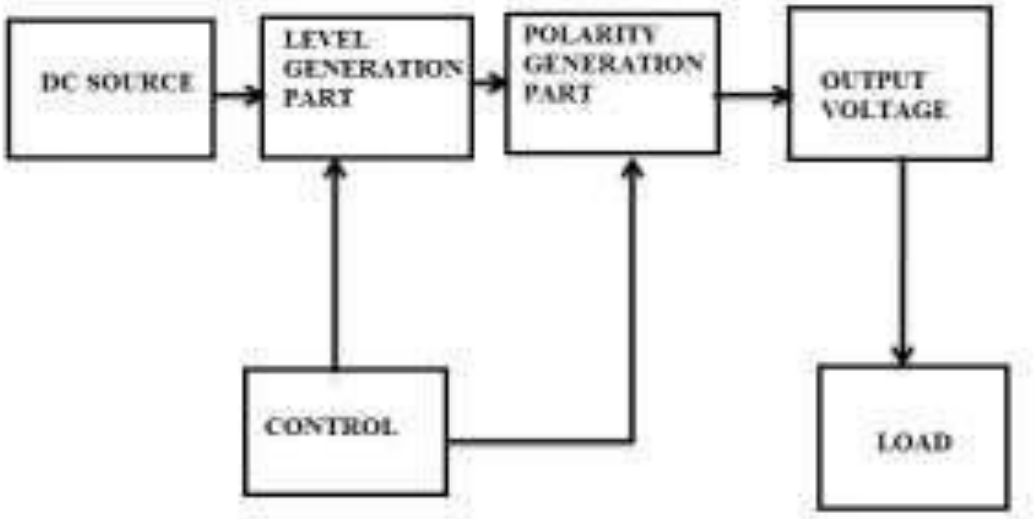



Fig.4.2: General Block Diagram of Seven Level proposed Topology

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

*Level 0*

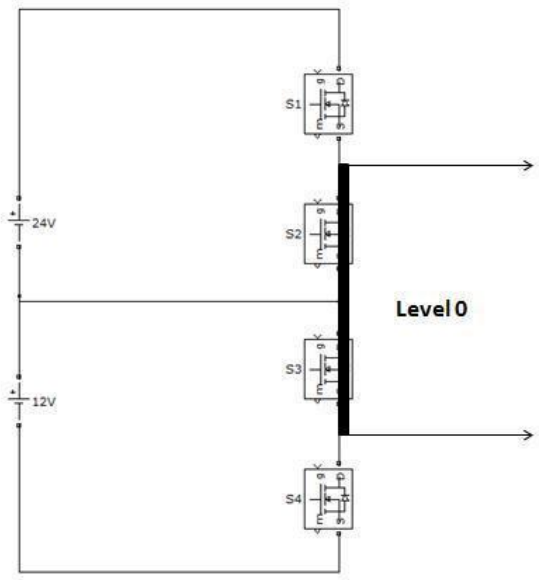



Figure 4.3: Switching sequence for level 0

As in figure 4.2, switches 2 and 3 are turned on for level 0.The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. As a result ,zero volt is the output.

Level 1

As in figure 4.3, switches 2 and 3 are turned on for level 0.The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. As a result ,zero volt is the output.

Level 2

As in figure 4.4, switches 2 and 3 are turned on for level 0.The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. As a result ,zero volt is the output.

Level 3

As in figure 4.5, switches 2 and 3 are turned on for level 0.The ultimate output volt-age level is the sum of voltage sources, which are included in the current path that is marked in bold. As a result ,zero volt is the output

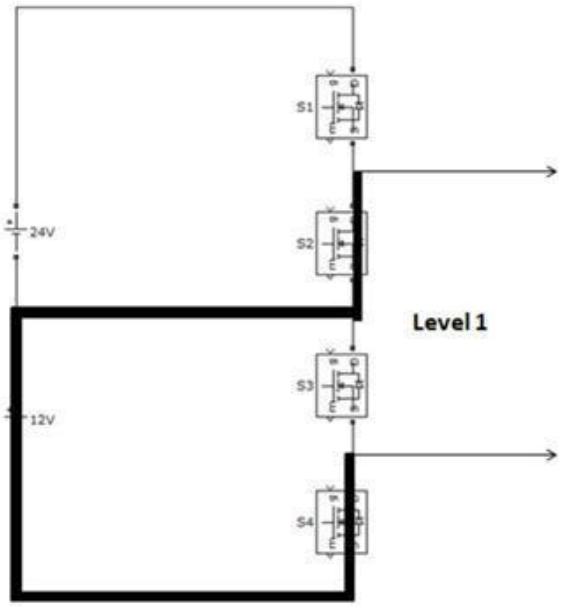



Figure 4.4: Switching sequence for level 0

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

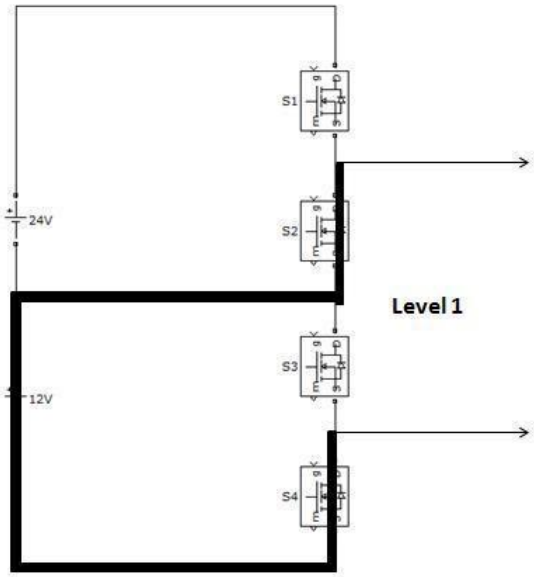



Figure 4.5: Switching sequence for level 1

The number of switches in the path of conducting current also plays an important role in the efficiency of overall converter. For example, a seven-level cascade topology has 12 switches, and half of them, i.e., six switches, conduct the inverter current in each instance. However, the number of switches which conduct current in the proposed topology ranges from four switches (for generating level 3) to ve switches conducting for other levels, while two of the switches are from the low-frequency (polarity generation) component of the inverter. Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the cascade inverter, and hence, it has a better efficiency. The same calculation is true in a topology mentioned. The least number of switches in the current path for a seven-level inverter.

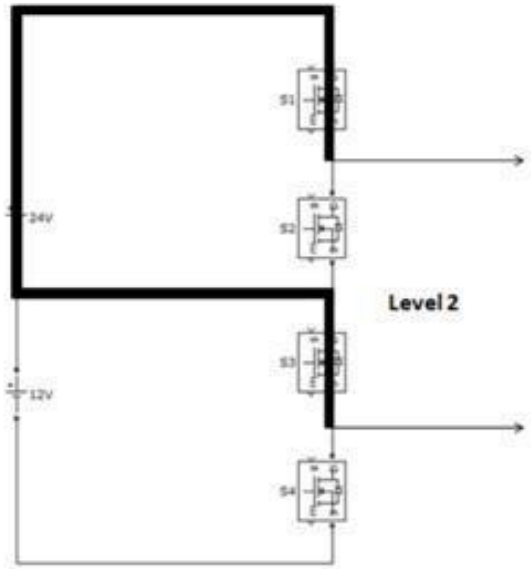



Figure 4.6: Switching sequence for level 2

According to is positive (for generating level 3), which requires one switch more in the current path compared to the proposed topology which requires only four conducting switches. These switching sequences can be implemented by logic gates or DSP. The signal stage should be isolated from the power stage by optocouplers for control circuit protection. The drive circuit is also responsible to generate the dead time between each successive switching cycle across the dc source. The gating signal for the output stage, which changes the polarity of the voltage, is simple. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse modes. In the forward mode, switches 8 and 9 as in Figure 4.1 conduct, and the output voltage polarity is positive. However, switches 7 and 10 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, the low-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency.

*4.2 Switching Pattern*

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

| Level / Mode | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 1 | 2,3,4 | 2,3,5 | 1,4 | 1,5 |
| 2 | | 2,4,6 | 2,6,5 | |

In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation. According to the aforementioned suggestions, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. These sequences are shown in

Fig. 3. As can be observed from Fig. 3, the output voltage levels are generated in this part by appropriate switching sequences. The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required.

*4.3 Number of Components*

One of the promising advantages of the topology is that it requires less high-switching-frequency components. High-frequency switches and diodes are expensive and are more prone to be damaged than low-frequency switches. According to the MIL-HDBK-217F standard, the reliability of a system is indirectly proportional to the number of its components. Therefore, as the number of high-frequency switches is increased, the reliability of the converter is decreased. In the proposed converter, as can be seen, half of the switches in the full-bridge converter will not require to be switched on rapidly since they are only switched at zero crossings operating at line frequency (50 Hz). Thus, in this case, the reliability of the converter and also related expenses are highly improved.

It can clearly be inferred that the number of required three-phase components ac-cording to output voltage levels for the proposed topology is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels. As the most important part in multilevel inverters is the power semiconductor switches which de ne the reliability and control complexity, the number of required switches against the required voltage levels is shown in Figure 3.6 for the new topology as well as other topologies.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

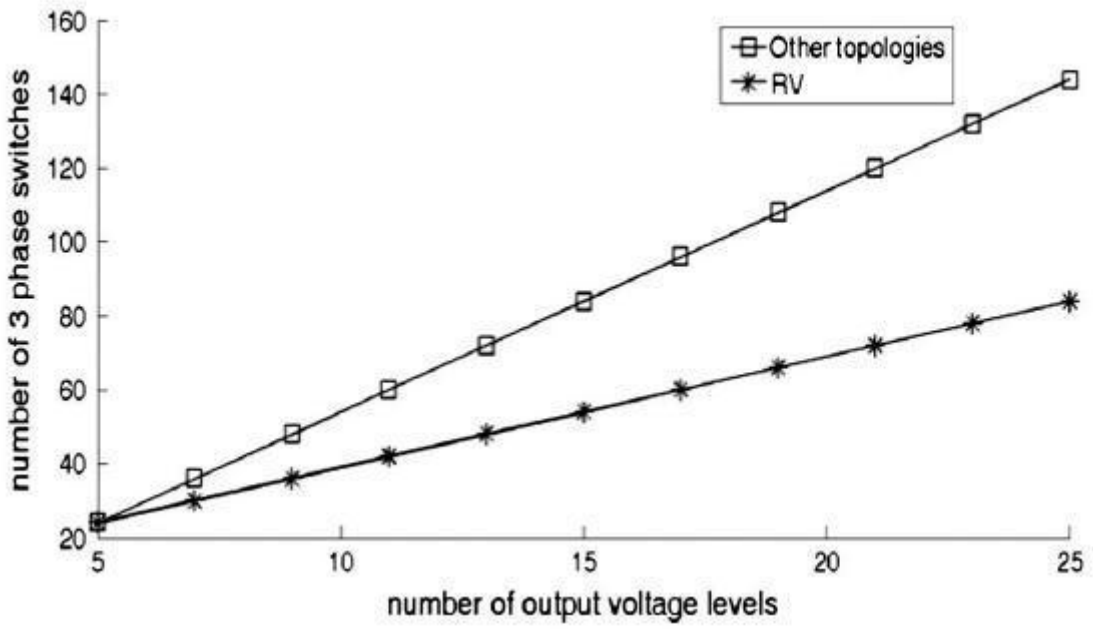



Figure 4.6: Required switches for multilevel inverter

*4.4 Control Strategy*

The carrier based PWM technique fulfills the on and off states of the switches by comparing a modulating signal VA output voltage and a triangular waveform VC (carrier signal). The modulating signal VA is a sinusoidal signal at frequency FC and amplitude VA and the triangular signal VC is at frequency FC and amplitude VC. This is the SPWM method. The modulation index is defined as ma = VC/VA and the normalized carrier frequency is mf = FC/FA. PWM has the following advantages.

1. The entire control circuit is digital, digital control lines reduce the susceptibility to interference and also motors may be able to operate at lower speeds.

2. The output voltage control can be obtained without any additional components.

3. Lower order harmonics can be reduced along with its output voltage control.

   In this topology, PD-SPWM is adopted for its simplicity and the carriers are in phase with each other. Here PD-SPWM is used for driving the high frequency switches and low frequency polarity generation part drive signals are generated with the line frequency (50Hz) and they only changes at zero- voltage crossings. For a conventional cascaded MLI, (n-1) triangle waveforms are used. In the proposed topology, a phase modulation signal is compared with (n-1)/2 triangle waveforms for an n-level inverter.

One of the main advantages of this topology is that it requires less high frequency switches and the reliability of the system is indirectly proportional to the number of its components. As the number of high frequency switches is decreased, the reliability of the converter is increased. Hence the reliability is highly improved in this topology. Also high frequency switches are expensive and easily damaged. It can clearly be mentioned that the number of components of this topology is lower than that of other topologies and it will decrease tremendously with higher voltage levels. Switches in the full bridge converter are switched at line frequency.

## CHAPTER 5
## SIMULATION MODELS AND OUTPUT WAVEFORMS

The detailed MATLAB/Simulink model for seven level inverter is shown in figure 5.1. The different blocks used for this project are explained separately. In the figure 5.1,

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

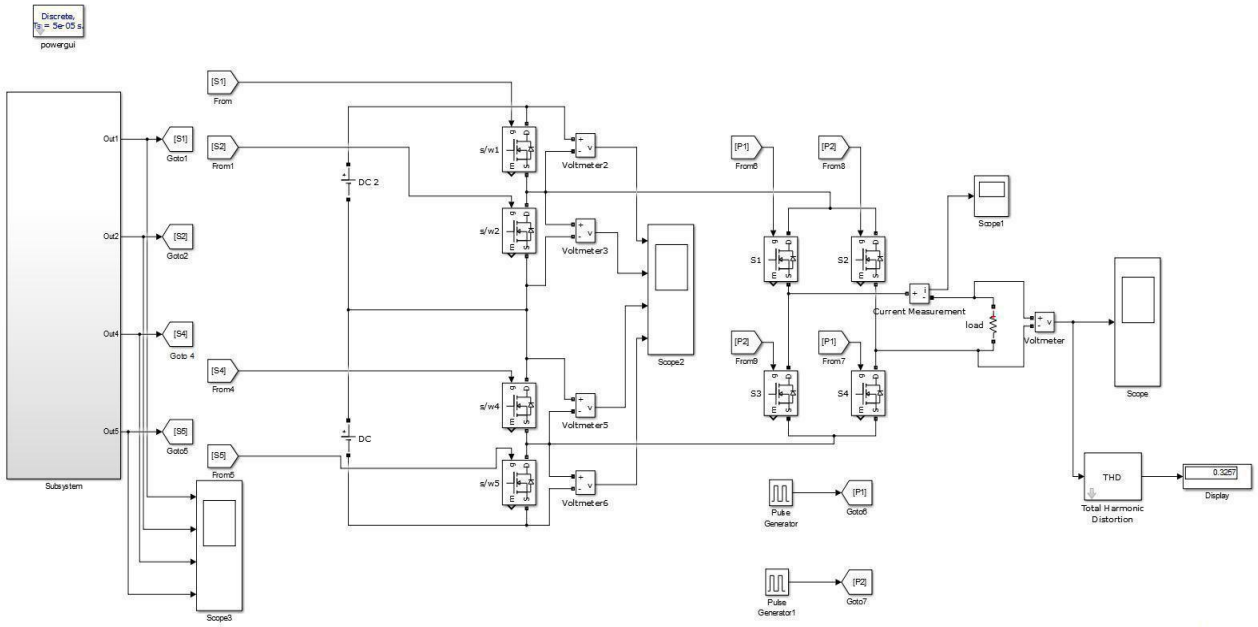



Figure 5.1: Seven level inverter

complete model of seven level inverter is shown. Switches are triggered using PD-SPWM technique.

*5.1 PWM GENERATOR*

According to Figure 5.3, three states are considered. The first state is when the modulator signal is within the lowest carrier. The second state is when it is within the middle carrier. Finally, the third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements. According to this definition, the PWM logic was generated as shown in the figure 5.3

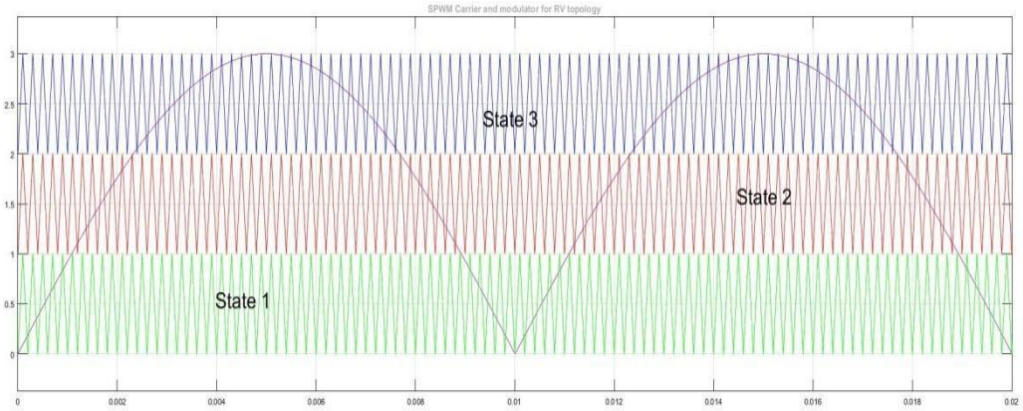



Figure 5.2: SPWM carrier and modulator for RV topology

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

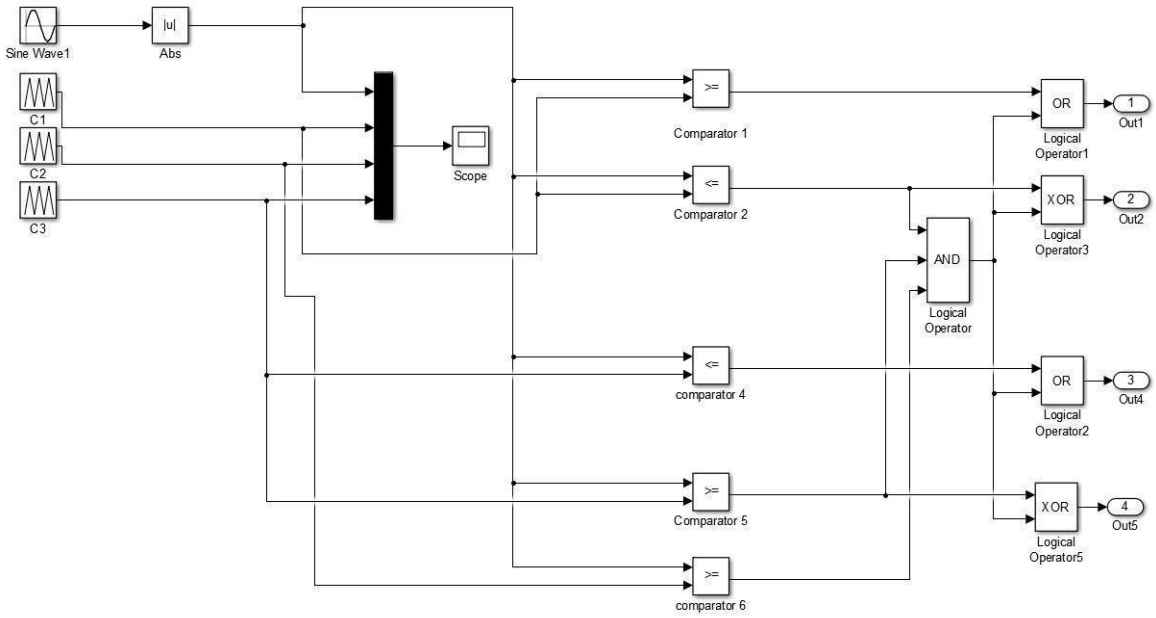



Figure 5.3: Carrier subsystem

The PWM pulses to different switches for level generation part are as shown in figure 5.4.The simulation was carried out and the waveforms of current and voltage waveforms were obtained. The load used is a 1 ohm resistor. The voltage waveform across 1 ohm resistor is shown in figure 4.4 and the waveform of current through 1 ohm resistor is shown in figure 5.5.

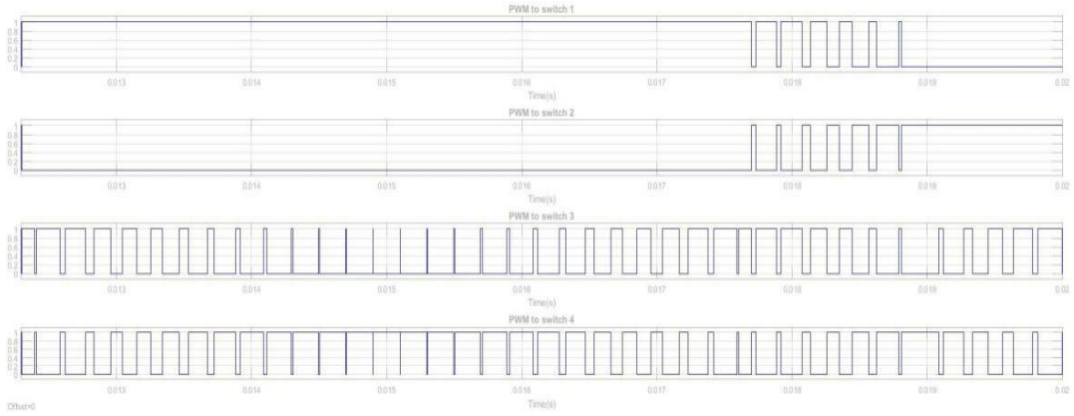



Figure 5.4: Gate signals for level generation part

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

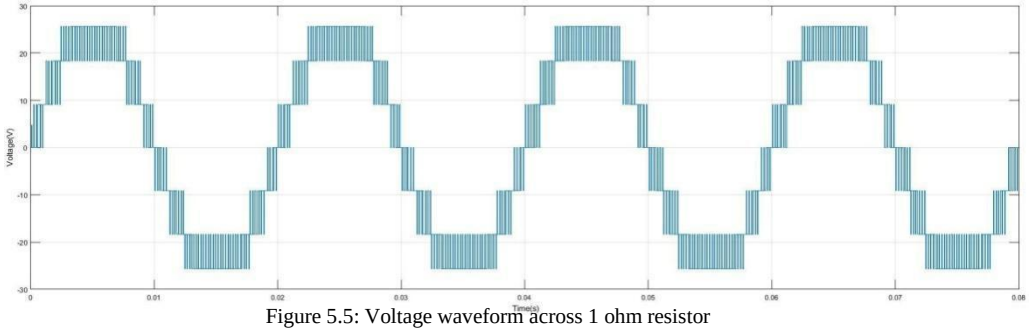



Figure 5.5: Voltage waveform across 1 ohm resistor

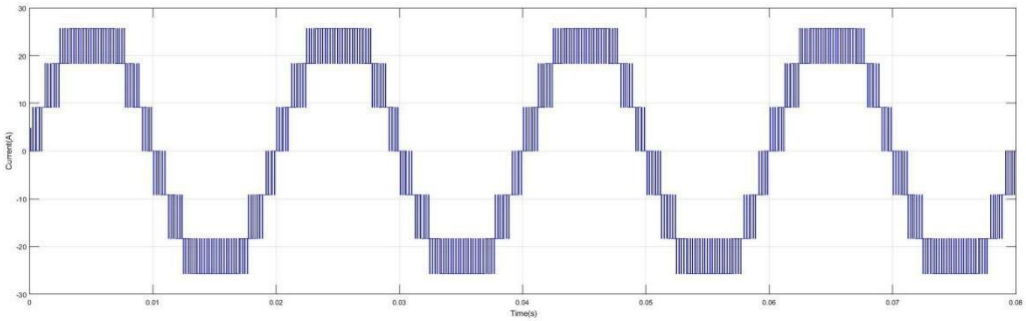



Figure 5.6: Current waveform through 1 ohm resistor

## CHAPTER 6
## THREE PHASE MULTILEVEL INVERTER

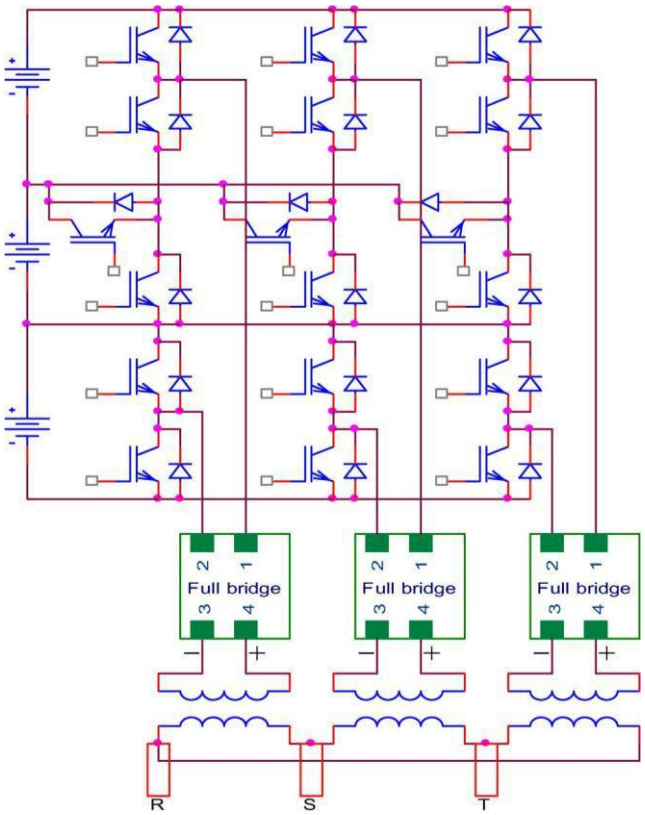



Fig.6.1. Three-phase RV multilevel topology.

This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig.6.1. Therefore, this topology is modular and can be easily increased to higher voltage levels by adding the middle stage in Fig.6.1. It can also be applied for three-phase applications with the same principle. This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. In Fig. 6.1, the complete three-phase inverter for seven levels is shown with a three-phase delta connected system. According to Fig. 6.1, the multilevel positive voltage is fed to the full-bridge converter to generate its polarity. Then, each full bridge converter will drive the primary of a transformer. The secondary of the transformer is delta(Δ) connected and can be connected to a three-phase system. This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient.

# CHAPTER 7
# HARDWARE RESULTS

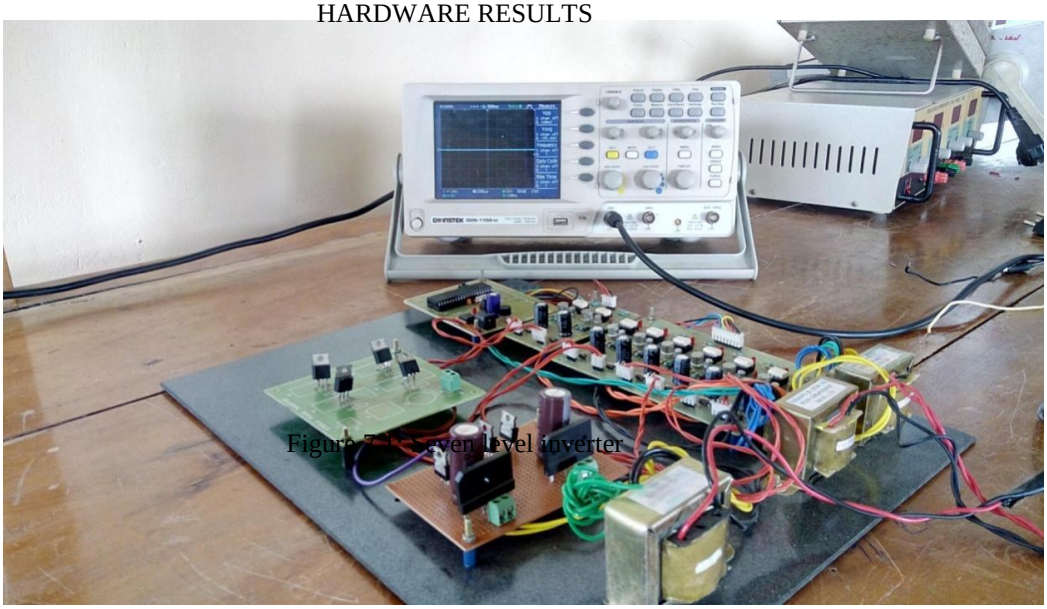


Figure 7.1 Seven level inverter

Complete model of seven level inverter is shown. Switches are triggered using PD-SPWM technique.

The laboratory prototype of seven level inverter is shown in figure 7.1. It consists of 8 MOSFET switches with its driver circuit. Driver circuit is used to provide 12V necessary for triggering of the switches as the pic output voltage is only 5V. The DC supply in the circuit is provided after rectification from a step down transformer of 230/12 and 230/24.

The model is designed to operate at a fixed frequency. The microcontroller used was PIC16F877A. There is a pic regulatory circuit used to step down transformer voltage of 12V to 5V required for the PIC IC. The 8 MOSFETS in the level generation part is connected to 8 output pins of port C of PIC.

Then this circuit is coupled to MOSFET driver circuit through an optocoupler. The gating signals from pic reach the MOSFETS through the driver circuit. Prototype of the model is made. The output voltage obtained in the DSO is shown in figure

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

*7.2. The output voltage obtained is nearly 24V.*

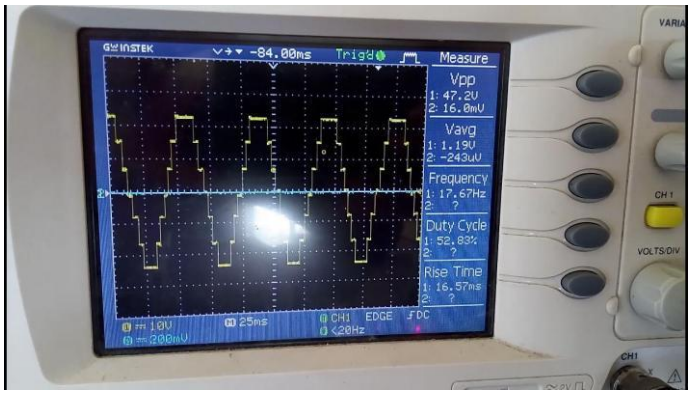



Figure 7.2: Output voltage waveform

## CHAPTER 8
## MULTILEVEL INVERTER TOPOLOGIES

There are several topologies of multilevel inverters available. The difference lies in the mechanism of switching and the source of input voltage to the multilevel inverters. Three most commonly used multilevel inverter topologies are:

1. Cascaded H-bridge multilevel inverters
2. Diode Clamped multilevel inverters
3. Flying Capacitor multilevel inverters

### *8.1. Cascaded H-Bridge Multilevel Inverters*

This inverter uses several H-bridge inverters connected in series to provide a sinusoidal output voltage. Each cell contains one H-bridge and the output voltage generated by this multilevel inverter is actually the sum of all the voltages generated by each cell i.e. if there are k cells in a H-bridge multilevel inverter then number of output voltage levels will be 2k+1. This type of inverter has advantage over the other two as it requires less number of components as compared to the other two types of inverters and so its overall weight and price is also less.

One phase of a cascaded H-bridge multilevel inverter

In single phase inverter, each phase is connected to single dc source. Each level generates three voltages which are positive, negative and zero. This can be obtained by connecting the AC source with the DC output and then using different combinations of the four switches. The inverter will remain ON when two switches with the opposite positions will remain ON. It will turn OFF when all the inverters switch ON or OFF. To minimize the total harmonic distortion, switching angles are defined and implemented. The calculations for the measurement of switching angle will remain the same. This inventor can be categorized further into the following types:

- 5 levels cascaded H Bridge Multilevel Inverter
- 9 levels cascaded H Bridge Multilevel Inverter

In 5 level cascaded H Bridge Multilevel Inverters, Two H Bridge Inverters are cascaded. It has 5 levels of output and uses 8 switching devices to control whereas in 9 level cascaded H Bridge Multilevel Inverters, Four H Bridge Invertors are cascaded. It has 9 output levels and use and use 16 switching devices.

Applications of Cascaded H-bridge Multilevel Inverters

Cascaded H Bridge Multilevel Inverters are mostly used for static var applications i.e., in renewable resources' of energy and battery based applications. Cascaded H Bridge Multilevel Inverters can be applied as a delta or wye form. This can be understood by looking at the work done by Peng where he used an electrical system parallel with a Cascade H Bridge. Here inverter is being controlled by regulating the power factor. Best application is when we used as photovoltaic cell or fuel cell. This is the example of Parallel connectivity of the H Bridge Multilevel Inverter.

### *8.2. Diode Clamped Multilevel Inverters*

Diode clamped multilevel inverters use clamping diodes in order to limit the voltage stress of power devices. It was first proposed in 1981 by Nabae, Takashi and Akagi and it is also known as neutral point converter. A k level diode clamped inverter needs (2k – 2) switching devices, (k – 1) input voltage source and (k – 1) (k – 2) diodes in order to operate. Vdc is the voltage present across each diode and the switch.

One phase of a diode clamped inverter

The concept of diode clamped inverter can better be understood by looking into three phase six level diode clamped inerter. Here the common dc bus is shared by all the phases, use five capacitors and six levels. Each capacitor has a voltage of Vdc and same is the voltage limit of switching devices. One important fact should be noted while considering the diode clamped inverter is that five switches will remain ON at any time. Six level, three phase dc clamped multilevel inverter is shown in the figure below.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

Advantages of Diode Clamped Multilevel Inverters

- Capacitance of the capacitors used is low.
- Back to back inverters can be used.
- Capacitors are pre charged.
- At fundamental frequency, efficiency is high.
- Disadvantages of Diode Clamped Multilevel Inverters
- Clamping diodes are increased with the increase of each level.
- Dc level will discharge when control and monitoring are not precise.

*8.3. Flying Capacitor Multilevel Inverters*

The configuration of this inverter topology is quite similar to previous one except the difference that here flying capacitors is used in order to limit the voltage instead of diodes. The input DC voltages are divided by the capacitors here. The voltage over each capacitor and each switch is Vdc. A k level flying capacitor inverter with (2k – 2) switches will use (k – 1) number of capacitors in order to operate.

A Flying Capacitor Multilevel Inverter with five voltage levels

If we compare above figures, it shows that the number of switches, main diodes and DC-bus capacitors are same in both the cases. The only difference between the two topologies is that the previous one uses clamping diodes in order to limit the voltage while this topology uses flying capacitors for this purpose, and as capacitors are incapable of blocking the reverse voltage, which diodes do, the number of switches also increases. Voltage on each capacitor is differing from the next as it has a ladder structure. Voltage difference between two back to back capacitors determines the voltage in the output frame.

Advantages of Flying Capacitor Multilevel Inverters

- Static var generation is the best application of Capacitor Clamped Multilevel Inverters.
- For balancing capacitors' voltage levels, phase redundancies are available.
- We can control reactive and real power flow.

Disadvantages of Flying Capacitor Multilevel Inverters

- Voltage control is difficult for all the capacitors
- Complex startup
- Switching efficiency is poor
- Capacitors are expansive than diodes

## CHAPTER 9
## HARMONICS ANALYSIS OF MULTILEVEL INVERTER

Harmonics are currents or voltages with frequencies that are integer multiples of the fundamental power frequency being 50 or 60Hz (50Hz for European power and 60Hz for American power). For example, if the fundamental power frequency is 50 Hz, then the 2nd harmonic is 100 Hz, the 3rd is 150 Hz, etc. In modern test equipment today harmonics can be measured up to the 63rd harmonics.

To give an understanding of this, consider a water piping system. Have you ever taken a shower when someone turns on the cold water at the sink? You experience the effect of a pressure drop to the cold water, reducing the flow of cold water. The end result is you get burned! Now imagine that someone at a sink alternately turns on and off the cold and hot water. You would effectively be hit with alternating cold and hot water! Therefore, the performance and function of the shower is reduced by other systems. This illustration is similar to an electrical distribution system with non-linear loads generating harmonics.

There are several industrial applications which may allow a harmonic content of 5% of its fundamental component of input voltage when inverters are used. Actually, the inverter output voltage may have harmonic content much higher than 5% of its fundamental component. In order to bring this harmonic content to a reasonable limit of 5%, one method is to insert filters between the load and inverter. If the inverter output voltage contains high frequency harmonics, these can be reduced by a low-size filter. For the attenuation of low-frequency harmonics, however, the size of filter components increases. This makes the filter circuit costly, bulky and weighty and in addition, the transient response of the system becomes sluggish. This shows that lower order harmonics from the inverter output voltage should be reduced by some means other the filter.

Harmonic Optimization Techniques in Multilevel VSI

One of the major problems in electric power quality is the harmonic contents. There are several methods of indicating the quantity of harmonic contents. The most widely used measure is the total harmonic distortion (THD). Various switching techniques have been used in static converters to reduce the output harmonic content.

We compare the two harmonic optimization techniques, known as optimal minimization of the total harmonic distortion (OMTHD) technique and optimized harmonic stepped-waveform (OHSW) technique used in multi-level inverters with unequal dc sources. Both techniques are very effective and efficient for improving the quality of the inverter output voltage. First, we describe briefly the cascaded H-bridge multi-level inverter structure.

Multi-level inverter is recently used in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

advantages of multi-level structure is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter output power. The output voltage waveform of a multi-level inverter is composed of a number of levels of voltages, typically obtained from capacitor voltage sources.

The so-called multi-level starts from three levels. As the number of levels increases, the output THD approaches zero. The number of achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Therefore, an important key in designing an effective and efficient multi-level inverter is to ensure that the total harmonic distortion (THD) in the output voltage waveform is small enough. The well-known multi-level inverter topologies are: cascaded H-bridge multi-level inverter, diode-clamped multi-level inverter and flying capacitor multi-level inverter. The multi-level inverter composed of cascaded H-bridges with separate dc sources (SDCSs), hereafter called a cascaded multi-level inverter, appears to be superior to the other multi-level topologies in terms of its structure that is not only simple and modular but also requires the least number of components. This modular structure makes it easily extensible to higher number of output voltage levels without undue increase in power circuit complexity. In addition, extra clamping diodes or voltage balancing capacitors are not necessary. It is generally accepted that the performance of an inverter, with any switching strategy, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms.Up to now, in multi-level technology, several well-known modulation techniques have been used as follows: Harmonic Optimization, Space Vector PWM (SV-PWM), and Carrier-Based PWM techniques.

The harmonic optimization techniques can be categorized into two methods: Optimal Minimization of the Total Harmonic Distortion (OMTHD) and Optimized Harmonic Stepped-Waveform (OHSW). OMTHD technique is based on minimization of THD by reducing all harmonics with no emphasis on any particular component, where as, OHSW is based on elimination of some specific harmonic components. In this paper, OMTHD and OHSW techniques are applied to a cascaded multi-level inverter with non-equal dc sources. Usually, it is assumed that the dc sources are all equal, which will not probably be the case in practice even if the dc sources are nominally equal. Here the dc sources are taken with different voltages for generality of the study. The study is performed for both cases focusing on harmonic content of the output voltage and the results obtained by the two techniques are compared. The paper is organized as follows: First the cascaded H-bridge multilevel inverter's structure and operation are briefly described. Then, the switching algorithms for the multilevel inverter, based on OHSW and OMTHD techniques are explained. Finally, the results obtained for the two techniques are analyzed and compared. Also, several informative results verify the effectiveness of both techniques in multi-level inverter with non-equal dc sources, clarifying the advantages of each technique.

Harmonics evaluation of single & multilevel inverter

| Harmonics | Harmonic factor of single inverter When $m_{a1}$=0.8,$m_{a2}$=0.8 | Harmonic factor of multilevel inverter when $m_{a1}$=o.8 , $m_{a2}$=0.8 | Harmonic factor of multilevel inverter when $m_{a1}$=0.8,$m_{a2}$=0.6 | Harmonic factor of multilevel inverter when $m_{a1}$=0.8,$m_{a2}$=0.4 |
|---|---|---|---|---|
| 1 | 77.96 | 155.9 | 136.4 | 116.8 |
| 3 | 0.07378 | 0.1541 | 0.1628 | 0.1617 |
| 5 | 0.04118 | 0.101 | 0.9879 | 0.09414 |
| 7 | 0.02814 | 0.08091 | 0.06048 | 0.05945 |
| 9 | 0.00674 | 0.04434 | 0.03065 | 0.05511 |
| 11 | 0.002845 | 0.03161 | 0.0354 | 0.03261 |
| 13 | 0.005282 | 0.03159 | 0.02703 | 0.02161 |
| 15 | 0.006377 | 0.01526 | 0.0145 | 0.03141 |
| 17 | 0.02244 | 0.01049 | 0.05138 | 0.0684 |
| 19 | 1.184 | 0.01774 | 0.9184 | 1.195 |
| 21 | 13.54 | 0.01739 | 6.727 | 11.3 |
| 23 | 30.82 | 0.009702 | 5.346 | 0.9306 |
| 25 | 30.86 | 0.01475 | 5.32 | 0.9174 |
| 27 | 13.53 | 0.02815 | 6.729 | 11.3 |
| 29 | 1.172 | 0.01386 | 0.9207 | 1.202 |

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

| | | | | |
|---|---|---|---|---|
| 31 | 0.01346 | 0.01426 | 0.04191 | 0.06479 |
| 33 | 0.02282 | 0.02411 | 0.02008 | 0.03249 |
| 35 | 0.01417 | 0.03323 | 0.04444 | 0.0267 |
| 37 | 0.01494 | 0.05213 | 0.03986 | 0.02206 |
| 39 | 0.01513 | 0.2844 | 0.149 | 0.1193 |
| 41 | 1.647 | 3.272 | 1.931 | 1.617 |
| 43 | 8.169 | 16.32 | 6.729 | 8.707 |
| 45 | 11.32 | 22.61 | 0.9207 | 18.02 |
| 47 | 10.21 | 20.35 | 0.04191 | 5.261 |
| 49 | 10.21 | 20.37 | 0.02008 | 5.2791 |
| 51 | 11.33 | 22.62 | 24.2 | 18.03 |
| 53 | 8.15929 | 16.31 | 11.39 | 8.707 |
| 55 | 1.65 | 3.274 | 1.929 | 1.616 |
| 57 | 0.1443 | 0.2709 | 0.1099 | 0.1014 |
| 59 | 0.01911 | 0.03362 | 0.3192 | 0.05269 |
| 61 | 0.2963 | 0.02776 | 0.3285 | 0.3523 |
| 63 | 1.878 | 0.03805 | 1.616 | 1.893 |
| 65 | 5.913 | 0.02344 | 3.929 | 5.758 |
| 67 | 5.847 | 0.01814 | 1.071 | 3.698 |
| 69 | 5.406 | 0.003869 | 9.975 | 13.93 |
| 71 | 2.941 | 0.005309 | 9.72 | 2.175 |
| 73 | 2.946 | 0.01203 | 9.741 | 2.165 |
| 75 | 5.378 | 0.01587 | 9.979 | 13.9 |
| 77 | 5.86 | 0.01547 | 1.063 | 3.738 |

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

*Applications in Harmonic Elimination*

The present chapter helps us to understand the effects of non-linear loads on the power system and the implementation of suitable devices to cancel out the harmonics. The use of inverters in active power filters has been emphasized and the simulated circuits and results have been described in particular.

*Non Linear Loads*

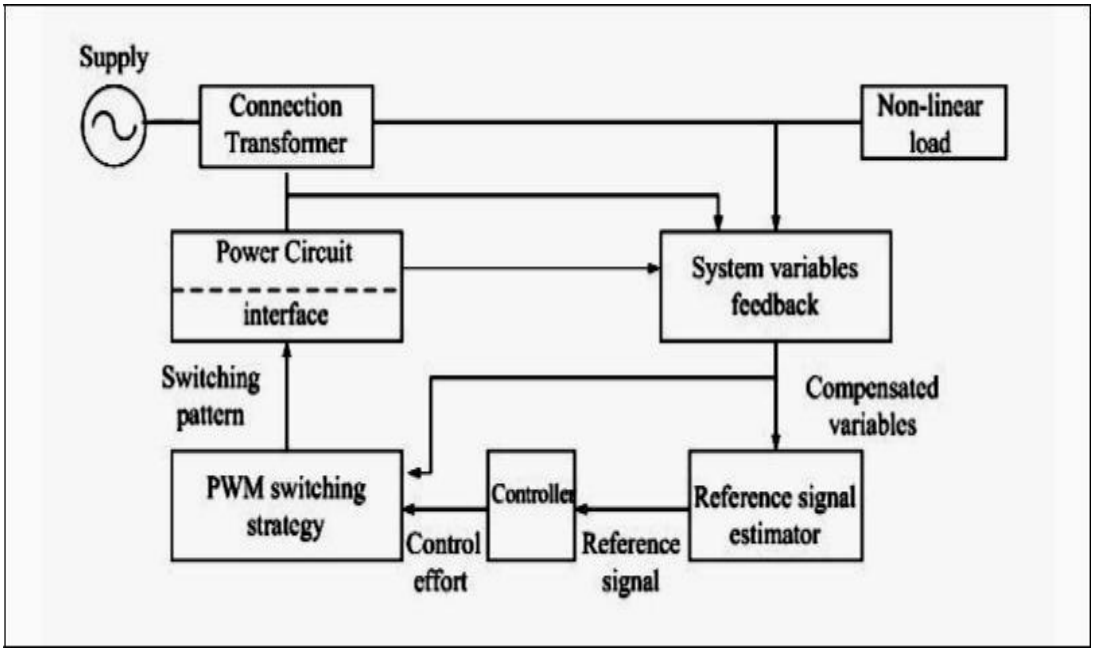
A non-linear load on a power system is typically a rectifier or some kind of arc discharge device such as a fluorescent lamp, electric welding machine, or arc furnace in which current is not linearly related to the voltage. Because current in these systems is interrupted by a switching action, the current contains frequency components that are multiples of the power system frequency. This leads to distortion of the current waveform which in turn distorts the voltage waveform. Distortion power factor is a measure of how much the harmonic distortion of a load current decreases the average power transferred to the load.

*Active Power Filters*

The increasing use of power electronics based loads (adjustable speed drives, switch mode power supplies, etc.) to improve system efficiency and controllability is increasing the concern for harmonic distortion levels in end use facilities and on the overall power system. The application of passive tuned filters creates new system resonances which are dependent on specific system conditions.

In general, passive tuned filters have been used to minimize low-frequency current harmonics while high-pass units have been connected to attenuate the amplitude of high frequency current components. However, high-pass filters present disadvantages due to the resistance connected in parallel to the inductor, which increases the filter losses and reduces the filtering effectiveness at the tuned frequency. The most critical aspects of passive filters are related to the fact that they cannot modify their compensation characteristics following the dynamic changes of the nonlinear load, the performance dependence they present with the power system parameters, and the probability of series resonances with the power system's equivalent reactance. Passive filter ratings must be coordinated with reactive power requirements of the loads and it is often difficult to design the filters to avoid leading power factor operation for some load conditions.

Also, the passive filter generates at fundamental frequency reactive power that changes the system voltage regulation, and if the filter is not designed properly or disconnected during low load operating conditions, over-voltages can be generated at its terminals. A flexible and versatile solution to voltage/current quality problems is offered by active power filters. Active filters have the advantage of being able to compensate for harmonics without fundamental frequency reactive power concerns. This means that the rating of the active power can be less than a conquerable passive filter for the same nonlinear load and the active filter will not introduce system resonances that can move a harmonic problem from one frequency to another.



International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

*9.1 Generalized block diagram for active power filter*

Figure shows the components of a typical active-power-filter system and their interconnections. The information regarding the harmonic current, generated by a nonlinear load, for example, is supplied to the reference-current/voltage estimator together with information about other system variables. The reference signal from the current estimator, as well as other signals, drives the overall system controller. This in turn provides the control for the PWM switching-pattern generator. The output of the PWM pattern generator controls the power circuit via a suitable interface. The power circuit in the generalized block diagram can be connected in parallel, series or parallel/series configurations, depending on the connection transformer used.

Shunt Active Power Filters

The purpose of the shunt active power filters is to cancel load harmonics fed to the supply. It can also contribute to reactive-power compensation and balancing of three phase currents. Shunt active power filters compensate current harmonics by injecting equal-but-opposite harmonic compensating current. In this configuration active power filter operates as a current source injecting the harmonic components generated by the load but phase shifted by 180o. This principle is applicable to any type of load considered a harmonic source. Moreover, with an appropriate control scheme, the active power filter can also compensate the load power factor. In this way, the power distribution system sees the non linear load and the active power filter as an ideal resistor.

Parallel filters have the advantage of carrying only the compensation current plus a small amount of active fundamental current supplied to compensate for system losses. It is possible to connect several filters in parallel to cater for higher currents, which makes this type of circuit suitable for a wide range of power ratings

Modelling of Three Wire Shunt Active Power Filter

The concept of using active power filters to mitigate harmonic problems and to compensate reactive power was proposed more than two decades ago. Since then the theories and applications of active power filters have become more popular and have attracted great attention. Without the drawbacks of passive harmonic filters, the active power filter appears to be a viable solution for reactive power compensation as well as for eliminating harmonic currents.

Active power filters are researched and developed as a viable alternative over the passive filters and static var compensators to solve the problems of harmonics injection and reactive power requirement of non-linear loads .Among the various topologies developed the shunt active power filter based on the current controlled voltage source type PWM converter has proved to be effective even when the load is highly non-linear.

The control strategies of the active filters are implemented mainly in three steps – Signal conditioning, estimation of compensating signals and generation of firing signals for switching devices. Estimation of compensating signal is the most important part of the active filter control. It has a great impact on the compensating objectives, rating of active filters and its transient as well as steady state performance. The control strategies use either frequency domain or time domain approaches to extract compensating signals from the corresponding distorted currents/voltages.

Role of Inverters in Active Filters

The voltage source inverter used in the active power filter makes the harmonic control possible. This inverter uses a dc capacitor as the supply and can switch at a high frequency to generate a signal which will cancel the harmonics from the nonlinear load.

The current waveform for cancelling harmonics is achieved with the voltage source inverter(IGBT based) and an interface reactor.The interface reactor converts the voltage signal created by the inverter to a current signal.The desired waveform is obtained by accurately controlling the switches in the inverter. Control of the current wave shape is limited by the switching frequency of the inverter and by the available driving voltage across the interface reactor. The driving voltage across the interface reactor determines the maximum di/dt that can be achieved by the power filter. This is important because relatively high values of di/dt may be needed to cancel higher order harmonic components.

The voltage source inverter is the heart of the active power filter. In the system model of the project it has been modelled as a three phase full wave inverter (IGBT based). Each of the three identical inverter legs consisted of two IGBT and two anti-parallel diodes. The igbt used here is modelled in the simulink as a resistor (Ron) and inductor (Lon) in series with a switch(transistor) controlled by a logical signal. It switches between on and off state instantaneously when triggered.

## CHAPTER 10
## CONCLUSION

A new inverter topology is used which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. Here, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the internal prototype. The experimental results of the developed prototype for a seven-level inverter of this topology is included. The results clearly show that the topology can e effectively work as a multilevel inverter with a reduced number of switches. Overall number of components is reduced in this

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 04, April-2017

topology and thus the circuit becomes less complex. The absence of voltage balancing problem makes the circuit more efficient.

REFERENCES

[1] Ehsan Naja ,Abdul Halim Mohamed Yatim, \Design and Implementation of a New Multilevel Inverter Topology ", IEEE Trans. Ind Applicaton, , vol. 59, no. 11, Nov 2012.

[2] K. Jang-Hwan, S.-K. Sul, and P. N. Enjeti \ A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltagesource inverter ", IEEE Trans. Ind. Appl.vol. 44, no. 4, pp. 12391248, Jul./Aug. 2008.

[3] W. Chen, A. Huang, C. Li, et al, \DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application", IEEE Trans. Power Elec-tron.,,vol. 28, no. 4, pp. 20142023,2013.

[4] A. Parastar, A. Gandomkar, M. Jin, and J. Seok, Multilevel converters for large electric drives,, IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 3644, Jan./Feb. 1999

[5] X. Yun, Y. Zou, X. Liu, and Y. He, \A novel composite cascade multilevel con-verter,", IET Power Electron.,vol.2, no. 6, pp. 675685, 2009.

[6] G. S. Perantzakis, F. H. Xepapas, and S. N. Manias, \A novel four-level volt-age source inverter-in uence of switching strategies on the distribution of power losses", IEEE Trans. Power Electronvol. 22, no. 1, pp. 149159, Jan. 2007

[7] N. A. Rahim, K. Chaniago, and J. Selvaraj,, \Single-phase seven-level grid-connected inverter for photovoltaic system", IEEE Trans. Ind. Electron.,,vol. 25, no. 4, pp. 21642173, 2010.

[8] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi,, \A reduced switch-count ve-level inverter with common-mode voltage elimination for an open-end winding induction motor drive,", IEEE Trans. Ind. Electron.,,vol. 29, no. 1, pp. 444452, 2014.

[9] E. Beser, B. Arifoglu, S. Camur, and E. K. Beser, \Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source,J. Power Electron.,,vol. 10, no. 2, pp. 138145, Mar. 2010.

[10] G. Shahgholiyan, E. Haghjou, and S. Abazari,, \Improving the mitigation of volt-age icker by usage of fuzzy control in a distribution static synchronous compen-sator (DSTATCOM),", Majlesi J. Elect. Eng.,,, vol. 3, no. 2, pp. 2535, Jun. 2009.

[11] G. M. Martins, J. A. Pomilio, S. Buso, and G. Spiazzi, \Three-phase lowfrequency commutation inverter for renewable energy systems", IEEE Trans. Ind. Elec-tron.,,vol. 53, no. 5, pp. 15221528, Oct. 2006.

[12] G.-J. Su, \Multilevel dc-link inverter", IEEE Trans. Ind. Electron.,,vol. 41, no. 3, pp. 848854, May/Jun. 2005.

[13] C. Cecati, F. Ciancetta, and P. Siano, \A multilevel inverter for photovoltaic systems with fuzzy logic control ", IEEE Trans. Ind. Electron., , vol. 57, no. 12, pp. 41154125, Dec. 2010..

[14] A. Radan, A. H. Shahirinia, and M. Falahi, `Evaluation of carrier-based PWM methods for multi-level inverters", in Proc. IEEE ISIE,2007, pp. 389394..

[15] Y.-M. Park, H.-S. Ryu, H.-W. Lee, M.-G. Jung, and S.-H. Lee,,"Design of a cas-caded H-bridge multilevel inverter based on power electronics building blocks and control for high performance,", IEEE Trans. Ind. Electron., vol. 10, no. 3, pp. 262269, May 2010.