Micro and Nano Engineering 3 (2019) 59–81

Contents lists available at ScienceDirect

Micro and Nano Engineering

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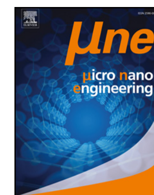
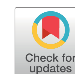


Research paper

3D GaN nanoarchitecture for field-effect transistors



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ARTICLE INFO

Keywords:
GaN
3D architecture
Nanowire
Nanofin
Nanoelectronics
Field-effect transistor (FET)
Vertical transistor
Lateral transistor

ABSTRACT

The three-dimensionality of 3D GaN field-effect transistors (FETs) provides them with unique advantages compared to their planar counterparts, introducing a promising path towards future FETs beyond Moore's law. Similar to today's Si processor technology, 3D GaN FETs offer multi-gate structures that provide excellent electrostatic control over the channel and enable very low subthreshold swing values close to the theoretical limit. Various concepts have been demonstrated, including both lateral and vertical devices with GaN nanowire (NW) or nanofin (NF) geometries. Outstanding transport properties were achieved with laterally contacted NWs that were grown in a bottom-up approach and transferred onto an insulating substrate. For higher power application, vertical FETs based on regular arrays of GaN nanostructures are particularly promising due to their parallel integration capability and large sidewall surfaces, which can be utilized as channel area. In this paper, we review the current status of 3D GaN FETs and discuss their concepts, fabrication techniques, and performances. In addition to the potential benefits, reliability issues and difficulties that may arise in complex 3D processing are discussed, which need to be tackled to pave the way for future switching applications.

1. Introduction

Gallium nitride (GaN)-based field-effect transistors (FETs) are expected to exhibit outstanding performances in high-frequency and high-voltage operations due to the excellent material properties of III-nitrides, such as large band gap, high critical field, high electron mobility, and high saturation electron velocity (Fig. 1) in comparison to silicon (Si) and silicon carbide (SiC) counterparts. AlGaN/GaN-based heterostructure field-effect transistors (HFETs) utilize the excellent transport properties of the polarization field induced two-dimensional electron gas (2DEG), making them ideal for high-frequency operation. Substantial progress was achieved within the last decades in suppressing the problematic trapping related phenomena of current collapse [1–5] as well as in obtaining *E*-mode HFETs by depleting the usually present 2DEG at zero gate bias using different methods such as recess gate [6], p-GaN gate [7–9] or fluorine implantation [10], which consequently had led to their commercialization. More recently, vertical GaN transistors have attracted great attention for future power electronics, since their blocking voltage is scalable independent from the used chip area, and many devices with remarkable breakdown voltages above 1.2 kV were demonstrated [11,12].

Finally, another group of device concepts has been introduced through the use of GaN nanostructures, offering a number of unique advantages that can help to significantly improve the performance of GaN transistors. High aspect-ratio nanowire (NW) and nanofin (NF) structures can be grown epitaxially or etched down from planar substrates, providing large areas at their sidewalls, which can be utilized for LEDs [13], sensing applications [14], or serve as channel area for transistor devices. Their small footprint enables relaxation of strain induced by lattice mismatch [15]. Furthermore, dislocation elimination processes occur during 3D growth allowing bottom-up GaN nanostructures to be free of extended defects [16]. When used for vertical FETs, the gate length as well the length of the drift region can be controlled by the height of the nanostructures and is completely independent of the chip area. The three-dimensionality of the structures brings additional advantages for the realization of enhancement mode (*E*-mode) devices, which are usually favored for safe switching conditions, as surface Fermi level pinning acts depleting on the GaN nanostructures, mainly depending on their diameter and doping concentration [17]. 3D FETs with both depletion mode (D-mode) and *E*-mode operation were reported with threshold voltages ranging between −30 V and 2.5 V. Finally, as known from modern Si MOSFETs [18],

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https://doi.org/10.1016/j.mne.2019.04.001
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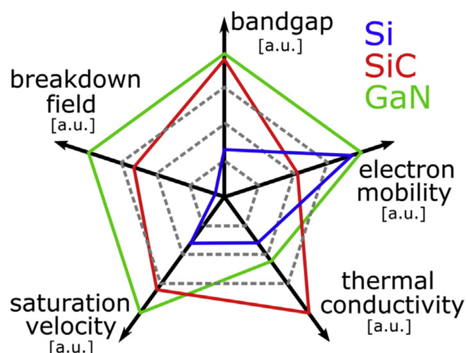

Fig. 1. Comparison of the relevant material properties for Si, SiC and GaN power electronics.

multigate technologies such as wrap-around gates for NWs or trigates for NFs can efficiently improve the electrostatic channel control, resulting in a very low subthreshold swing (SS) and reduced short channel effects [19]. Moreover, nanostructures can improve both the linearity [99,141,149] and thermal performance [138,140] of transistors, as will be discussed later.

These potential advantages suggest that GaN nanostructures should be considered for future transistor technology. The promising performances achieved by various 3D GaN devices discussed in this article underline their benefits for GaN electronics.

2. Advanced 3D device architectures

2.1. Lateral 3D GaN FETs

2.1.1. Lateral nanofin FETs

Recently, fin-based device structures have been extensively investigated to overcome the theoretical limitations of conventional planar device structures. GaN-based lateral NF FET structures were fabricated to reduce the short channel effects and leakage current as well as to obtain better gate controllability. In 2009, Ohi and Hashizume reported that the threshold voltage of the AlGaN/GaN high-electronmobility transistor (HEMT) is shifted in the positive direction with better OFF-state device characteristics [20]. They developed an AlGaN/GaN multi-mesa-channel (MMC) with the periodic trenches and parallel mesa-shaped channels (Fig. 2a). Firstly, the fin patterns are formed by the electron beam lithography on AlGaN/GaN heterostructure and followed by the reactive-ion-beam etching. The height of the mesa channel is 50–70 nm and the width of the channels is varied from 50 to 200 nm.

A novel tri-gate GaN MISFET for normally-off operation was reported for the first time (Fig. 2b) by Palacios *et al.* [21]. The device was designed combining the 3D tri-gate structure and a submicrometer gate recess to achieve the normally-off device. The Cl_2-based plasma etching was employed for the formation of trench (30 nm-deep). A dual dielectric stack with SiO_2/Al_2O_3 was deposited after the UV-ozone treatment. The authors showed the suppression of short-channel effects using the tri-gate device structure with a sub-micrometer gate length. In 2011, AlGaN/GaN nanoribbons (Fig. 2c) have been fabricated using top-down approach by Palacios *et al.* [22]. The arrays of AlGaN/GaN nanoribbons are patterned between the two Ohmic contacts by using electron-beam lithography and followed by reactive ion etching to etch away the material in between adjacent nanoribbons by using BCl_3/Cl_2 gas. The authors opted for very slow etch rate technique to reduce the plasma damage.

Similar studies were reported by Lee. *et al.* in 2013 [23], in which they studied the single-nanoribbon AlGaN/GaN metal-insulator-semiconductor FET (MISFET). The device fabrication is similar to that presented in [20], which began with the patterning of the nanoribbon-shaped structure on AlGaN/GaN heterostructure and subsequent transformer coupled etching (TCP) using BCl_3/Cl_2 gas mixture. Tetramethyl ammonium hydroxide (TMAH) solution was used to eliminate the plasma damage from the etched GaN surface. This was followed by the gate dielectric deposition (Al_2O_3) and formation of Ohmic and gate contacts. The width and height of the nanoribbon are 90 and 250 nm, respectively. The schematic and the TEM images of the single-nanoribbon AlGaN/GaN MISFET are shown in Fig. 2d. In 2013, the same group fabricated GaN junctionless NF FET for the first time as shown in Fig. 2e [24]. The Si-doped *n*-type GaN layer on a high resistive undoped GaN/Sapphire template was used for the device fabrication. The device architecture and fabrication process are quite similar to [23]. The authors state that the current flows through the volume of the heavily doped GaN fin rather than at the surface channel, which greatly improves device performances by eliminating the adverse effects related to the interface quality. They also compared the devices performances with and without AlGaN/GaN heterostructure [26]. It was shown that, the GaN NF FETs with AlGaN heterostructure exhibited lower on-resistance than that of heterojunction-free GaN NF FET. On the other hand, the GaN junctionless NF FET exhibited excellent off-state performances because the current flows in the heavily doped volume of the fin.

To further improve the off-state performances, the authors also fabricated omega gate nanowire fin FET for the first time [25], in which TMAH solution played a crucial role. This novel device is fabricated using the two-step dry etching and followed by the wet chemical etching. The HfO_2 sacrificial layer protects the top and sidewalls of the fin structure, whereas the buffer layer is etched. The longer (10 h) time etching in anisotropic TMAH solution led to the formation of omega gate device structure. The detailed processing steps of fabrication were shown in Fig. 2f. The authors claimed that the improved on/off performances were observed than the conventional fin structures, due to the fully-depletion of the active region and reduced leakage paths between GaN buffer layer and 2DEG channel.

2.1.2. Lateral nanowire FETs

The first lateral 3D GaN NW FETs were reported in 2002 by Huang *et al.*, who demonstrated a D-mode (normally-on) FET based on a single GaN NW (Fig. 3a) [27]. The GaN NWs were synthesized by a laser catalytic growth bottom-up method [28,29]. The nominally undoped NWs with diameters of 17.6 nm and heights of 10 µm showed electron concentrations in the range of $10^{18} - 10^{19}\ cm^{-3}$, which was attributed to nitrogen vacancies and oxygen impurities [27]. The NWs were placed on an oxidized silicon substrate by dispersing a NW/ethanol suspension. Ohmic Ti/Au (50/70 nm) drain and source contacts were formed by electron beam lithography.

A similar D-mode lateral GaN NW FET was demonstrated by Motayed *et al.* in 2006 using 200 µm long GaN NWs with diameters of 50–300 nm [30]. Here, a dielectrophoretic method was applied to distribute the NWs between the predeposited Ti/Al/Ti (30/100/30 nm) source and drain pads (Fig. 3b), followed by a top metallization (Fig. 3c). Different NW lengths (10–80 µm) and diameters (50–300 nm) were compared, and lower electron mobilities (μ) were found for smaller NW diameters due to enhanced surface scattering, affecting the maximum drain current $I_{d,max}$ (see Table 1) [31].

In the same year, Cha *et al.* developed the lateral GaN NW FETs using a top- and bottom-gate structure with 20–40 nm thick NWs (Si-doped GaN of $1.44 \times 10^{19}\ cm^{-3}$) fabricated in a bottom-up approach, as shown in Fig. 3c [32]. Ti/Al/Mo/Au was used as drain and source contact, the substrate was employed as bottom-gate and a Ni/Au omega like gate was deposited on top of the NWs. The breakdown voltage (BV) measurements show a BV value of around 60 V, which is higher than that of the bottom-gate FETs (i.e., 15 V). A gate memory effect was found on these FETs which is attributed to the surface charging on the GaN NW sidewalls enhanced by the higher trap states on oxide layer due to the oxide quality grown by plasma enhanced chemical vapor

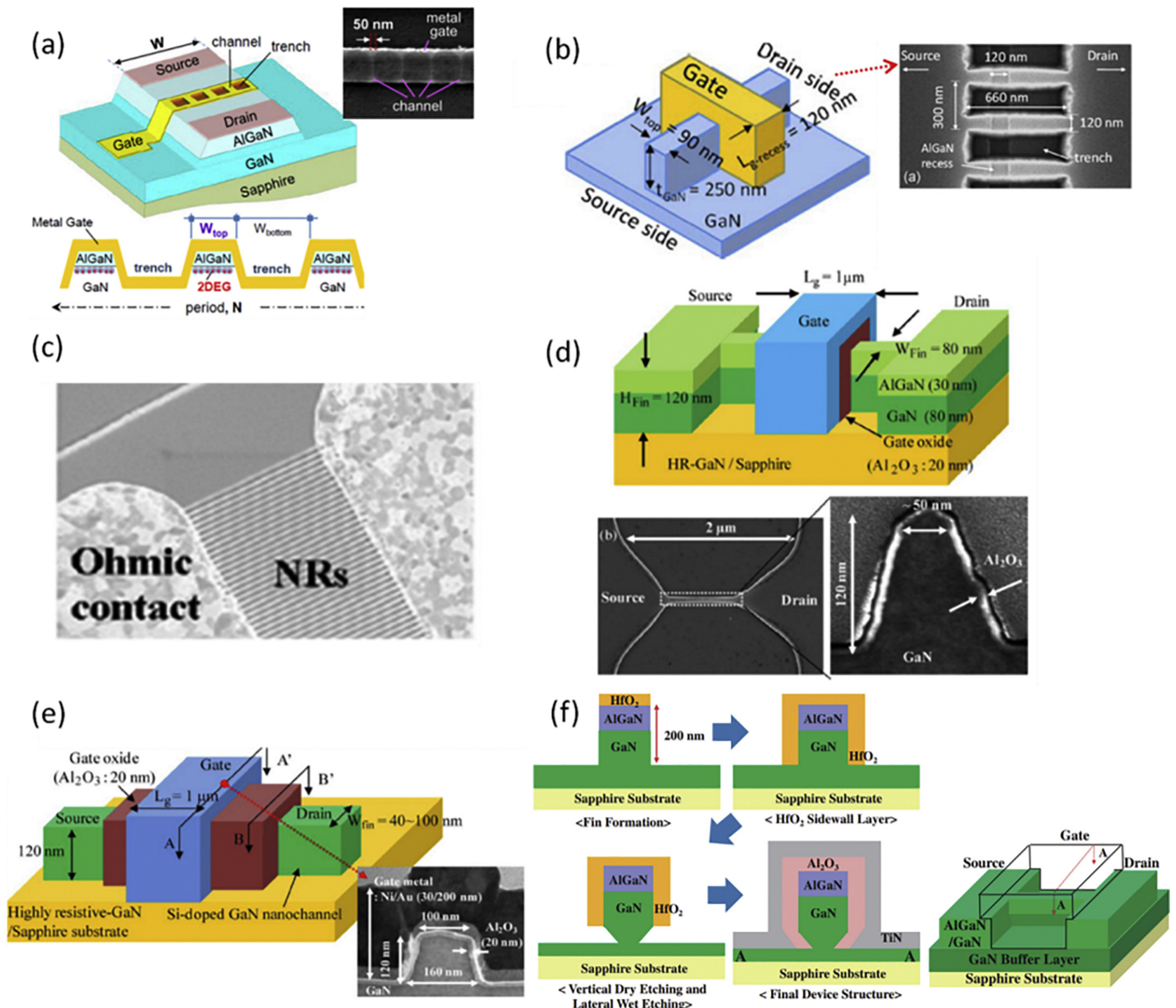

Fig. 2. (a) Schematic illustration of the MMC HEMT showing the periodic trench structure and cross-sectional SEM image in the inset. © [2013] IEEE. Reprinted, with permission, from [20]. (b) Schematic of the normally-off channel region and its cross-sectional SEM image in the inset. © [2012] IEEE. Reprinted, with permission, from [21]. (c) SEM image of GaN nanoribbons. Reprinted from [22], with the permission of AIP Publishing. (d) Schematic of single-nanoribbon triple-gate Al_2O_3/GaN MISFET, including top-view SEM images and cross-sectional TEM image. © [2013] IEEE. Reprinted, with permission, from [23]. (e) Schematic of GaN nanochannel fin FET including device dimensions and cross-sectional TEM image in the inset. © [2013] IEEE. Reprinted, with permission, from [24]. (f) Schematic of AlGaN/GaN omega shaped NF FET and its fabrication process flow [25]. Copyright 2015 The Japan Society of Applied Physics.

deposition (PECVD) [32].

A new type of NW FETs was introduced by Li *et al.* in 2006 who employed epitaxially grown core-shell GaN/AlN/AlGaN NWs into lateral D-mode high electron mobility transistors (HEMTs) [33]. Similar to planar HEMTs, the high mobility from the low-dimensional electron gas at the GaN/AlN interface enables excellent transport properties. Using these devices with top gated structure, they could obtain high $g_{m,max}$, around 500 mS/mm. Fig. 3d represents the TEM image of the device showing the composition of GaN/AlN/AlGaN triangular NW grown by MOCVD on a bulk GaN. The NW has a diameter of 100 nm and a length of 10–20 μm. A 6 nm-thick ZrO_2 with high-*k* of 22 ± 3 was used as a dielectric material to enhance the passivation (Fig. 3e) [34]. The high electron mobility μ in this HEMT is caused by the 1-dimension electron gas on the interface between the undoped GaN and AlN/AlGaN, which was endorsed by internal electric field formed by piezoelectric polarization in GaN core AlN/AlGaN shells. This condition has resulted in the $g_{m,max}$ of 420 mS/mm with μ of 3100 cm^2/Vs at room temperature [35]. The g_m in this value was normalized by the gate width of 0.1 μm as the NW diameter. The authors attributed the subthreshold characteristic close to ideal subthreshold swing (SS) at room temperature (K_BT/e ln (10)) of 68 mV/dec (Fig. 3f) [33].

Other D-mode lateral GaN NW devices were introduced by Blanchard *et al.* in 2008 as single GaN NW metal-semiconductor FETs (MESFETs) employing Pt/Au as a Schottky gate with similar top gate structure like the devices from Cha *et al.* [36]. They developed 10 single lateral NW FETs with the wire diameters of 210–470 nm and lengths of 11–19 μm. Ti/Al (20/200 nm) metal layers were used as source and drain contact electrodes and 30/300 nm Pt/Au films as gate metal contact electrode. The transfer of the fabricated NW on the foreign substrate and its alignment to drain source contact were conducted using dielectrophoresis method [37]. The typical SS of this device is 75 mV/dec, whereas average SS values from 10 FETs are 70 mV/dec.

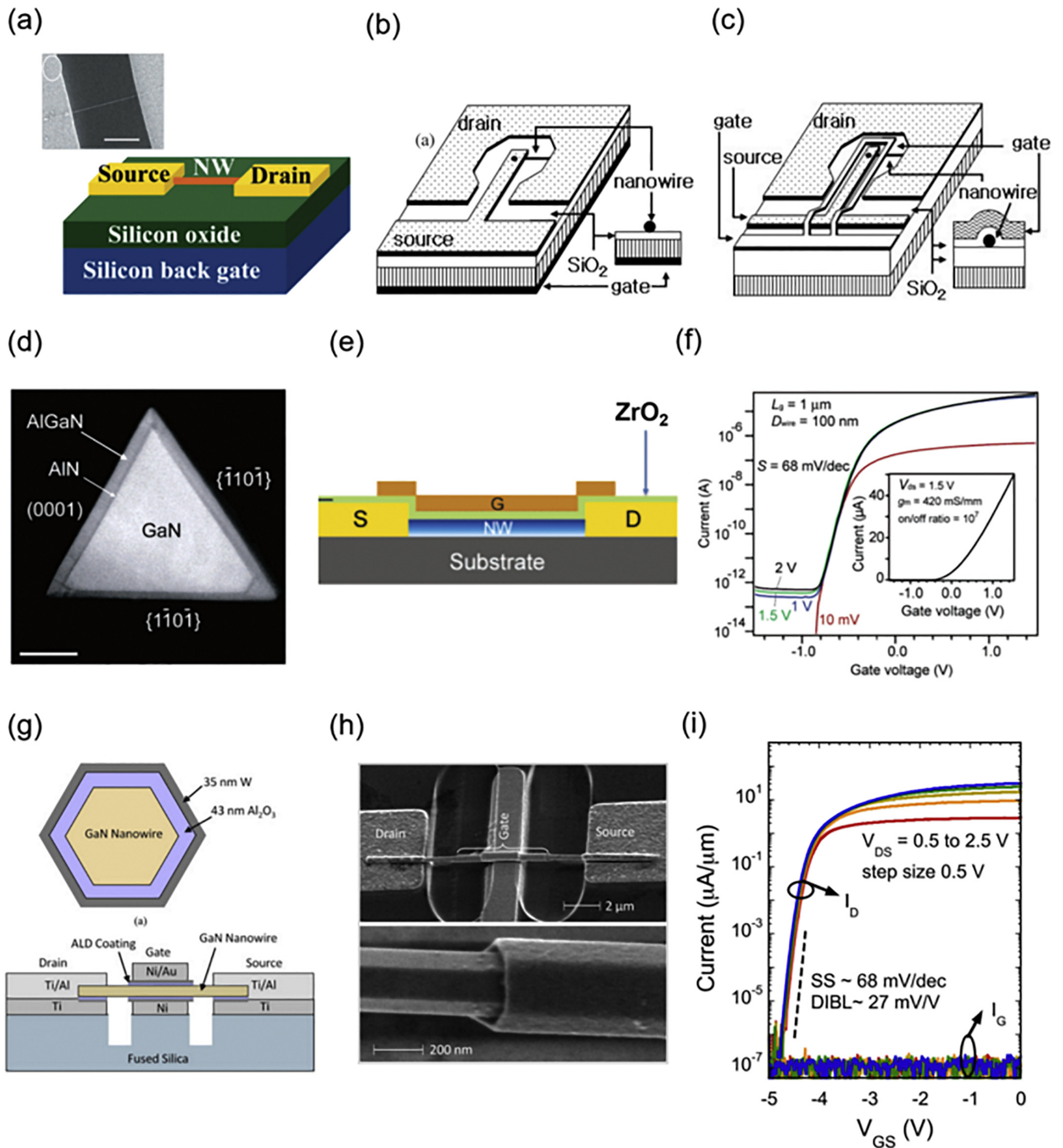

Fig. 3. (a) Lateral 3D GaN NW FET schematic with drain and source side by side from Huang *et al.* Reprinted with permission from [27]. Copyright (2006) American Chemical Society. 3D schematics of lateral GaN NW FETs with (b) bottom gated and (c) top gated structures from Cha *et al.* [32]. © IOP Publishing. Reproduced with permission. All rights reserved. (d) A high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of GaN/AlN/AlGaN NW (scale bar = 50 nm), (e) schematic of lateral GaN NW HEMT, and (f) logarithmic transfer characteristics of GaN/AlN/$Al_{0.25}Ga_{0.75}N$ NW HEMTs with diameter of 100 nm and L of 1 nm with inset of linearly I_dV_g at V_{ds} of 1.5 V from Li *et al.* Reprinted with permission from [33]. Copyright (2006) American Chemical Society. (g) A 2D cross-sectional schematic of single lateral GaN NW FETs, (h) an SEM image of the device as seen from top and inset of gate area from Blanchard *et al.* © [2012] IEEE. Reprinted, with permission, from [38]. (i) Lateral GaN NW FETs transfer characteristics with SS of 68 mV/dec from Li *et al.* © [2018] IEEE. Reprinted, with permission, from [40].

Table 1
Comparison of fabricated 3D GaN FETs based on nanowires and nanofins created in lateral and vertical architectures.

Ref.	FET structure	Substrate	N	D nm	L µm	V_{th} V	BV V	$I_{d,max}$ µA	$I_{d,max}$ mA/mm	$g_{m,max}$ mS/mm	I_{on}/I_{off}	SS mV/dec	R_{on} mΩcm²
Huang et al. 2002 [27]	Lateral NW FET	Silicon	1	17.6	3	−8	–	2	111	22	–	–	–
Cha et al. 2006 [32]	Lateral top-gate NW FET	Silicon	1	33	3	−7.5	60	1.8	35	–	–	–	–
Cha et al. 2006 [32]	Lateral bottom-gate NW FET	Silicon	1	33	4	−12.5	15	3.5	106	–	–	–	–
Motayed et al. 2006 [30]	Lateral NW FET	Silicon	1	95	35	−30	–	0.8	8.4	1.1	–	–	–
Blanchard et al. 2008 [36]	Lateral NW FET	Silicon	1	290	2	−3.7	–	12	57	8.2	10^8	63	
Blanchard et al. 2012 [38]	Lateral NW FET	Silicon	1	210	2	−5.5	–	50	240	48	10^8	190	
Gačević et al. 2016 [39]	Lateral NW FET	Silicon	1	90	0.3	−0.7	–	5	56	22	–	–	–
Li et al. 2006 [33]	Lateral NW HEMT	Bulk GaN	1	100	1	−0.5	–	50	500	420	10^7	68	–
Li et al. 2018 [40]	Lateral NW FET	Silicon	1	146	0.3	−4.2		9.6	42	10.5	10^8	68	
Lee et al. 2013 [24]	Lateral junctionless FinFET	Sapphire	5	60	1	0	280	–	670	168	10^8	68	1.3
Lee et al. 2015 [25]	Lateral Omega gate FinFET	Sapphire	36	50	5	−1	–	–	450	432	10^{10}	62	0.19
Lee et al. 2014 [98]	Lateral junctionless FinFET	Sapphire	5	200	0.35	−5.8	–	–	403	123.6	–	–	–
Lee et al. 2015 [99]	Lateral FinFET	Sapphire	100	150	5	−1	400	–	1250	155	10^8	58	–
Chen et al. 2017 [100]	Lateral FinFET	SiC	625	152	0.18	−2	–	–	1600	600	–	–	–
Palacios et al. 2012 [21]	Lateral FinFET	Silicon		90	2	0.8	565		530		10^8	82	13.8
Jo et al. 2015 [46]	Vertical NW FET	Sapphire	12	100	0.12	0.6	–	156	130	70	10^9	153–163	–
Yu et al. 2016 [47]	Vertical NW FET	Sapphire	7	500	1.3–1.6	1.2	140	3400	314	125	10^8	68	2.2
Yu et al. 2017 [48]	Vertical NW FET	Sapphire	99	360	1.3–1.6	1.5	110	11,000	98	35	10^9	67	–
Hu et al. 2017 [51]	Vertical NW FET	Bulk GaN	120	800	–	1	513	–	–	–	–	–	0.4
Yu et al. 2018 [20]	Vertical NW FET	Sapphire	103	470	0.5	2.5	69	18,000	118	41	10^9	120	5.3
Chaney et al. 2018 [50]	Vertical NW FET	Bulk GaN	–	~60	–	0.4	–	–	–	–	–	109	–
Son et al. 2018 [51]	Vertical NW FET	Sapphire	1	120	0.3	0.4	–	9	23.8	6.6	10^9	110	–
Palacios et al. 2017 [42]	Vertical FinFET	GaN Bulk	–	–	–	1.5	800	–	–	–	10^{11}	75	0.36
Palacios et al. 2018 [43]	Vertical FinFET	GaN Bulk	–	–	–	1.3	1200	–	–	–	–	–	2.1

However, the 210 nm FETs have a SS of 63 mV/dec, which is close to the ideal SS at room temperature (60 mV/dec).

In 2012, Blanchard *et al.* improved their D-mode lateral GaN NW FETs by adding Al_2O_3 as a dielectric layer and creating W gate-all-around (GAA) metal contact directly on the GaN NW as lateral GaN NW MOSFETs with a doping concentration (Si-doped) of $1 \times 10^{18}\,cm^{-3}$, diameter of around 200–400 µm, and length of 10–20 µm, as shown in Figs. 3g,h [38]. The bottom-up GaN NWs were grown and placed to an insulating substrate as discussed above for other lateral NW FETs, but with addition of 43 nm Al_2O_3 and 35 nm W that were coated on GaN NW by atomic layer deposition (ALD). A Ti/Al (20/200 nm) metal stack was then deposited by *E*-beam evaporation as drain and source contacts followed by Ni/Au (200/50 nm) deposition as 2D gate metal contact. The gate-source leakage was below 1 pA, which proves good electrostatic control from GAA structure in this device.

Another lateral GaN NW MESFET was demonstrated by Gačević *et al.* in 2016 with a semi cylindrical top contact Schottky gate having a similar gate-drain-source structure as Blanchard *et al.* (Fig. 3h) [39]. They claimed that this design could improve the electrostatic control in the channel and be used for background study of vertical FET design. In their device, the Si-doped (~$7 \times 10^{18}\,cm^{-3}$) GaN NWs were fabricated using bottom-up approach with the average diameter and length of 90 nm and 1.2 µm, respectively.

After placing the NWs onto a foreign substrate, Ti/Au (20/100 nm) films for drain and source contacts and Ti/Au (15/100 nm) layers for gate metal contact were created and followed by thermal annealing. The higher normalized $g_{m,max}$ in these MESFET structures compared to Blanchard *et al.* FETs in 2008 (see Table 1) was due to smaller NW diameter that decreases the size of gate width. From the most recent research in 2018, Li *et al.* had demonstrated lateral GaN NW FETs with GAA structure and 16 nm Al_2O_3 as a dielectric layer. These devices exhibit SS of 68 mV/dec (Fig. 3i) [40]. The NW was fabricated by bottom-up method with doping concentration (Si-doped) of $1 \times 10^{18}\,cm^{-3}$, wire diameter of ~146 nm and gate length L of ~274 nm. Similar metal contacts as Blanchard *et al.* FETs in 2012 were used in this case. Their $g_{m.max}$ was 10.5 mS/mm, which shows good efficiency for low-power switching [41].

2.2. Vertical 3D GaN FETs

2.2.1. Vertical nanofin FETs

Although lateral GaN NF FETs showed immense performances, the main drawback of lateral geometry is still the consumed device area. Thus, the area of the device affects the breakdown voltage. In addition, numerous material interfaces are exposed to high electric fields, which reduces reliability and prevents avalanche breakdown. For higher-voltage high-current applications, the lateral-device size increases dramatically, and very high current levels are difficult to handle on only one surface. It is expected that vertical devices would reduce the die size and be more reliable as the electric field peaks are far away from the surface. The most studied vertical GaN transistor (i.e., the current aperture vertical electron transistor (CAVET)) has made significant progress in performance, but it still faces two challenges. First, the CAVET structure requires a p-doped current blocking layer buried in the n-doped GaN layer. Fully activating the p-dopant Mg in GaN has been found very challenging and the vertical leakage current tends to be high. Second, the needs for a high quality regrowth of the AlGaN/GaN access region substantially increases the manufacturing cost.

In 2016, the first vertical NF FET was reported by Sun *et al.* from Palacios group at the Massachusetts Institute of Technology (MIT) [42,45]. The authors used a combined dry/wet etching technology, which was critical in the demonstration of vertical channel sidewall. Inductively coupled plasma (ICP) dry etching was first performed using BCl_3/Cl_2 plasma to obtain the initial trapezoidal channel. Then, wet etching in tetramethylammonium hydroxide (TMAH) was applied to obtain the vertical fin sidewalls. The authors state that the morphology

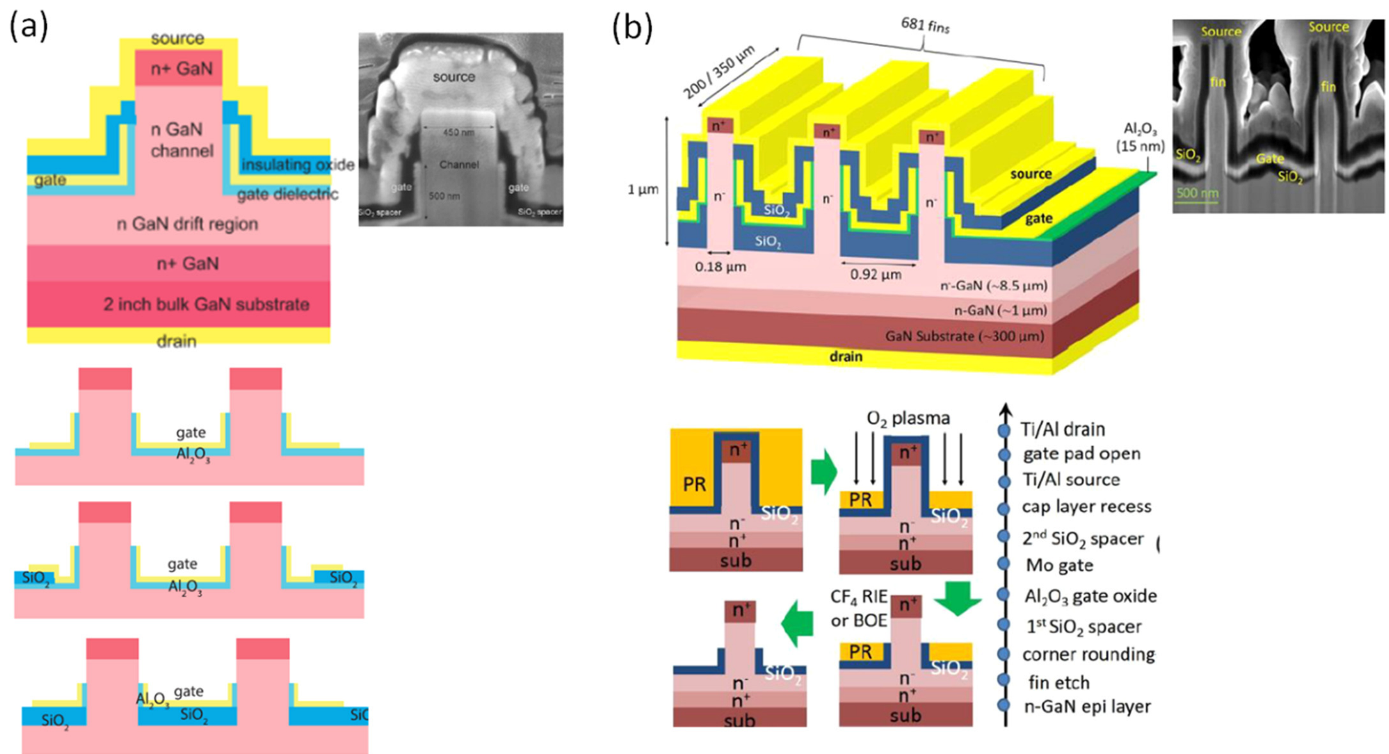

Fig. 4. (a) Schematic, cross-sectional SEM image, and detailed fabrication process flow of vertical 3D GaN NF FETs. © [2017] IEEE. Reprinted, with permission, from [42]. (b) 3D schematic and cross-sectional SEM image of 3D GaN NF FETs with multiple fins ([2018] IEEE. Reprinted, with permission, from [43]), as well as their detailed fabrication process flow. © [2017] IEEE. Reprinted, with permission, from [44].

of the etched sidewall is also related to the channel orientation. The device results in much smoother surface when the channel is aligned along the ⟨1120⟩ direction than that when it is along ⟨1100⟩ direction. This is followed by the deposition of thin Al_2O_3 gate dielectric layer by ALD and sputtering of Molybdenum layer as a gate metal. SiO_2 layer is deposited to serve as the spacer layer to isolate source and drain electrodes. The schematic and cross sectional SEM image of its channel region is shown in Fig. 4a. The device exhibited normally-off operation with a low on-resistance.

Still from the same group, to improve the on and off-state characteristics, they modified the epitaxial structure and fabricated the vertical NF FET structure (Fig. 4b) [43]. Zhang *et al.* employed new techniques such as corner rounding, after the fin etching. Also, edge termination was formed for the first time in vertical NF FETs, which showed the improved breakdown and on-resistance performances compared to those of ref. [42].

2.2.2. Vertical nanowire FETs

The first 3D vertical GaN NW FETs were demonstrated by Jo *et al.* in 2015 [46]. A device consisting of 12 GaN NWs was fabricated using a top-down approach based on hybrid etching involving transmission coupled plasma-reactive ion etching (TCP-RIE) and TMAH wet etching for GaN on sapphire substrate with SiO_2 as etch mask. The epi-GaN is composed of 70 nm and 500 nm Si-doped GaN (doping concentration, $N_D = 1 \times 10^{19}\,cm^{-3}$) at upper and bottom layers, respectively, and 120 nm undoped GaN in between. The NWs with a diameter of 100 nm and a height of ~300 nm were passivated with Al_2O_3 and subsequently coated with TiN as a GAA gate metal in ALD process. This process was followed by deposition of Ti/Al/Ni/Au layers as source and drain metal contacts, as shown in Fig. 5a. This *E*-mode vertical 3D GaN NW FET exhibits V_{th} of 0.6 V with I_{on}/I_{off} of 10^9 and no obvious hysteresis.

With similar model and substrate, in following year, Yu *et al.* from Braunschweig University of Technology, Germany reported on E-mode vertical GaN NW FETs in *n-i-n* epi-GaN wafer on sapphire substrate [47]. The hybrid etching step combining an induced coupled plasma-dry reactive ion etching (ICP-DRIE) with H_2/SF_6 gases and KOH-based wet etching was employed. They develop a device consisting of 7 NWs with diameter of 500 nm and height of 2.7 μm. The gate passivation layer was made of SiO_2 by plasma enhanced atomic layer deposition (PEALD). Additionally, the SiO_x film was deposited by e-beam evaporation method to enhance passivation between gate pad and bottom layer of the FETs. Thanks to the mushroom shape of the NWs obtained during wet etching, the SiO_x only covers the bottom space of NWs, as shown in Fig. 5b. A 300 nm Cr metal GAA structure was used in this FET. The gate length (L) was 1.3–1.5 μm, in which the gated NW structures were filled with photoresist cured at 250 °C to mechanically support the drain metal contact electrode of Ti/Cr/Au deposited by e-beam evaporation. Furthermore, a BV of 140 V was achieved in this FET, as depicted in Fig. 5c. Compared to FETs from Jo *et al.*, the gate hysteresis in this FET is still visible, in which they mentioned that it might be caused by gate oxide charge trapping in SiO_2. However, their normalized $I_{d,max}$ are 2 times larger than those in FETs of Jo *et al.* (see Table 1), which is attributed to the larger NW diameter [31,46].

In 2017, Yu *et al.* demonstrated the upscaling capability of this concept by integrating more NWs in a single vertical FET (i.e., 99 NWs) with similar epi-GaN wafer structure as used in previous work. In this case, the differences are made in terms of NW diameter, I_{on}/I_{off}, and V_{th} compared to previous one [48]. The hybrid wet/dry etching was still used in the device fabrication with Cr GAA metal applied on this FET. The NW diameter of 360 nm and height of ~2.6 μm were consequently reached with similar method in [47]. It exhibits V_{th} of 1.5 V and I_{on}/I_{off} of 10^9 or 1 order of magnitudes higher than previous one, as shown in Table 1. The *SS* is around 67 mV/dec, which is close to ideal showing good electrostatic control of GAA structure.

Another vertical GaN NW FET was reported by Hu *et al.* in 2017. They claim that the vertical direction in their GaN NW metal-insulator semiconductor FET (MISFET) could improve the reliability, scaling, and thermal management of the devices [49]. In their work, they used GaN

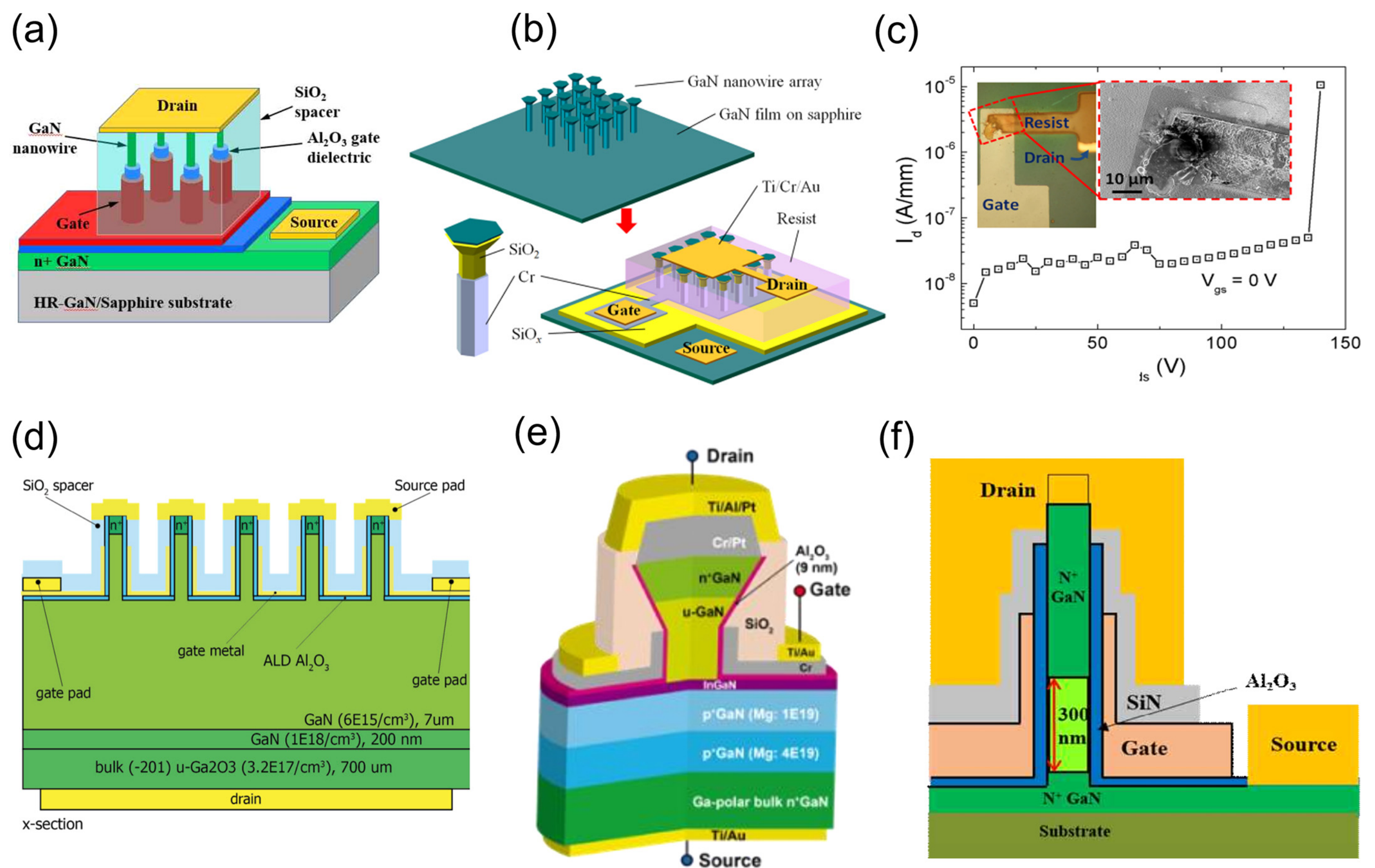

Fig. 5. (a) 3D schematic of vertical 3D GaN NW FETs with drain at top and source at bottom using SiO_2 as filling material and contact drain support from Jo *et al.* © [2015] IEEE. Reprinted, with permission, from [46]. (b) 3D schematics of vertical 3D GaN NW FETs, where drain and source are formed in vertical direction from NW array (top), and (c) BV characteristic at V_{gs} = 0 V from Yu *et al.* Reprinted from [47], with the permission of AIP Publishing. (d) Schematic of GaN NW FET from Hu *et al.* with bulk GaN as the substrate and drain at bottom and source formed on top of the NW. © [2017] IEEE. Reprinted, with permission, from [49]. (e) A vertical GaN NW TFET schematic with drain position on top of the NW using bulk GaN as substrate from Chaney *et al.* © [2018] IEEE. Reprinted, with permission, from [50]. (f) A 2D schematic of vertical GaN NW TFETs with gate-all-around (GAA) and drain position on top of the NW from Son *et al.*, where sapphire is used as the substrate. Reprinted from [51]. Copyright 2018, with permission from Elsevier.

NWs on 700 µm bulk GaN ($N_D = 3.2 \times 10^{17}$ cm^{-3}), 200 nm *n*-doped GaN layer ($N_D = 1 \times 10^{18}$ cm^{-3}), and 7 µm low-doped GaN layer as drift region ($N_D = \sim 6 \times 10^{15}$ cm^{-3}). They used Al_2O_3 as a gate dielectric material with the drain and source are located in opposite positions as the ones fabricated by Yu *et al.*, as depicted in Fig. 5d. The drain is connected to the bulk GaN at the bottom surface, while the source is set on the top surface of NW. The TMAH-based wet etching solution was used and dry etching was employed beforehand to produce NWs with smooth sidewall surfaces and wire diameter of ~800 nm. The BV of 513 V has been reported from this device (gate to source voltage, $V_{gs} = -15$ V).

In 2018, Yu *et al.* reported a 103 NW *n-p-n* vertical GaN NW FET [52] with a similar fabrication method shown in [47,48] (Fig. 5b). They claimed that it was the first time an inverted p-GaN channel was used in vertical MOSFETs with GAA structures [5]. Due to the p-channel, the threshold voltages could be increased to 2.5 V, which is beneficial for safe power switching. The employed epi-GaN wafer (from top to bottom) consists of 0.5 µm highly n-doped GaN (Si doped) 10^{19} cm^{-3}, 1.6 µm n-doped GaN of 3×10^{18} cm^{-3}, 0.5 µm p-doped GaN (Mg doped), 1.0 n-doped GaN of 3×10^{18} cm^{-3}, and 2.5 µm n-doped GaN of 2×10^{18} cm^{-3} on sapphire substrate. The GAA covered a p-channel as a gate channel with length $L = 0.5$ µm, where the NW diameter and length are around 470 nm and 2.8 µm, respectively. R_{on} of 5.3 Ωm cm^{-2} was measured with small barrier voltages at around 1 V on output characteristic, in which they mentioned that it might be caused by imperfect Ohmic contact. Regardless of all superior DC characteristics, the device has shown a pronounced gate hysteresis. The authors attribute this instability to mobile ions in the SiO_2 gate dielectric layer which might be incorporated during KOH-based wet chemical etching. Therefore, a denser dielectric material (e.g., Al_2O_3 or Si_3N_4) could be a solution towards this issue. Compared to work from Jo *et al.* [46], the Al_2O_3 layer has proven its stability in the dual sweep mode that results in smaller hysteresis. Thus, it is suggested for any kind of 3D GaN FET devices that Al_2O_3 could be adapted as one of the promising gate dielectric materials. Even though there was a *p*-channel in this NW FET, the BV was still about 69 V, which could be due to either the short drift region space or about 1.6 µm space between highly doped area and the edge of *p*-channel. Overall, the performance optimization was needed for these FETs, especially to reduce the gate hysteresis by using denser dielectric material as passivation layer (e.g., Al_2O_3).

Another type of GaN NW FETs was developed by Chaney *et al.* in 2018, in which they demonstrated for the first time GaN NW based tunnel FETs (TFETs) [50]. In these TFETs, the SS could achieve very low value surpassing the SS limit in MOSFETs or below 60 mV/dec [53]. They made the transistors on a bulk GaN substrate grown by plasma-assisted molecular beam epitaxy (MBE) and fabricated the NWs by hybrid etching, where KOH-based solution was used in the wet chemical etching treatment. The epi-GaN structure from bottom to top consists of bulk *n*-GaN, *p*-doped GaN (Mg: 4×10^{19} cm^{-3} and 1×10^{19} cm^{-3}), a 5 nm InGaN, an undoped GaN, and *n*-GaN. The NW diameter was 60 nm with a GAA structure as shown in Fig. 5e. The Cr/Pt/Ti/Al/Pt layers were used as the metal contact, while Al_2O_3 film was

employed as dielectric material. For the filling material, SiO_2 was chosen. Although the ideal SS value in these TFETs was not able to be achieved (Table 1), the *E*-mode operation could still be demonstrated with the V_{th} of ~0.4 V.

In the same year, another vertical GaN NW FET was reported by Son *et al.* who fabricated E-mode GaN NW FETs on a sapphire substrate by hybrid etching using TMAH as wet chemical etching solution [51]. The etched NWs have a height of 1 μm and a diameter of ~120 nm from the epi-GaN wafer grown by MOCVD with the doping profile (from top to bottom) of *n*-doped GaN of 2.0×10^{18} cm^{-3} (800 nm), *n*-doped GaN of 2.0×10^{16} cm^{-3} (300 nm), and *n*-doped GaN of 2.0×10^{18} cm^{-3} (800 nm). Fig. 5f shows the 2D schematic of the fabricated vertical GaN NW FETs with GAA structure utilizing Al_2O_3 as the dielectric material for gate passivation and SiN as the filling material between gate and drain on top. For the drain, gate, and source contacts, they employed Au/Ni/Al/Ti/Si metal layers with 800 °C rapid thermal annealing in N_2 ambient condition to form ohmic contacts. The low $g_{m,max}$ of 6.6 mS/mm in this FET is attributed to the small diameter size of the NW, which results in small gate width and very high electric field in the drift region leading the drain current to reach saturation condition earlier [17,35].

3. Device fabrication methods

3.1. Bottom-up approach for 3D GaN FETs

The bottom-up growth of GaN nanostructures has been investigated extensively since the late 1990s by many groups, mainly due to their potential application in solid state lighting, which was assumed to greatly benefit from the large active area [29]. The 3D epitaxy allows the fabrication of high aspect ratio structures with improved material quality making it a promising tool for transistor devices as well. In this case, two different approaches are possible. Either the grown 3D structures are transferred onto an insulating substrate to build lateral FETs or they are processed directly on the growth substrate.

For the indirect approach, GaN nanowires are typically grown self-organized by molecular beam epitaxy (MBE) on Si (111) substrates (Fig. 6a). The growth mechanism of self-organized GaN NWs has been studied extensively and is shortly summarized here. A more detailed summary is given e.g., in [29,54]. First, the impinging Ga atoms are nucleating at randomly distributed nuclei on the substrate [55]. The nucleation can be delayed by an incubation time [56]. A shape transition of the GaN nuclei into hexagonal forms with flat c-plane tips initiates the NW elongation [55]. The NW growth is assumed to be driven by diffusion of Ga adatoms towards the NW tip [57–59]. Many groups pointed out that the III/V ratio plays an important role for the self-organized NW growth [60,61]. Nitrogen rich growth conditions reduce the diffusion length of Ga and thus support 3D growth [57]. GaN NWs grown by self-organized MBE on Si (111) substrates can achieve very thin diameters down to 10 nm [59]. Due to their small footprint, the GaN NWs can relax strain induced by lattice mismatch and eliminate threading dislocations [16]. MBE grown N-polar NWs show intensive photoluminescence with sharp excitonic peaks, indicating an excellent material quality [60].

The self-organized nucleation leads to a dense and inhomogeneous distribution of NWs with varying diameter, height and angle, which hinders their integration into a FET device directly on the growth substrate. Instead, the nanowires are transferred onto an insulating substrate, typically Si coated with SiO_2, to fabricate a lateral NW FET device. Ultrasonic agitation can be used to harvest the NWs from the growth substrate and disperse them onto the foreign substrate either randomly followed by electron beam lithography (EBL) for contacting [40] or position controlled via dielectrophoresis [36]. In the latter case, a 75 kHz sine wave was generated between previously defined contact pads during the dispensation of a NW/isopropanol droplet.

Although this indirect approach is well suited to investigate the electrical transport of single GaN NWs, it is limited to low power applications. For the switching of macroscopic currents, parallel integration of many NWs is required which is hardly possible with transfer techniques. Furthermore, self-organized grown NWs typically show large deviations in shape and size, which leads to varying electrical properties of the individual NWs. Therefore, a position-controlled growth of nanostructures with homogeneous properties is favorable for most applications.

The selective area growth (SAG) of GaN nanostructures was first demonstrated by Kishino *et al.* [65] and applied by many groups both using MBE [54,66–69] or MOVPE [16,70,71]. The selectivity is achieved by patterning the growth substrate (GaN or AlN) lithographically with a mask of chemically inert materials (e.g., TiN, SiO_2 or Si_3N_4), which strongly suppresses parasitic nucleation. Nucleation only occurs inside the mask openings, whereas on the mask, adsorbed Ga atoms either desorb or diffuse towards the openings. If the openings are small enough, all nuclei within coalesce before the elongation starts, so that a single nanostructure is formed. A regular distribution of mask openings enables the growth of uniform nanostructure arrays (Fig. 6b).

For NW SAG by MOVPE, silane was found to be able to enhance the vertical growth rate drastically [72], which is assumed to be caused by the formation of a thin SiN passivation layer at the sidewalls supporting diffusion towards the NW tips [73]. With high silane flows, very high vertical growth rates up to 145 μm/h could be obtained [62]. Via bottom-up growth, especially using MOVPE, core-shell geometries with different material compositions or doping are accessible and widely used for NW LEDs. Such geometries could be utilized for transistor devices as well for further engineering the channel properties along the sidewalls. For instance, Li *et al.* implemented MOVPE grown NWs with radial GaN/AlN/AlGaN heterostructures as high electron mobility transistors (HEMTs) [33]. A similar method was demonstrated by Song

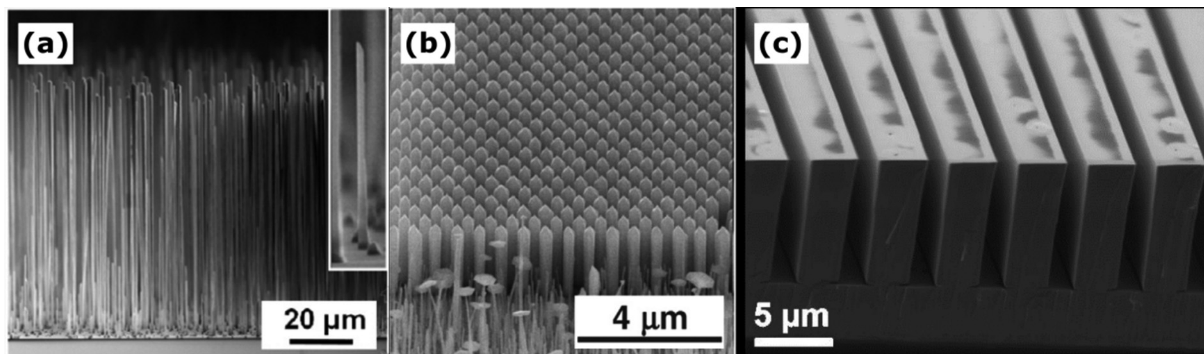

Fig. 6. SEM image of bottom-up grown GaN nanostructures. (a) Self-organized GaN NW on Si(111) by MBE [62]. © IOP Publishing. Reproduced with permission. All rights reserved. (b) A regular array of GaN NWs grown by MBE SAG [63]. Copyright (2008) The Japan Society of Applied Physics. (c) An array of GaN fin microstructures grown by MOVPE SAG. Reprinted from [64]. Copyright 2017, with permission from Elsevier.

et al. who grew lateral GaN microwires on Si grooves with GaN/AlN/AlGaN core-shell structures on the polar and semipolar sidewall facets and fabricated HEMT devices after releasing the wires from the growth substrate [74]. It should be noted that both devices utilized GaN NWs aligned along the nonpolar ⟨11 − 20⟩ a-direction possessing polar and semipolar sidewall facets where a 2DEG can be formed solely by polarization fields. HEMTs based on NWs grown along the usually obtained c-direction would require modulation doping to obtain a 2DEG channel.

The SAG is not limited to wires, but can be applied for various different shapes. The most promising alternative geometry for electronics are GaN fin structures, which are expected to obtain better stability and homogeneity compared to NWs. The SAG of GaN fins with a height up to 50 μm and smooth a-plane sidewalls has been demonstrated by Hartmann *et al.* (Fig. 6c) [64,75]. Although the fin cores contain many extended defects, the sidewalls exhibit low dislocation densities and could be used as channels for 3D electronic devices.

Although the direct approach is favorable for most applications, to the best of our knowledge, there is no report so far on FET devices based on directly processed bottom-up nanostructures. Instead, a top-down approach is applied, which offers a more precise control over the structure dimensions and enables the integration of vertical doping profiles. Nevertheless, the bottom-up approach should not be neglected because it can provide much higher structures with reduced defect densities compared to etched structures and enables the utilization of core-shell geometries, which could extend the design flexibility of future 3D electronic devices by an additional dimension.

3.2. Top-down approach for 3D GaN FETs

3.2.1. Hybrid etching for 3D GaN

Top-down approaches, generally by virtue of etching techniques, were introduced as a low-cost but highly efficient way towards 3D GaN structures, which were mainly employed by early researchers for optoelectronic devices as well. The etching processes were directly performed on GaN epitaxial or bulk wafers.

Similar to Si, plasma etching tools (e.g., inductively coupled plasma dry reactive ion etcher) can be directly utilized to create GaN nanostructures, using hard etching masks (e.g., oxides or metal) [76–80]. In particular, it is noteworthy that the masks can be well addressed and defined by photolithography, which greatly benefits realistic implementations [76,80]. In 2012, Paramanik *et al.* reported the fabrication of large-area GaN nano-columns on Si (111) substrate with a sidewall oblique angle of 86° by using chlorine-based ICP chemistries (Fig. 7a) [76]. The authors further pointed out the geometry and morphology of dry etched nano-columns can be adjusted by etching parameters and employed gas chemistries [76,81]. Besides toxic Cl_2-based chemistries, SF_6/H_2 were also considered and reported for dry etching of GaN nanostructures [80]. However, to be different from the plasma etching of Si NWs with smooth sidewalls [82,83], GaN nanostructures after dry etching process usually lead to damaged structure surfaces due to the ion bombardment effect, which is not suitable to be directly applied in surface sensitive devices (e.g., FETs and LEDs) [84].

As an alternative, anisotropic etching in proper wet chemical etchant can result in nanostructures with smooth surfaces. Liu *et al.* reported the preparation of vertical GaN NW arrays on sapphire substrate with well-aligned *c*-axis orientation by using a conventional electrode free photoelectrochemical (PEC) method in 2011 [85]. In their work, the etchant was a mixed base solution with 1 M KOH and 0.1 M $K_2S_2O_8$. Moreover, a 150 W Xe lamp was employed as the UV light source, which can generate free holes at the material surface and promote the oxidation process. This etching process was proven to be a dislocation-hunted process, which ensures a high material quality and, however, at the same time limits the precise control in terms of NW number, location, and dimension (Fig. 7b) [85].

A two-step hybrid etching approach, including dry and wet etching in sequence, was therefore proposed by researchers to combine the advantages in structure homogeneity and material quality [47,48,77,80,81,86]. In 2012, Li *et al.* reported the fabrication of non-tapered GaN NWs by employing hybrid etching for single-mode lasing, as shown in Fig. 7c [87]. The authors had achieved a single-mode lasing with a line-width of ∼0.12 nm and a side-mode suppression ratio of > 18 dB, proving the hybrid-etched GaN NWs can have a precise control in dimension as well as a high material quality for enhancing gain [87]. Hybrid-etched GaN nanostructures were later successfully applied in the electronic applications [42,46–48,52,86]. Jo *et al.* demonstrated a vertical GaN NW FET using SiO_2 as etch mask and 5% TMAH as etching solution in 2015 [46]. Later, Yu *et al.* reported another vertical GaN FET based on hybrid-etched NWs using Cr and AZ400K developer (KOH-based solution) as etching mask and etchant, respectively. The authors achieved regular NW arrays with smooth hexagonal sidewalls, which were verified to be *a*-plane oriented [47,48]. In 2017, Sun *et al.* demonstrated a vertical GaN NF FET with bulk substrate and TMAH treatment. The fins with sidewall in both *a*- and *m*-plane orientations had been investigated in their work and the latter case presented smoother surface morphology [42. In 2016, Im *et al.* performed the hybrid etching of lateral GaN NWs on GaN-on-insulator wafers by wet etching on ICP-patterned strips. TMAH solution with concentration of 5% was employed in their case and triangle-shaped NWs were achieved [86,88].

3.2.2. Wet chemical etching: Mechanism and engineering

Since wet etching plays a crucial role in improving the morphology and surface quality of hybrid-etched GaN NWs, it is practically important to understand its mechanism. Thanks to the previous research on anisotropic etching in other semiconductor materials (e.g., Si), the etching mechanism can be well understood and developed by some well-founded theories. In general, the wet etching process on GaN in

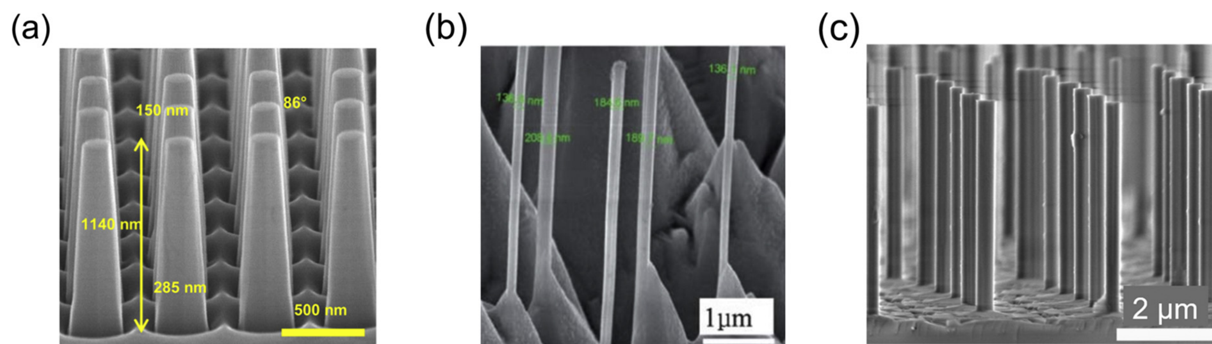

Fig. 7. SEM images of GaN NWs prepared by different etching treatments: (a) Dry etching. Reprinted with permission from [76]. Copyright 2012, American Vacuum Society. (b) Wet etching. Reproduced from [85] with permission from The Royal Society of Chemistry. (c) Hybrid etching approaches. Reprinted with permission from [87], The Optical Society.

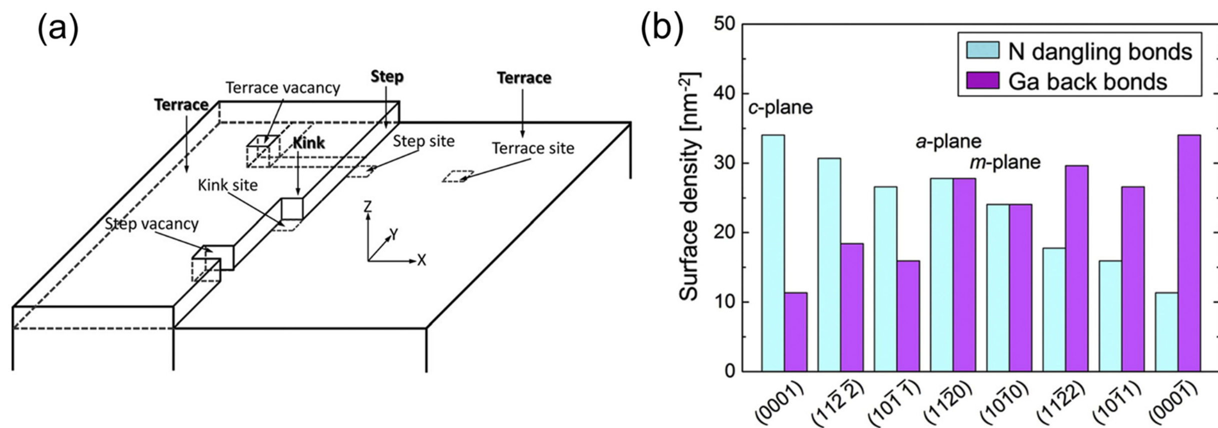

Fig. 8. (a) Schematic of kink, step, and terrace sites on crystal for growth and etching process. Reproduced from [91] with permission from The Royal Society of Chemistry. (b) Histogram of surface N dangling bonds and Ga back bonds on several common crystal facets [48]. © IOP Publishing. Reproduced with permission. All rights reserved.

non-reducing base solutions can be described by Eq. (1).

$$GaN + H_2O \overset{OH^-}{\rightarrow} Ga_2O_3 + NH_3 \quad (1)$$

where OH^- is the catalytic of forming gallium oxide and dissolves it afterwards [89]. UV illumination is usually applied for promoting the etching process especially in *n*-GaN. By generation of electron-hole pairs at the material surface, holes are driven to surface due to the upward band bending and reduce the potential for oxidation.

In general, because of the symmetry of Wurtzite crystal, GaN NWs with smooth sidewalls usually have either a hexagonal or triangle shape [47,86]. Similar to the anisotropic etching of Si, the etching behavior on crystals can follow a step-flow model, which can be regarded as an inverse process of bottom-up growth [90–93]. As shown in Fig. 8a, the etching rate on kink and step sides shall be higher than on the terrace site [91,93]. Meanwhile, the etching stability of flat crystallographic facts could be influenced by the surface bonding configuration. Li *et al.* studied the etching of +*c*- and –*c*-plane GaN in KOH solutions and found out the etching rate is highly suppressed on *c*-plane surface due to the electrostatic repulsion from N dangling bonds [94]. Based on that, Yu *et al.* also investigated the surface densities of both N dangling bonds and Ga back bonds on several common facets (Fig. 8b) and successfully explained the formation of featured mushroom-like geometry in their hybrid etching of GaN NWs. The authors also figured out a concentration dependent orientation of NW sidewalls, which were changed from *a*-plane to *m*-plane oriented when the concentration of KOH aqueous solution increased from 0.5 M to 1 M, indicating that the etching rates of different nonpolar planes can be quite sensitive to experimental conditions [12]. Almost simultaneously, Leung *et al.* carefully studied the orientation dependent etching rate on GaN through delicately designed experiments and the ratio of etching rates between *m*- and *a*-plane was calculated to be 0.3–0.9 in several different base solutions [93].

The etching rate on semiconductor surface can be influenced by doping in terms of adjusting surface potential as well as band bending. In general, wet etching on *p*-GaN surface shows a lower rate than on *n*-GaN [89,95]. Most previously reported works on top-down GaN nanoFETs were with only *n*-type material. A recent progress is done by Yu *et al.* in 2018 that they have successfully employing hybrid etching on *c*-axis NW FETs with an *n-p-n* doping profile, which present the same morphology of pure *n*-type NWs (Fig. 9a) [48,52].

By comparing with the morphology of vertical nanowires after hybrid etching on *p-n* layers (Fig. 9b), the authors investigated the mechanism of etching on nonpolar sidewalls by employing a step-flow model, which reveals the etching rate depends on forming atomic cavities with steps on crystal surfaces and further proposes that the step propagation rate along –*c*-axis should be much faster than along *c*-axis, as illustrated in Fig. 9c. Although fewer cavities are expected to be formed on the terrace of *p*-GaN, NWs with *n-p* profile can maintain a non-tapered sidewall because of the fast propagation of steps from top *n*-region, which is, however, not possible in the case with a *p-n* profile (see the inserts of Figs. 9a,b). The significance of this work is to reveal a practical approach towards GaN NWs with both vertical architecture and flexible doping profile, which is promising for implementations in future 3D electronics.

3.2.3. Top-down fabrication of vertical GaN nanoFETs

To be different from the conventional processing procedures on lateral transistors, GaN nanoFETs with vertical device architecture have featured processing concepts, which will bring advantages as well as challenges. In general, as depicted in Fig. 10, a vertical nano-FET mainly contains three parts (i.e., dielectric and multi-gate structure, top and bottom electrodes, and insulating spacing between electrodes). Again, because of the overlap of electrode in the vertical direction, more considerations should be brought into this vertical processing to ensure that every sequential processing step will not influence the reliability of former steps. Briefly, a proper idea of processing on vertical NWs or NFs can be described as following (Fig. 10): After preparation of the top-down NW arrays with the hybrid etching approach, an insulting layer made of nitrides or oxides, should be deposited on the bottom GaN surface for further gate deposition. In most cases, MOSFET structures were employed and thus oxides will be conformably deposited on the 3D sample surface to serve as both dielectric and passivation layers. Then, gate material will be properly placed on 3D channels. Afterwards, before the top electrode deposition, another insulating spacing layer should be placed on top of the gate to separate it from the following top electrode deposition. The deposition of bottom electrode shall depend on the wafer type. For a case of using conductive bulk GaN substrate, metal contact can be placed at the bottom of bulk substrate to form an ideal vertical current path, which can be done at the beginning or end of the whole process. As for devices on insulating foreign substrate (e.g., sapphire or AlN/Si), the bottom electrode has to be located on the upper surface of bottom substrate, which is usually done together with top electrode [42,46,47,49–51].

3.2.3.1. Multi-gate architecture and dielectric. The formation of multi-gate structure (e.g., wrap around gate on NWs and double gate on NFs) is an inherent big advantage of vertical nano-FETs, which is beneficial for gate control and output enhancement. In order to realize a conformable coating of dielectric and gate layers on vertical channels, atomic layer deposition (ALD) tools or advanced deposition treatment are required. Both SiO_2 and Al_2O_3 by ALD have been usually employed as the dielectric material. A good interface between hybrid-etched GaN

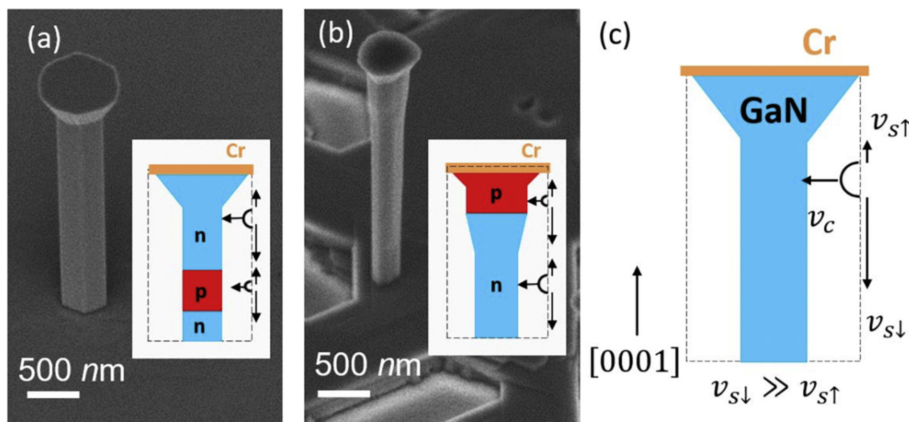

Fig. 9. 45° tilted SEM images of hybrid-etched GaN NWs with (a) *n-p* and (b) *p-n* junction structures. Inserts are schematics of the mechanism of forming featured morphologies during wet etching. Here "N" and "P" stand for the n- and p-type doping regions, while the dashed line is the boundary of the cylindrical-like NWs at the early stage of wet etching. (c) Schematic of the NW wet etching process by a step flow model. v_c is the velocity of forming atomic cavities on sidewalls, while $v_{(s\uparrow)}$ and $v_{(s\downarrow)}$ represent the step propagation rate along *c* and -*c*directions, respectively. © [2018] IEEE. Reprinted, with permission, from [52].

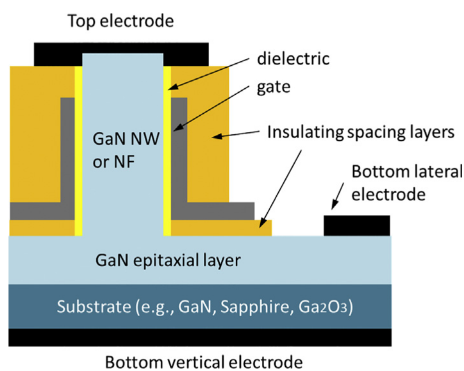

Fig. 10. Device structure schematic of vertical GaN nano-FETs.

NW and PE-ALD deposited SiO_2 with a small interface trap density of $D_{it} < 1.3 \times 10^{11} cm^{-2} eV^{-1}$ had been reported by Yu *et al.* in their early work. However, the authors further pointed out that the SiO_2 dielectric layer could not have high immunity to unintentionally incorporated mobile ions, which can result in serious gate hysteresis [47,52]. In contrast, using Al_2O_3 as dielectric layer can overcome this problem since it has a denser structure and a higher permittivity, although further optimization in oxide trap charging minimization might be still required [96].

Another critical issue is the defining of gate length in 3D nano-FETs, which is kind of a byproduct of the convenience in forming multi-gate structures since conventional lift-off process is no longer available in vertical processing. High work-function metals (e.g., Cr [47], Mo [42], TiN [46]) were usually employed by researchers to realize E-mode device operation. Jo *et al.* first described an "etch back" process to determine the gate length in their vertical GaN NW FETs, and similar processes were also implemented by other research groups [42,46,49,52]. In brief, after metal gate deposition on NWs or NFs, the nanostructures were usually buried with photoresist and then the top part would be exposed by plasma etching. After that, wet etching would be employed to remove the unrequired metal part. A remarkable alternative technique is proposed by Yu *et al.* In their work, by employing their proper hybrid-etching technique, a mushroom-like NW geometry could be realized. Thanks to the shadow effect from the NW top part, the length of gate metal on NW sidewalls can be controlled by adjusting the wafer tilt angle during e-beam evaporation, which greatly reduces the processing complexity and could be an efficient and reliable way towards short gate devices [47].

3.2.3.2. Top and bottom electrodes. These two electrodes function as source and drain contacts in nanoFETs. Both source and drain contacts could be arranged on the top or bottom, depending on the detailed wafer type and device application. As presented in Fig. 10, for bulk GaN or conductive substrates, drain can be located at the back side of bottom substrate with perfect vertical current path and sufficiently thick drift layer, which is promising for high voltage switching applications. In particular, the height of NWs or NFs can be short for resistance mitigation and fast transition of electrons in channel [42,49]. On the other hand, when GaN layers were grown on foreign insulating substrates, the source contact would be formed on the top surface of bottom substrate with a lateral current path, while the top electrode becomes the drain contact. Thus, the height of NWs or NFs would be expected to be sufficiently large to achieve the desired performance in power application [46,47,52]. Normally, the Ohmic contact could be easier to be formed at the bottom electrode, which has a much larger contact area than the top electrode. Thus, efforts mainly focus on the formation of Ohmic contact at the top electrode. Most reported works employed a high doping concentration at the top of GaN nanostructures, which can be easily realized through current epitaxy techniques. In particular, as deposited metal Ohmic contact could be preferable since conventional thermal annealing for planar FETs might influence previous processing steps. For instance, Yu *et al.* employed Ti/Cr/Au and Ti/Au metal stack for GaN NW FETs [11,15], and Zhang *et al.* use the Ti/Al stack for their NF power FETs [44]. It is noteworthy that also a plasma-assisted surface roughening was employed by Zhang et al., which effectively enhance the Ohmic behavior [44].

3.2.3.3. Insulating spacing between electrodes. Normally, the insulating spacing between gate and bottom electrodes can be realized by conformable deposition of dielectric layer on sample surface [42,44,46,51]. Though it is convenient, the thickness of insulating layer on bottom surface could be limited by the dielectric, of which the thickness should not be large for efficient gate control. Therefore, Yu *et al.* suggested their mushroom-like NW FETs, which can maintain a flexible thickness combination of gate dielectric and gate-to-bottom spacing, by virtue of a thick SiO_x evaporation after PEALD of SiO_2 dielectrics [47]. In terms of the spacing between gate and top electrodes, spacing material should be adapted to the detailed device architecture and design. For top source devices or top drain ones with a submicron structure height, physical or chemical vapor deposition of oxides (e.g., SiO_2 and Al_2O_3) on NWs or NFs will be a good choice [42,46,50,51]. In contrast, for top drain FETs with height in scale of μm, a thick spacing should be ensured especially for high power applications. Yu *et al.* employed cured photoresist as a filling material in their top drain NW FETs, which are still facing the challenges in terms of electrical reliability and thermal stability [47,52]. Alternative spacing materials (e.g., Benzocyclobutene) had been proposed in nanoFETs based on other semiconductor nanostructures [97]. Although the power performance of top-drain nanoFETs cannot compete with the top-source ones based on bulk GaN substrates, they still have the advantages for mid-power applications with low cost and high-temperature operation.

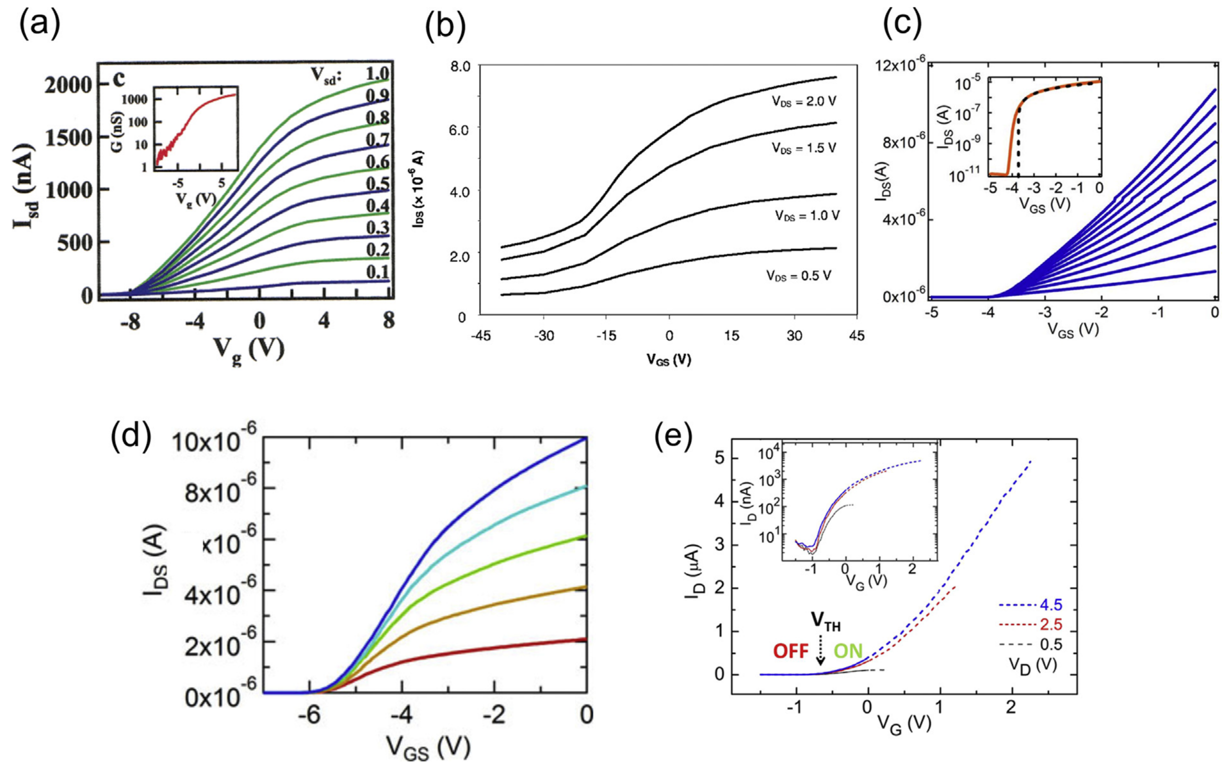

Fig. 11. Transfer characteristics of lateral GaN NW FETs from (a) Huang *et al.* (Reprinted with permission from [27]. Copyright (2006) American Chemical Society), (b) Motayed *et al.* (Reprinted from [30], with the permission of AIP Publishing), (c) Blanchard *et al.* (© [2008] IEEE. Reprinted, with permission, from [36]), (d) Blanchard *et al.* (© [2012] IEEE. Reprinted, with permission, from [38]), and (e) Gačević *et al.* Reprinted from [39], with the permission of AIP Publishing.

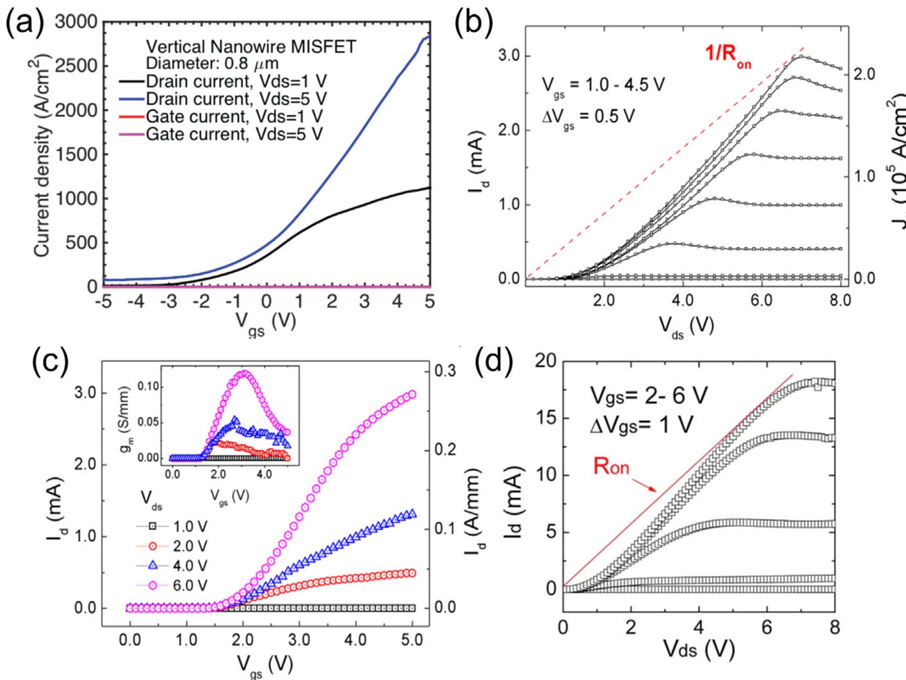

Fig. 12. (a) Transfer characteristics of vertical *n-i-n* GaN NW FETs on bulk GaN from Hu *et al.* with lowest R_{on}. © [2017] IEEE. Reprinted, with permission, from [49]. (b) Output and (c) transfer characteristics of vertical *n-i-n* GaN NW FETs on sapphire from Yu *et al.*Reprinted from [47], with the permission of AIP Publishing. (d) Output characteristics of vertical *n-p-n* GaN NW FETs on sapphire with the highest R_{on}. © [2018] IEEE. Reprinted, with permission, from [52].

4. Device performances

As there are several 3D GaN nanoFETs developed in the recent years, Table 1 has listed all devices based on GaN NW and NF structures created in lateral and vertical architectures, including their performance characteristics. More explanations in terms of on- and off-state performances, effect of diameter and number of the nanowire, effect of gate length of the nanowire, and low frequency noise characteristics will also be described in the following sections.

4.1. On- and off-state performances

The D-mode (normally on) FETs have several advantages in terms of their device performances, but usually could not sustain for higher power application. This occurs due to high electric field in the depletion channel, even at negative bias voltage ($V_{th} < 0$ V) compared to *E*-mode

transistor, which needs higher bias voltage to create the channel. For logic application, the D-mode device can be combined with E-mode to create integrated monolithic GaN CMOS.

All lateral NW FETs mentioned in this review (see Table 1) function as D-mode devices with the lowest V_{th} of -30 V obtained by Motayed *et al.* [30] and the highest V_{th} of -0.5 V achieved by Li *et al.* as shown in Fig. 11 [33]. Depending on device parameters (e.g., NW diameter, gate length, and doping concentration N_D), the D-mode GaN NW FETs could reach different V_{th} and $I_{d,max}$. Moreover, the hysteresis could be reduced by engineering the positions of drain and source contacts (e.g., either vertical or planar positions) [42]. All D-mode 3D transistors have no GAA structure except the ones from Blanchard *et al.* that used W gate metal as GAA structure resulting in V_{th} of -5.5 V. Their diameters are also smaller than those of vertical NW FETs fabricated by hybrid etching method. The vertical GaN NW FETs listed in Table 1 are operated in *E*-mode (normally off) with the V_{th} ranges from 0.4 to 2.5 V, while the R_{on} varies between 0.4 and 5.3 mΩcm^2. The R_{on} from the vertical GaN NW FETs was influenced by the active area or the space between the NW, which also depends on the NW or NF pitch. The higher the active area, the higher the R_{on}, which consequently can reduce the FET efficiency. The lowest R_{on} of 0.4 mΩcm^2 was demonstrated by Hu *et al.* in their 120 GaN NW FETs with bulk GaN as a substrate.

Meanwhile, Yu *et al.* had obtained R_{on} values of 2.2 mΩcm^2 and 5.3 mΩcm^2 for 7 and 103 GaN NW FETs on sapphire substrate, respectively [18,20], as shown in Fig. 12. Furthermore, for single GaN NW FET that does not really consider the active area, the R_{on} mainly also depends on the channel and contact resistance, which could be explained as terms of surface state on NW or NF sidewall and metal contact profile (i.e., either Schottky or Ohmic behavior), respectively [31]. The surface state could make additional depletion in the drift region and increase the resistance by making more depletion layer in wire. The non-ideal Schottky behavior on the drain contact could also increase the R_{on} since it can make higher turn-on voltage in output characteristics thus lowering the efficiency. Besides the surface state and Schottky contact, the N_D and the thickness of drift region (L_D) of the GaN NW or NF FETs have a significant impact to the R_{on}, as follows [102]:

$$R_{on} = \frac{L_D}{\mu.\ q.\ N_D} \tag{2}$$

where q is the electron charge and μ is the electron mobility.

Apart from that, the BV in E-mode FETs was influenced also by the drift region thickness and N_D. In vertical GaN NW FETs on sapphire substrate, BV values of up to 140 V were reported [47]. Those devices showed a gate dielectric breakdown, which was assumed to occur at the drain side of the gate, where simulations indicate the peak of the electric field. The authors attribute the low BV to the small drift length around 1 µm in the NW. Simulations of similar devices identify the NW drift height, NW diameter and doping concentration as key parameters to achieve reasonable BV [101]. In another way around to ideal R_{on}, for higher BV, the suitable diameter and N_D in the drift region have to be chosen to achieve optimum depletion conditions (Fig. 13a). The simulated BV increases almost linear with the effective NW drift height and reaches 800 V for a height of 4 µm (Fig. 13b). The decent breakdown behavior of the simulated vertical NW FET is contributed to a reduced surface electric field (RESURF) effect leading to a more homogeneous electric field distribution [97].

The effect of L_D to the BV was demonstrated by work from Hu et al., in which they employed a bulk GaN as a substrate for their vertical GaN NW FETs having source contact on the bottom and drain on top of the substrate. This has resulted in longer L_D and induced BV of 513 V, which is higher than other vertical GaN NW FETs with sapphire substrate having shorter L_D. The authors attributed the reasons behind this high BV: 1) the bulk GaN as a substrate creates a long space (> 900 µm) between source on top and drain on bottom as it induces lower drain induced barrier lowering (DIBL) [42,103,104]; 2) the longer drift region (7 µm) with very low N_D creates lower electric field [17]; and 3) GAA structure provides better electrostatic control in channel. In case of D-mode GaN NW FETs, work from Cha *et al.* shows the bottom-gate structure has lower BV than top gated FETs due to the drift region space or the space between the gate and the drain [31,52,103]. In the bottom-gate GaN NW FETs, the drift region space was only 40 nm long. Meanwhile, for the top-gate GaN NW FETs, the drift region space was 1.5 µm as a consequence from the planar pitch of drain to gate structure.

Fig. 14 shows a figure of merit (FoM) of R_{on} against BV for 3D, vertical, and lateral GaN FETs [7,11,21,44,45,47,49,52,88,105–116]. It shows that some 3D vertical FETs are suitable for power electronics because they demonstrate good device performance (i.e., from MIT and Cornell) following Figure of Merit (FoM) [117,118]:

$$\text{FoM} = \frac{BV^2}{R_{on}} \tag{3}$$

However, the lateral GaN FETs still leads the FoM based on their structure, but the 3D vertical FETs very close to the best FoM which in near future could be improved.

4.2. Effect of diameter and number of the nanowire

Since the diameter and number of NW FETs have significant effects to the $I_{d,max}$ and $g_{m,max}$ of all lateral or vertical GaN NW FETs, they could be critical to be compared. The smallest diameter of lateral GaN NW FETs was exhibited by Huang *et al.* [27], where they fabricated 17 nm lateral GaN NW FET (*n*-doped GaN of $10^{18}-10^{19}$ cm^{-3}) that could obtain the $g_{m,max}$ of 22 mS/mm and normalized $I_{d,max}$ of 111 mA/mm. This device operated in D-mode with V_{th} of -8 V. A larger NW in lateral GaN NW FETs from Cha *et al.* [32] has a diameter of 33 nm (*n*-doped GaN of 1.44×10^{19} cm^{-3}) and back gate structure. In that device, the $I_{d,max}$ could reach 106 mA/mm, which is similar to the $I_{d,max}$ of the FETs developed by Huang *et al.* [27]. Moreover, lateral FETs with diameter of 95 nm by Motayed *et al.* [30] have the normalized $I_{d,max}$ of 8.4 mA/mm and $g_{m,max}$ of 1.1 mS/mm, which are very low than previous mentioned lateral GaN FETs. For almost the same diameter of 90 nm (Si-doped GaN of 7×10^{18} cm^{-3}), Gačević *et al.* [39] have shown that the normalized $I_{d,max}$ could reach 56 mA/mm with $g_{m,max}$ of 22 mS/mm. The largest diameter of lateral NW FETs (i.e., 290 nm, Si doped GaN of 1×10^{18} cm^{-3}) was shown by devices from Blanchard *et al.* [36], which obtained the normalized $I_{d,max}$ of 57 mA/mm and $g_{m,max}$ of 8.2 mS/mm. Using the same architecture but smaller wire diameter of 210 nm, higher normalized $I_{d,max}$ of 240 mA/mm and $g_{m,max}$ of 48 mS/mm could be achieved by the same group.

Thus, looking at the trend of the diameter from the lateral GaN NW FETs in respect to the $I_{d,max}$, the diameter dependence on the $I_{d,max}$ should be proportional to gate width, which follows this equation [35]:

$$I_{d,max} = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_{th})^2}{2} \tag{4}$$

where C_{ox} is the oxide capacitance and W is the gate width that depends on the NW diameter for GAA structure and is proportional to the $I_{d,max}$. From several lateral GaN FETs mentioned above, normalized $I_{d,max}$ seems not to have linear relationship with diameter since other parameters (i.e., μ and C_{ox}) may also vary from one to other devices.

For vertical GaN NW FETs, the diameter dependence on normalized $I_{d,max}$ can be seen from Yu *et al.* who had fabricated identical NW FETs with different wire numbers of 7 and 9 NWs and different diameters of 500 nm and 300 nm, respectively [48]. The normalized $I_{d,max}$ values of 314 mA/mm and 98 mA/mm were measured for GaN NW FETs with wire diameters of 500 nm and 300 nm, respectively, which follows Eq. (4).

Apart from that, Calarco *et al.* have shown that the Fermi level is pinned at the NW sidewall surfaces, yielding internal electric fields and

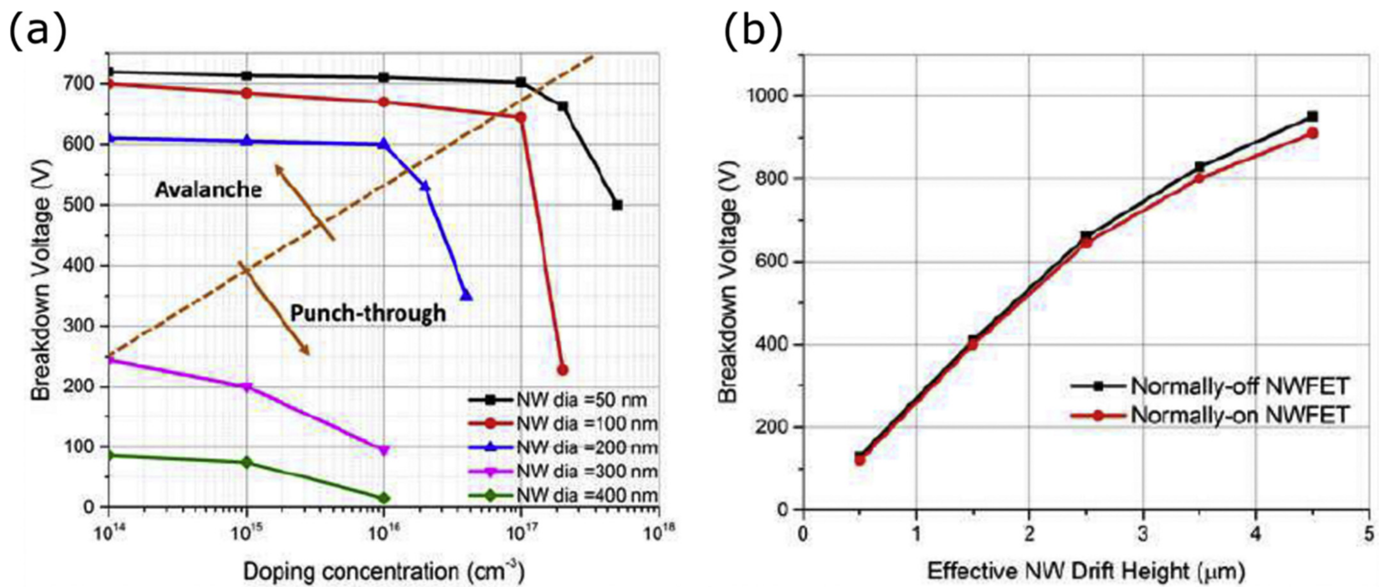

Fig. 13. Simulation study of the breakdown behavior for vertical *n-i-n* GaN NW FETs. (a) BV dependence on NW diameter and doping concentration for a NW drift height of 2.5 nm. (b) BV dependence on the NW drift height for NW diameter of 200 nm and a doping concentration of 10^{17} cm^{-3}. Reprinted with permission from [101]. Copyright 2017, The Electrochemical Society.

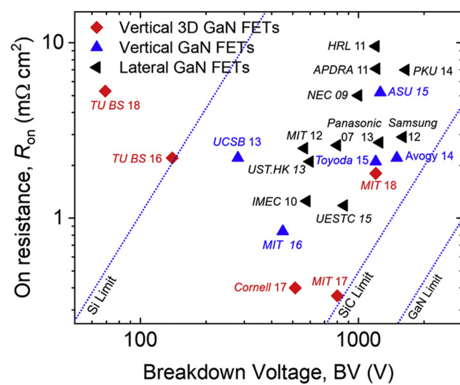

Fig. 14. Figure of merit (FoM) displaying R_{on} and BV from 3D GaN FETs made of vertical nanowires or nanofins in comparison with other types of vertical and lateral GaN FETs.

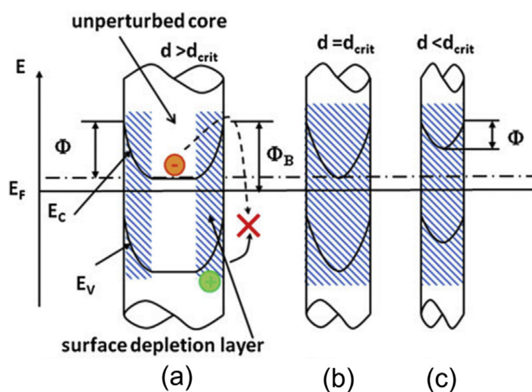

Fig. 15. Schematics of electric fields inside NW induced by Fermi level pinning at its sidewall surfaces. Three different conditions for NW with: (a) larger, (b) equal, and (c) smaller than the critical diameter (d_{crit}). The blue shadowed regions in the wires correspond to the depletion region, in which only for larger diameters, there is still a small conducting channel. © Materials Research Society 2011. Reproduced with permission from [17]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

thus full depletion for NWs below a critical diameter (i.e., around 80 nm) (Fig. 15) [17,31]. The Fermi level pinning at the NW sidewall surfaces depends on the oxidation state of the GaN surface, which can be modified by UV illumination. This consideration is important to understand the physic phenomena from the developed devices. For instance, in the vertical 3D GaN NW FETs developed by Yu et al., devices with NW diameter of 360 nm have exhibited a higher V_{th} of 1.5 V than that of 500 nm NW FETs (i.e., V_{th} of 1.2 V) [18,19].

4.3. Effect of gate length of the nanowire

Besides the gate width W that has an effect to the output performances of the GaN NW FETs, the gate length L also induces opposite influence compared to W, as mentioned in Eq. (4). The gate length from several lateral GaN NW FETs was varied from 0.3 μm to 35 μm. Huang *et al.* used L of 3 μm similar to Cha *et al.* who set L to be 3–4 μm in their single GaN NW FETs devices [27,32]. With similar L and doping concentrations of 10^{18}–10^{19} cm^{-3} (Huang *et al.* [33]) and 1.44×10^{19} cm^{-3} (Cha *et al.* [38]), the V_{th} of the bottom gate structure FETs [33] was −8 V, while the top gate structure FETs [38] exhibited V_{th} of −7.5 V. It should be noted that those two FETs have different diameter sizes (i.e., the latter has almost two times larger diameter). In those FETs, the gate structure and doping concentration have a major role to the difference of obtained V_{th} rather than the electrostatic effect of NW diameter. Thus, the lower V_{th} found in FETs of Huang *et al.* [33] was suggested to be attributed to lower doping concentration and higher electric fields in the gate channel. Furthermore, using similar NW diameter, Cha *et al.* [38] made a comparison of top and bottom gate structures with L of 3 μm and 4 μm, respectively. The bottom-gate FET has a lower V_{th} of −12.5 V than top-gate FET (V_{th} > −7.5 V). The longer gate length may induce higher electric fields. Thus, it needs lower voltage to create the channel than smaller gate length, even though the gate was on the top of the NW. Apart from that, the longer drift region space at lateral top gate structure results in higher BV of > 60 V, which is about four times higher than that of bottom gate structure [31,103].

In the vertical direction, similar with previous mentioned *c*-axis FETs, the GAA structure provides advantages for controlling the electric fields [48,49]. The GAA architecture is found to be obviously affecting the BV since it has enhanced electrostatic control on the depletion

region and can suppress drain-induced barrier lowering (DIBL) [119]. With DIBL effect or parasitic effect being suppressed, the BV and V_{th} of GAA vertical GaN NW FET could then be increased into larger values than those of lateral ones, as demonstrated by Hu *et al.* [49,120].

Another effect of gate length to V_{th} was demonstrated by Jo *et al.* and Son *et al.* [46,51]. Jo *et al.* demonstrated vertical GaN NW FETs with shorter GAA structure of 0.12 μm than Son *et al.* (L of 0.3 μm) on 100 nm and 120 nm NWs, respectively. Even though the unintentionally doped GaN was used at the drift region for both NW FETs, different V_{th} values were achieved, i.e., 0.6 V [50] and 0.4 V [54]. It could be seen that besides the effect of the doping concentration in the GaN NW channel that enhances the surface depletion layer thickness [17], the effects of shorter gate length and smaller wire diameter in FETs of Jo *et al.* [50] can be the reason for higher threshold voltage.

5. Reliability issues of 3D GaN FETs

5.1. Low frequency noise characteristics

Low frequency noise (LFN) characterization is an efficient diagnostic tool to evaluate the electrical properties of complex interfaces. LFN is important to analyze the defects and non-idealities in semiconductor devices, which directly or indirectly impact device performances and reliability. Furthermore, in very small area devices, the LFN is dominant that introduces high levels of fluctuations and further performance risks can appear. For past several years, the low frequency noise characterization of GaN HFETs, MOSHFETs, and MISHFETs were extensively studied. Vodapally et al., studied the low frequency noise characteristics of AlGaN/GaN NF FETs for the first time and further compared with AlGaN/GaN MISHFET (planar device) and analyzed the drain lag effect (schematic as shown in Fig. 16a [121]). The authors showed the better noise performances in AlGaN/GaN NF FET compared to that of planar device as depicted in Fig. 16b. They claim that both devices follow the carrier number fluctuation model, whereas the NF FETs suffer much less charge trapping effect compared to the MISHFET (i.e., two orders lower trap density was observed). The authors investigated the drain lag phenomena using LFN measurements. It was shown that the NF FET devices exhibited typical 1/f noise characteristics with γ = 1, whereas the planar AlGaN/GaN MISHFET exhibited γ = 2 along with bias dependent Lorentz components (G-R bulges) in the saturation region (Figs. 16c,d).

In 2017, the same group also analyzed the low frequency noise measurements for AlGaN/GaN Omega-NF FETs [122]. The schematic and TEM image are shown in the Fig. 16e. The authors showed that the LFN in AlGaN/GaN nanowire omega-NF FETs is dependent on the width of the fin (Fig. 16f). On the other hand, the AlGaN/GaN nanowire omega-NF FETs with two types of conductions (2DEG and MOS channels) are dominated by carrier number fluctuations irrespective of the fin width. In relatively wide fin devices, the current is governed by the AlGaN/GaN HEMT structure and the noise by carrier capture in GaN traps. It was found that in the narrow fin devices, the noise mainly stems from the carrier trapping in the sidewall Al_2O_3 gate dielectric. The volume accumulation in the body masks the GaN traps and results in less charge trapping. The authors also studied the LFN characteristics

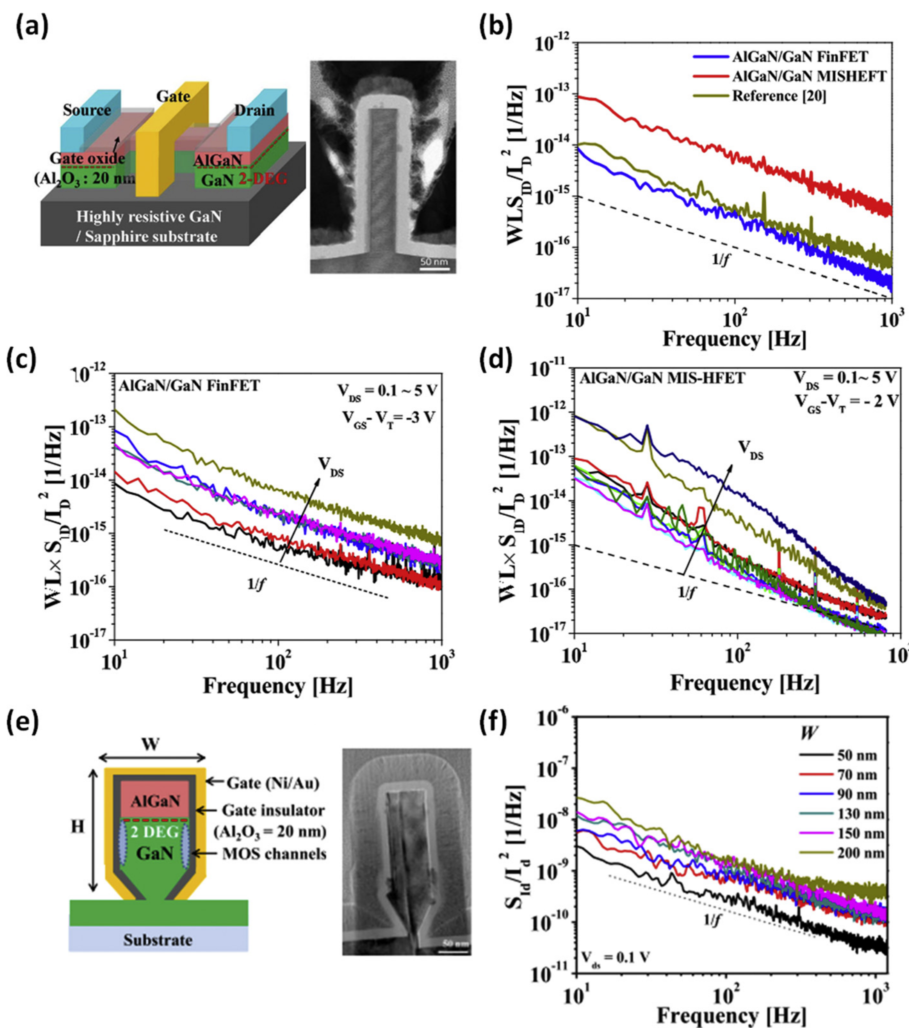

Fig. 16. (a) Schematic and TEM image of AlGaN/GaN FinFET. (b) Area normalized drain-current spectral density as a function of the frequency of AlGaN/GaN FinFET and MISHFET at V_{gs}–V_{th} = 0.2 V compared with Ref. [122]. (c) Area normalized drain-current spectral density as a function of the frequency at different drain voltages (V_{ds} = 0.1–5 V) for AlGaN/GaN FinFET and (d) MISHFET. © [2017] IEEE. Reprinted, with permission, from [121]. (e) Schematic and TEM image of AlGaN/GaN omega gate FinFET, and (f) normalized drain current spectral density according to the frequency of the fabricated AlGaN/GaN omega-FET with different nanowire widths (W) at V_{ds} = 0.1 V, $V_{gs}-V_{th}$ = 0.4 V. © [2017] IEEE. Reprinted, with permission, from [122].

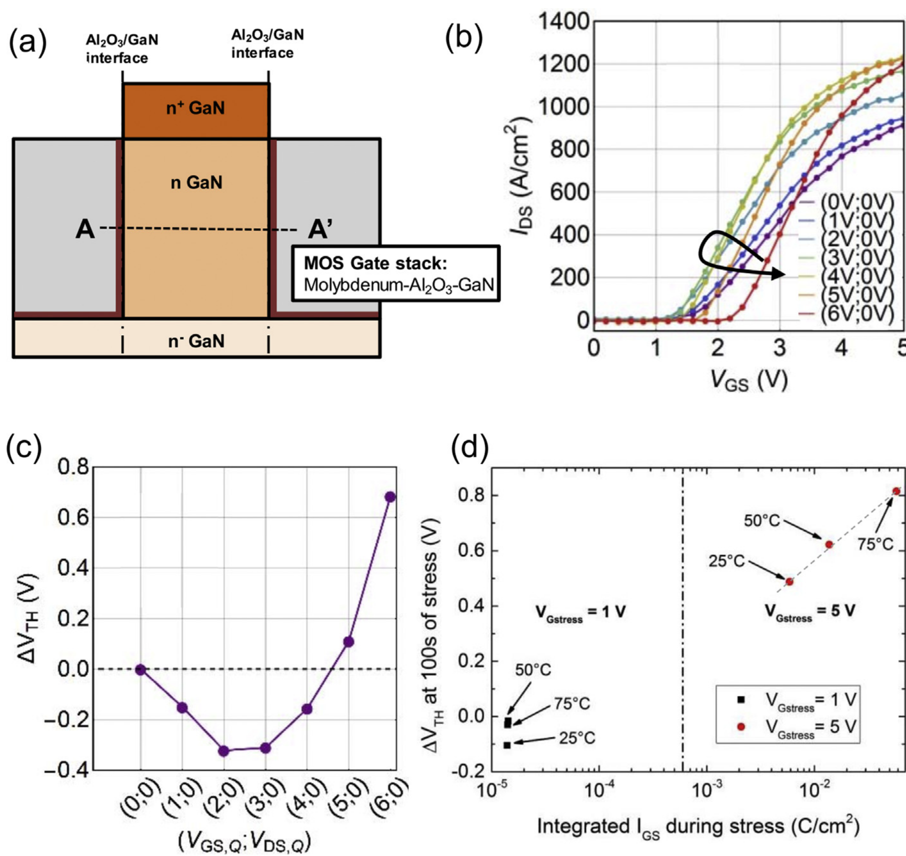

Fig. 17. (a) Schematic of vertical GaN on GaN FETs reported by Ruzzarin *et al.*, (b) transfer characteristics at V_{gs} of 5 V at quiescent gate bias from 0-6 V, (c) V_{th} negative shift at around $V_{gs,Q}$ = 0-2 V and positive shift at $V_{gs,Q} \geq$ 2 V, and (d) V_{th} plot to the gate current on different temperatures at V_{gs} stress of 1 and 5 V. © [2017] IEEE. Reprinted, with permission, from [96].

for AlGaN/GaN NF FETs with TMAH surface treatment [123]. The author showed the improved LFN performances for the device with TMAH surface treatment due to the improved interface quality between the gate dielectric and GaN sidewall surface. The interface trap density was two orders reduced in TMAH treated devices.

5.2. Threshold voltage shift

The threshold voltage V_{th} dependence to gate bias stress was demonstrated by Ruzzarin *et al.* on vertical GaN on GaN FETs having Al_2O_3 and Mo as a gate dielectric and a gate metal layer, respectively (Fig. 17a) [96]. The dual pulsed measurement was demonstrated using fast sweeps of 5 µs (on-state) and 5 ms (off-state) with a quiescent bias (*Q*) at the V_{gs} and V_{ds} for 100 s stress and 1000 s recovery. The V_{th} changed at different $V_{gs,Q}$ = 0–6 V and constant $V_{ds,Q}$ = 0 V (Figs. 17b,c). At $V_{gs,Q}$ < 2 V, the negative shift occurs due to the electron de-trapping from the oxide layer to the metal layer. Meanwhile, the positive V_{th} was observed due to higher gate leakage current at $V_{gs.Q}$ = 6 V and made the electron trapping or electron migration from the accumulation layer or channel to the oxide layer [96,124,125].

However, V_{th} does not only depend on the V_{gs} stress, but also temperature, as shown in Fig. 17d, in which it increases with temperature. For V_{gs} stress = 1 V at different temperatures, the V_{th} does not shift dramatically. Whereas, for V_{gs} stress = 5 V, the V_{th} equally changes with temperature. This occurs due to, at V_{gs} stress = 1 V, the de-trapping was not thermally activated while on V_{gs} = 5, the trapping was thermally activated inducing electron to move to oxide layer and increasing the V_{th}.

As mentioned previously, the BV of the FETs depends on the drift channel length L_D and its doping concentration N_D [101]. The higher the N_D, the lower the BV. Meanwhile, longer drift channel will increase the BV. For instance, the works from Sun *et al.* that used a bulk GaN as their FET substrate have taken an advantage from its thickness to obtain very long drift channel region by locating the drain on the bottom substrate, while source on the top of the Fin structures. This structure could produce a BV of up to 800 V [42].

Another important aspect that has to be considered is the current collapse due to trapping and de-trapping in oxide layer or interface between GaN NWs and oxide. Since the surface charging related to this phenomenon could happen on the interface of oxide layer and GaN NW, the high quality or high-*k* dielectric (e.g., SiN or Al_2O_3) material could maintain this problem due to suppressed Fermi level pinning on NW sidewalls [17]. It is essential because additional electric field on the drift region due to negative surface charge could reduce the $I_{d,max}$ or the FETs pinch-off voltage [31]. At a high voltage, the mechanism of charge trapping on GaN NW FETs with Al_2O_3 as passivation layer has been proposed by Ruzzarin et al., as shown in Fig. 18 [96]. This mechanism could revoke the stability of V_{th} or lead to higher V_{th} on the MOSFETs at high voltage (and temperature) which is very important for high power device application. On the other hand, charge de-trapping from oxide to

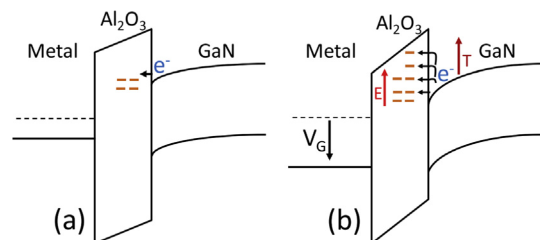

Fig. 18. A charge trapping mechanism proposed by Ruzzarin *et al.* on GaN NF FET at (a) positive bias creating a charge trapping inside the oxide layer from GaN and at (b) higher positive bias where more charges are trapped in the oxide layer generating higher average carrier energy. © [2017] IEEE. Reprinted, with permission, from [96].

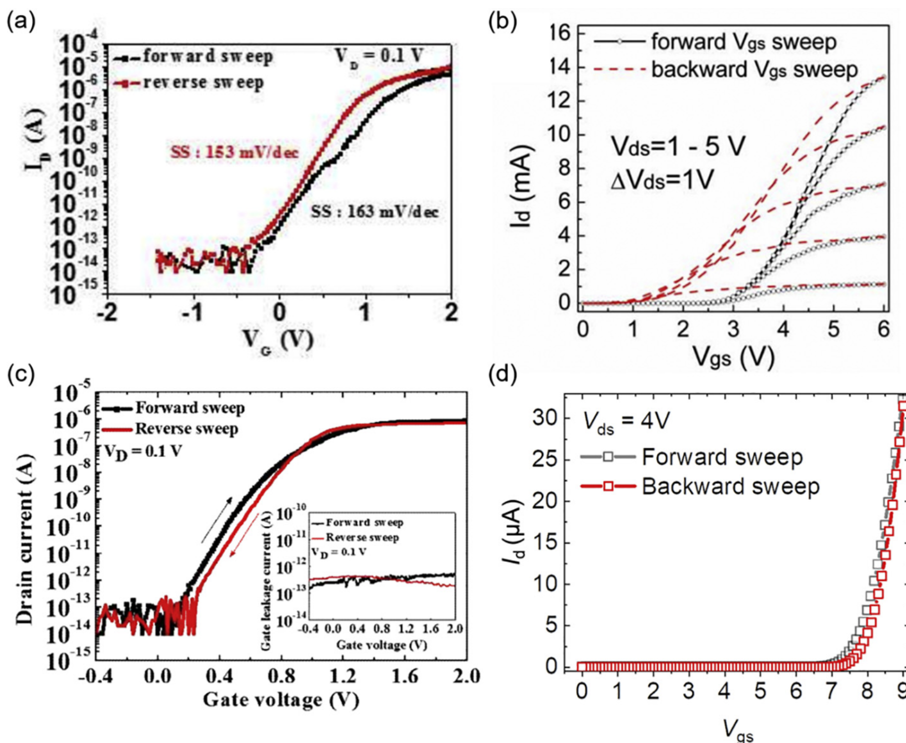

Fig. 19. A gate hysteresis from several 3D FETs: (a) vertical GaN NW FETs with Al_2O_3 passivation layer from Jo *et al.* © [2015] IEEE. Reprinted, with permission, from [46]. (b) Vertical *n-p-n* GaN NW FETs with SiO_2 passivation layer from Yu *et al.* © [2018] IEEE. Reprinted, with permission, from [52]. (c) Vertical GaN NW FETs with Al_2O_3 layer from Son *et al.* Reprinted from [51]. Copyright 2018, with permission from Elsevier. (d) Vertical *n-p-n* GaN NW FETs like in [52] with Al_2O_3 passivation layer.

gate metal might occur at low or small negative bias leading to decrease of the V_{th}. At the end, as mentioned previously, the quality of oxide layer has a major role to overcome this issue.

5.3. Gate hysteresis

The gate hysteresis or V_{th} shifted on backward or forward sweep as explained in previous section due to trapping or detrapping effect and the Fermi level pinning on GaN NW sidewall could be reduced by using a better dielectric material. For instance, an anticlockwise hysteresis in lateral GaN NW FETs from Blanchard *et al.* and vertical GaN NW FETs from Yu *et al.* FETs (Fig. 19b), as attributed by the authors (Yu et al.), caused by mobile ion and high trapping density in interface between SiO_2 and GaN NW which comes from contaminants during certain device processing steps [36,52,126]. As mentioned before, the hysteresis due to higher trapping density between GaN NW and oxide layer could be reduced by applying Al_2O_3 as a dielectric material since it has higher density and E_a compared to SiO_2, which was used in their previous lateral GaN NW FETs (i.e., $Al_2O_3E_a \approx 4.2$ eV) [38,42,49,51,127,128]. However, lateral NW GaN FETs from Blanchard *et al.* in 2012 do not show any improvement of gate hysteresis, even though Al_2O_3 has already been used [38]. An approach that might solve this problem is the vertical architecture, where current collapse at higher drain current causing the memory effect or hysteresis on the FETs can be minimized [42,103].

Again, very low gate hysteresis of vertical GaN NW FETs were demonstrated by Jo *et al.* (Fig. 19a) and Son *et al.* (Fig. 19c) which show logarithmic dual sweep voltage transfer characteristics with threshold voltage shift $\Delta V_{th} = 0.07$ V. In this case, the lower interface trap capacitance (C_{it}) or mobile ion was hindered by using alkali free wet etching and denser dielectric material of Al_2O_3 [46,51]. To demonstrate more evidences that Al_2O_3 could suppress the gate hysteresis than SiO_2, we have currently used Al_2O_3 as dielectric material for similar FET architecture by Yu *et al.* on the *n-p-n* vertical GaN NW FETs with NW number of 9 and diameter of 440 nm. As shown in Fig. 19d, the gate hysteresis was suppressed to almost zero or $\Delta V_{th} = 0.2$ V when the Al_2O_3 was used as dielectric material.

5.4. Self-heating

GaN transistors, particularly in vertical architectures, can reach enormous power density, which is one of the biggest advantages of this technology and enables very compact devices. However, high power densities are inherently connected with a strong heat generation due to the dissipated power. Moreover, temperatures above 300 °C are easily reached during high power operation, which can significantly degrade the device performance [129]. Therefore, a good thermal management to remove the heat from the active device region is essential for high power GaN electronics.

Various methods have been reported for evaluating device temperature, including physical, optical, and electrical methods [130]. The highest temperature is typically obtained close to the drain side of the gate, where the electric field reaches its peak. Since these hot spots are often buried under metal (e.g., gate field plates), extracting the channel temperature is challenging [131]. Thus, simulations are often used to support the thermal analysis. Pulsed measurements can be employed to mitigate self-heating and comparison with results obtained in static operation allows to investigate how the increased channel temperature affects the device performance. Higher temperature is known to reduce the low-field electron mobility due to enhanced phonon scattering, resulting in lower saturation current and velocity, which increases the R_{on} drastically [132]. Tunneling becomes more likely with rising temperature that can cause increase of the gate leakage. Furthermore, increasing subthreshold swings are reported to indicate loss of channel control. Since trapping is strongly temperature dependent, the threshold voltage can be shifted as well, in either positive or negative direction [133,134].

While highly heat conductive materials like SiC [136] or diamond [137] are proposed to reduce the thermal resistance of the substrate, the usage of 3D GaN structures can enhance the heat removal through the contact electrodes and thus improve the performance of FET devices, which was demonstrated for fin-shaped tri-gate HEMTs. Apart from a lower average temperature that was attributed to the increased surface area supporting heat removal, the tri-gate HEMT showed a better thermal stability of the on-resistance compared to the

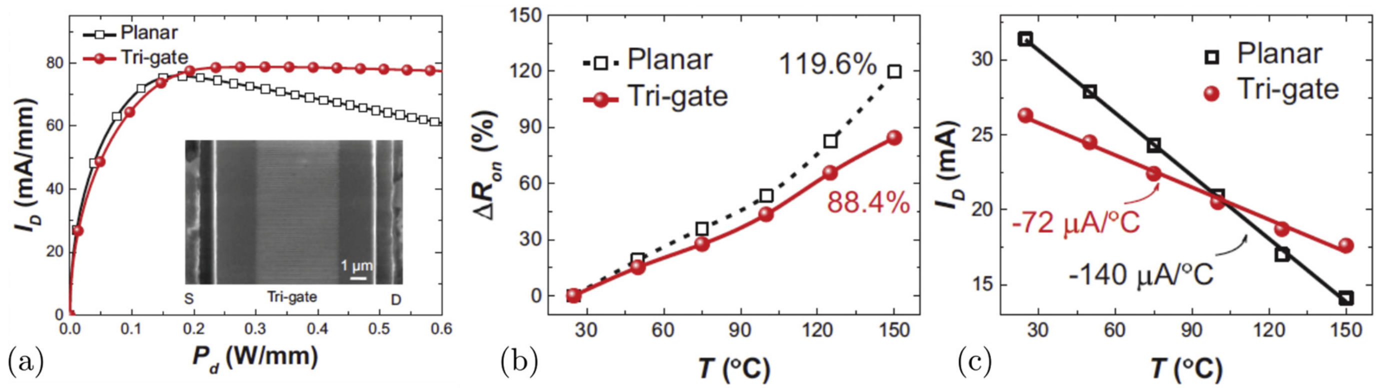

Fig. 20. Comparison of planar and nanostructured tri-gate HEMTs. (a) Drain current over dissipated power (Inset: SEM image of the tri-gate HEMT), (b) temperature dependency of on-resistance, and (c) drain current. © [2016] IEEE. Reprinted, with permission, from [135].

corresponding planar HEMT structure [138].

Severe self-heating is observed in a lateral nanowire channel GaN MOSFET with wrap-around gate (Fig. 20). The drain current is reduced by up to 50% when comparing static and pulsed measurements, in which channel temperatures up to 300 °C were estimated by thermal simulations. The authors state that the isolation to the buffer is responsible for the extensive self-heating [139].

Kamrani *et al.* compared the thermal performance of two different vertical 3D geometries, namely a vertical NF FET with drain-bottom and a NW FET with drain-top configuration as introduced in [47,88], respectively, using electrothermal simulations [140]. As determined by the maximum vertical electric field, both devices reached the highest temperatures at the drain side of the channel. However, the different positions of the drain electrode on the backside of the substrate (NF FET) or on the NW top (NWFET) are shown to have a large impact on the thermal flux. The heat removal in the NW FET with a drain-top configuration is concluded to be more effective, because most power is dissipated close to the NW top, where it can be easier extracted via the drain and gate contacts [140].

While highly heat conductive materials like SiC or diamond are discussed to reduce the thermal resistance of the substrate, the contacts of nanostructure transistor can serve as efficient heat conductors when they are located close to the area where the most power is dissipated. Kamrani *et al.* simulated the thermal performance of a vertical GaN NF FET and NW FET device as proposed in [47,88]. The peak temperature of the NW FET is found to be located close to the top drain contact of the device, which serves as heat sink and improves the thermal performance of the device significantly compared to the NF FET with a drain at bottom configuration [140]. The simulations indicate that a drain contact on top of the nanostructures is beneficial for the thermal device performance, as it can conduct the heat dissipation in the maximum field region to be more efficient.

5.5. Linearity

Many RF applications require high-frequency performance over a large input signal range. Non-linearity is a critical issue as it can lead to distortion of the amplified input signal. In MOSFETs, the g_m is usually strongly dependent on the drain current and decreases rapidly after reaching the maximum [142], in particular for small gate length devices, which strongly affects their linearity [79]. This effect is becoming even more pronounced when the gate length of transistors is scaled down. Thus, a broad transconductance characteristic is desired to obtain good linearity [99].

Several origins for the drop of g_m were proposed including emission of optical phonons [143], interface roughness [144], and self-heating effect [129], while the most prominent explanation is based on the source access resistance, which was shown to increase drastically with the drain current in GaN HEMTs [145–147]. The reduced source access resistance in a self-aligned HEMT structure with regrown n^+-GaN contacts reported by Shinohara *et al.* could suppress the g_m non-linearity [148], but the low breakdown voltage of the self-aligned device makes it unsuitable for high power RF applications.

Nanostructured HEMTs can enhance the RF linearity significantly [99,142,144]. By etching the nanofin structures into the channel region, a flatter g_m profile could be achieved, since the source access area is mainly non-etched and thus higher conductive than the channel (Fig. 21) [142]. The source access resistance can be minimized by

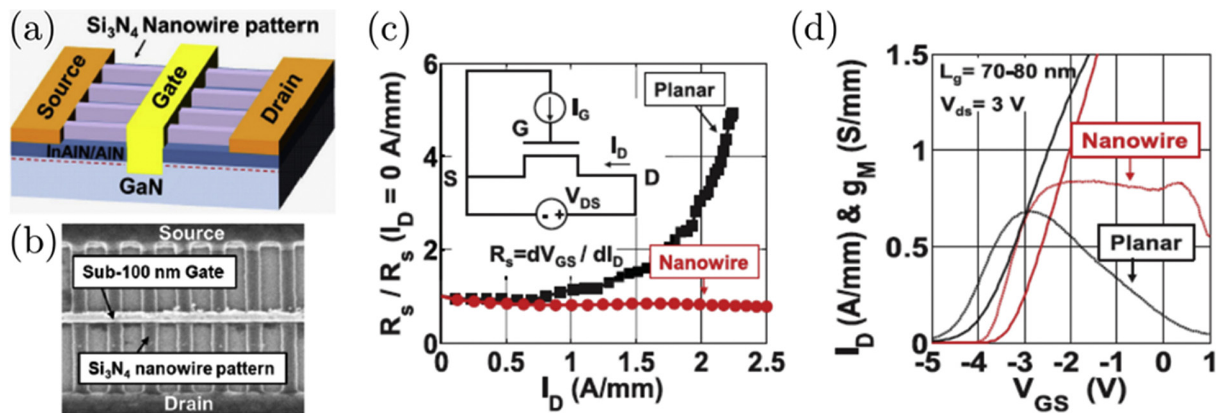

Fig. 21. (a) Schematic of the fin-channel HEMT, (b) SEM image of the fabricated device, (c) normalized source resistance in dependence of the drain current for the planar and nanostructured devices, and (d) comparison of I_dV_g characteristics and transconductance for the planar and nanostructured devices. © [2013] IEEE. Reprinted, with permission, from [141].

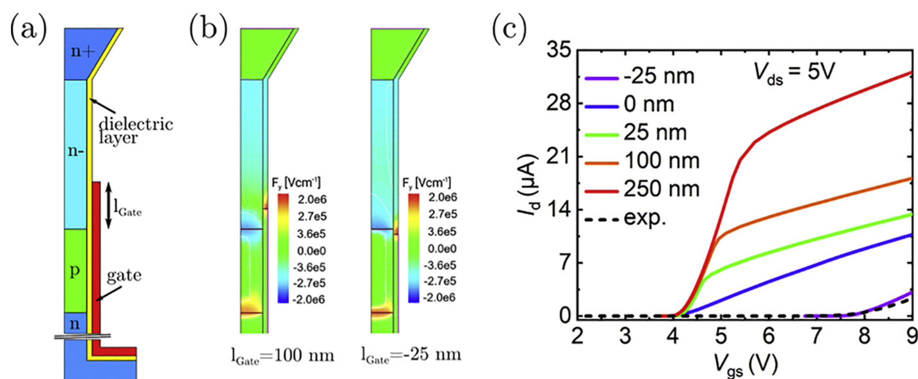

Fig. 22. (a) Schematic of the simulated vertical GaN NW FET device. (b) Simulated *E*-field concentration with a positive and negative gate extension showing the depletion. (c) I_dV_g characteristics in dependence of the gate extension l_{Gate}.

reducing the fin length [100]. Lateral AlGaN/GaN NF FETs with short fins extending only below the gate obtained flatter g_m characteristics than similar devices with longer fins or the corresponding planar HEMT [149]. This also supports the assumption that the non-linear source access resistance is dominating this effect. Since the transconductance profile of a nanofin HEMT depends on the fin dimensions, a combination of several parallel fins with different widths was proposed to broaden the transconductance on device-level in order to further improve linearity [150].

5.6. Problems in 3D processing

The three-dimensionality increases the complexity of device processing, so that various issues can occur during the processing steps, which strongly influence the device performance. Unfortunately, such problems are rarely discussed in publications.

One of the most important and critical steps for the fabrication of vertical GaN NW FETs is the formation of the wrap-around gate. The positioning of the gate edge towards the drain side affects the electric field distribution in off-state and therefore can have a large impact on the breakdown voltage. In order to reach high breakdown voltages, the distance between drain and the edge of the gate should be sufficiently large. However, if the gate is not covering the whole channel region, severe device degradation can occur as observed experimentally and verified in the TCAD simulation study shown in Fig. 22. Here, a vertical NW FET with a p-doped channel and drain contact on the NW top is investigated as realized in [52]. While positive gate extension only affects the current density of the device due to a reduced on-resistance, a negative gate extension of -25 nm is already sufficient to shift the threshold voltage 5 V up and reduce the current density by two orders of magnitude. This is caused by the fully depletion of the upper channel part and above due to the pn-junction and inefficient gate control as can be seen in Fig. 22c. A precise control of the gate formation process is necessary to prevent such problems.

6. Summary and outlook

From the demonstrations of 3D GaN field-effect transistors (FETs) based on nanowire (NW) and nanofin (NF) structures within the last decade, the 3D GaN nanoarchitectures have proven themselves to be versatile and adaptable to solve several problems that occur on planar FETs. Both bottom-up and top-down fabrication approaches from several devices have been compared demonstrating their advantages and disadvantages. Moreover, complex 3D processing has been described where several strategies and techniques have been proposed to ease the device production (e.g., back etch, mushroom-like structure, and planarization). Important device parameters and characteristics have been summarized that are used to evaluate the performances of the lateral and vertical GaN NW and NF FETs. 3D NW FETs with gate-all-around (GAA) structures have demonstrated better electrostatic control in the gate channel compared to normal top gate structures, which consequently can enhance the electrical characteristics of the transistors (e.g., subthreshold swing (SS), breakdown voltage (BV), and maximum drain current ($I_{d,max}$)). The effects of some device structures on their performances, including on- and-off states as well as the diameter, number, and gate length of the NW and NFs have been discussed. Furthermore, reliability issues including threshold voltage instability, gate hysteresis, self-heating, and linearity, which are normally faced during the device characterization have been reviewed, providing the guidelines for development and improvement of the 3D GaN transistors. All in all, regardless of the needed continuously ongoing optimization, the 3D GaN FETs are believed to be one of the promising routes for the next generation of nanoelectronics beyond Moore's law.

Competing interests

The authors declare no conflict of interest.

Acknowledgements

This work has been performed within the projects of 'LENA-OptoSense' funded by the Lower Saxony Ministry for Science and Culture (MWK) *Landesmittel des Niedersächsischen Vorab* and '3D Concepts for Gallium-Nitride Electronics (3D GaN)' funded by the German Research Foundation (DFG). The authors thank Friedhard Römer and Bernd Witzigmann from the University of Kassel, Germany for simulation of the GaN nanowire devices and constructive discussion on the topic of 3D GaN electronics. We also acknowledge the support from the Indonesian-German Center for Nano and Quantum Technologies (IG-Nano) and theMinistry of Research, Technology and Higher Education of the Republic of Indonesia (RISTEKDIKTI).

References

[1] T. Hashizume, S. Ootomo, H. Hasegawa, Suppression of current collapse in insulated gate AlGaN/GaN heterostructure field-effect transistors using ultrathin Al_2O_3 dielectric, Appl. Phys. Lett. 83 (2003) 2952–2954, https://doi.org/10.1063/1.1616648.

[2] T. Kikkawa, M. Nagahara, N. Okamoto, Y. Tateno, Y. Yamaguchi, N. Hara, K. Joshin, P.M. Asbeck, Surface-charge controlled AlGaN/GaN-power HFET without current collapse and gm dispersion, International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224), IEEE, Washington, DC, USA, 2001, , https://doi.org/10.1109/IEDM.2001.979574 25.4.1–25.4.4.

[3] S. Huang, Q. Jiang, S. Yang, C. Zhou, K.J. Chen, Effective passivation of AlGaN/GaN HEMTs by ALD-grown AlN thin film, IEEE Electron Device Lett. 33 (2012) 516–518, https://doi.org/10.1109/LED.2012.2185921.

[4] M.T. Hasan, T. Asano, H. Tokuda, M. Kuzuhara, Current collapse suppression by gate field-plate in AlGaN/GaN HEMTs, IEEE Electron Device Lett. 34 (2013) 1379–1381, https://doi.org/10.1109/LED.2013.2280712.

[5] H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P.R. Chalker, M. Charles,

K.J. Chen, N. Chowdhury, R. Chu, C. De Santi, M.M. De Souza, S. Decoutere, L. Di Cioccio, B. Eckardt, T. Egawa, P. Fay, J.J. Freedsman, L. Guido, O. Häberlen, G. Haynes, T. Heckel, D. Hemakumara, P. Houston, J. Hu, M. Hua, Q. Huang, A. Huang, S. Jiang, H. Kawai, D. Kinzer, M. Kuball, A. Kumar, K.B. Lee, X. Li, D. Marcon, M. März, R. McCarthy, G. Meneghesso, M. Meneghini, E. Morvan, A. Nakajima, E.M.S. Narayanan, S. Oliver, T. Palacios, D. Piedra, M. Plissonnier, R. Reddy, M. Sun, I. Thayne, A. Torres, N. Trivellin, V. Unni, M.J. Uren, M. Van Hove, D.J. Wallis, J. Wang, J. Xie, S. Yagi, S. Yang, C. Youtsey, R. Yu, E. Zanoni, S. Zeltner, Y. Zhang, The 2018 GaN power electronics roadmap, J. Phys. D. Appl. Phys. 51 (2018) 163001, , https://doi.org/10.1088/1361-6463/aaaf9d.

[6] W.B. Lanford, T. Tanaka, Y. Otoki, I. Adesida, Recessed-gate enhancement-mode GaN HEMT with high threshold voltage, Electron. Lett. 41 (2005) 449, https://doi.org/10.1049/el:20050161.

[7] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, Gate injection transistor (GIT)—a normally-off AlGaN/GaN power transistor using conductivity modulation, IEEE Trans. Electron Devices 54 (2007) 3393–3399, https://doi.org/10.1109/TED.2007.908601.

[8] I. Hwang, J. Kim, H.S. Choi, H. Choi, J. Lee, K.Y. Kim, J.-B. Park, J.C. Lee, J. Ha, J. Oh, J. Shin, U.-I. Chung, p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current, IEEE Electron Device Lett. 34 (2013) 202–204, https://doi.org/10.1109/LED.2012.2230312.

[9] B. Bakeroot, A. Stockman, N. Posthuma, S. Stoffels, S. Decoutere, Analytical model for the threshold voltage of p-(Al)GaN high-electron-mobility transistors, IEEE Trans. Electron Devices 65 (2018) 79–86, https://doi.org/10.1109/TED.2017.2773269.

[10] Y. Cai, Y. Zhou, K.M. Lau, K.J. Chen, Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: from depletion mode to enhancement mode, IEEE Trans. Electron Devices 53 (2006) 2207–2215, https://doi.org/10.1109/TED.2006.881054.

[11] S. Chowdhury, B.L. Swenson, M.H. Wong, U.K. Mishra, Current status and scope of gallium nitride-based vertical transistors for high-power electronics application, Semicond. Sci. Technol. 28 (2013) 074014, , https://doi.org/10.1088/0268-1242/28/7/074014.

[12] T. Oka, Y. Ueno, T. Ina, K. Hasegawa, Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV, Appl. Phys. Express 7 (2014) 021002, , https://doi.org/10.7567/APEX.7.021002.

[13] S. Li, A. Waag, GaN based nanorods for solid state lighting, J. Appl. Phys. 111 (2012) 071101, , https://doi.org/10.1063/1.3694674.

[14] J.L. Johnson, Y. Choi, A. Ural, W. Lim, J.S. Wright, B.P. Gila, F. Ren, S.J. Pearton, Growth and characterization of GaN nanowires for hydrogen sensors, J. Electron. Mater. 38 (2009) 490–494, https://doi.org/10.1007/s11664-008-0596-z.

[15] M. Gonzalez, L. Dillemans, K. Cheng, S.J. Jiang, P.M. Vereecken, G. Borghs, R.R. Lieten, Strain relaxation in GaN nanopillars, Appl. Phys. Lett. 101 (2012) 253102, , https://doi.org/10.1063/1.4772481.

[16] S.D. Hersee, A.K. Rishinaramangalam, M.N. Fairchild, L. Zhang, P. Varangis, Threading defect elimination in GaN nanowires, J. Mater. Res. 26 (2011) 2293–2298, https://doi.org/10.1557/jmr.2011.112.

[17] R. Calarco, T. Stoica, O. Brandt, L. Geelhaar, Surface-induced effects in GaN nanowires, J. Mater. Res. 26 (2011) 2157–2168, https://doi.org/10.1557/jmr.2011.211.

[18] I. Ferain, C.A. Colinge, J.-P. Colinge, Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature 479 (2011) 310–316, https://doi.org/10.1038/nature10676.

[19] J.-W. Yu, P.-C. Yeh, S.-L. Wang, Y.-R. Wu, M.-H. Mao, H.-H. Lin, L.-H. Peng, Short channel effects on gallium nitride/gallium oxide nanowire transistors, Appl. Phys. Lett. 101 (2012) 183501, , https://doi.org/10.1063/1.4764554.

[20] K. Ohi, J.T. Asubar, K. Nishiguchi, T. Hashizume, Current stability in multi-mesa-channel AlGaN/GaN HEMTs, IEEE Trans. Electron Devices 60 (2013) 2997–3004, https://doi.org/10.1109/TED.2013.2266663.

[21] B. Lu, E. Matioli, T. Palacios, Tri-gate normally-off GaN power MISFET, IEEE Electron Device Lett. 33 (2012) 360–362, https://doi.org/10.1109/LED.2011.2179971.

[22] M. Azize, T. Palacios, Top-down fabrication of AlGaN/GaN nanoribbons, Appl. Phys. Lett. 98 (2011) 042103, , https://doi.org/10.1063/1.3544048.

[23] K.-S. Im, R.-H. Kim, K.-W. Kim, D.-S. Kim, C.S. Lee, S. Cristoloveanu, J.-H. Lee, Normally off single-nanoribbon Al2O3/GaN MISFET, IEEE Electron Device Lett. 34 (2013) 27–29, https://doi.org/10.1109/LED.2012.2222861.

[24] K.-S. Im, Y.-W. Jo, J.-H. Lee, S. Cristoloveanu, J.-H. Lee, Heterojunction-free GaN nanochannel FinFETs with high performance, IEEE Electron Device Lett. 34 (2013) 381–383, https://doi.org/10.1109/LED.2013.2240372.

[25] K.-S. Im, V. Sindhuri, Y.-W. Jo, D.-H. Son, J.-H. Lee, S. Cristoloveanu, J.-H. Lee, Fabrication of AlGaN/GaN Ω-shaped nanowire fin-shaped FETs by a top-down approach, Appl. Phys. Express 8 (2015) 066501, , https://doi.org/10.7567/APEX.8.066501.

[26] K.-S. Im, C.-H. Won, Y.-W. Jo, J.-H. Lee, M. Bawedin, S. Cristoloveanu, J.-H. Lee, High-performance GaN-based nanochannel FinFETs with/without AlGaN/GaN heterostructure, IEEE Trans. Electron Devices 60 (2013) 3012–3018, https://doi.org/10.1109/TED.2013.2274660.

[27] Y. Huang, X. Duan, Y. Cui, C.M. Lieber, Gallium nitride nanowire nanodevices, Nano Lett. 2 (2002) 101–104, https://doi.org/10.1021/nl015667d.

[28] X. Duan, C.M. Lieber, Laser-assisted catalytic growth of single crystal GaN nanowires, J. Am. Chem. Soc. 122 (2000) 188–189, https://doi.org/10.1021/ja993713u.

[29] Q. Li, G.T. Wang, J. Wright, H. Xu, T.S. Luk, I. Brener, J. Figiel, K. Cross, M.H. Crawford, S.R. Lee, D.D. Koleske, Nanofabrication of Tunable Nanowire Lasers via Electron and Ion-Beam Based Techniques, Sandia National Laboratories, Albuquerque, New Mexico and Livermore, California, 2012http://prod.sandia.gov/techlib/access-control.cgi/2012/127665.pdf , Accessed date: 6 September 2017.

[30] A. Motayed, M. He, A.V. Davydov, J. Melngailis, S.N. Mohammad, Realization of reliable GaN nanowire transistors utilizing dielectrophoretic alignment technique, J. Appl. Phys. 100 (2006) 114310, , https://doi.org/10.1063/1.2397383.

[31] B. Witzigmann, F. Yu, K. Frank, K. Strempel, M.F. Fatahilah, H.W. Schumacher, H.S. Wasisto, F. Römer, A. Waag, Performance analysis and simulation of vertical gallium nitride nanowire transistors, Solid State Electron. 144 (2018) 73–77, https://doi.org/10.1016/j.sse.2018.03.005.

[32] H.-Y. Cha, H. Wu, M. Chandrashekhar, Y.C. Choi, S. Chae, G. Koley, M.G. Spencer, Fabrication and characterization of pre-aligned gallium nitride nanowire field-effect transistors, Nanotechnology 17 (2006) 1264–1271, https://doi.org/10.1088/0957-4484/17/5/018.

[33] Y. Li, J. Xiang, F. Qian, S. Gradečak, Y. Wu, H. Yan, D.A. Blom, C.M. Lieber, Dopant-free GaN/AlN/AlGaN radial nanowire heterostructures as high electron mobility transistors, Nano Lett. 6 (2006) 1468–1473, https://doi.org/10.1021/nl060849z.

[34] P.J. Harrop, J.N. Wanklyn, The dielectric constant of zirconia, Br. J. Appl. Phys. 18 (1967) 739, https://doi.org/10.1088/0508-3443/18/6/305.

[35] K.V. Cartwright, Derivation of the exact transconductance of a FET without calculus, Technol. Interface J. 10 (2009) 7.

[36] P.T. Blanchard, K.A. Bertness, T.E. Harvey, L.M. Mansfield, A.W. Sanders, N.A. Sanford, MESFETs made from individual GaN nanowires, IEEE Trans. Nanotechnol. 7 (2008) 760–765, https://doi.org/10.1109/TNANO.2008.2005492.

[37] P.R.C. Gascoyne, J. Vykoukal, Particle separation by dielectrophoresis, Electrophoresis 23 (2002) 1973–1983, https://doi.org/10.1002/1522-2683(200207)23:13 < 1973::AID-ELPS1973 > 3.0.CO;2-1.

[38] P.T. Blanchard, K.A. Bertness, T.E. Harvey, A.W. Sanders, N.A. Sanford, S.M. George, D. Seghete, MOSFETs made from GaN nanowires with fully conformal cylindrical gates, IEEE Trans. Nanotechnol. 11 (2012) 479–482, https://doi.org/10.1109/TNANO.2011.2177993.

[39] Ž. Gačević, D. López-Romero, T. Juan Mangas, E. Calleja, A top-gate GaN nanowire metal–semiconductor field effect transistor with improved channel electrostatic control, Appl. Phys. Lett. 108 (2016) 033101, , https://doi.org/10.1063/1.4940197.

[40] W. Li, M.D. Brubaker, B.T. Spann, K.A. Bertness, P. Fay, GaN nanowire MOSFET with near-ideal subthreshold slope, IEEE Electron Device Lett. 39 (2018) 184–187, https://doi.org/10.1109/LED.2017.2785785.

[41] G. Doornbos, M. Passlack, Benchmarking of III–V n-MOSFET maturity and feasibility for future CMOS, IEEE Electron Device Lett. 31 (2010) 1110–1112, https://doi.org/10.1109/LED.2010.2063012.

[42] M. Sun, Y. Zhang, X. Gao, T. Palacios, High-performance GaN vertical fin power transistors on bulk GaN substrates, IEEE Electron Device Lett. 38 (2017) 509–512, https://doi.org/10.1109/LED.2017.2670925.

[43] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, T. Palacios, Large area 1.2 kV GaN vertical power FinFETs with a record switching figure-of-merit, IEEE Electron Device Lett. (2018) 1, https://doi.org/10.1109/LED.2018.2880306.

[44] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, T. Palacios, 1200 V GaN vertical fin power field-effect transistors, 2017 IEEE International Electron Devices Meeting (IEDM), 2017, pp. 9.2.1–9.2.4, , https://doi.org/10.1109/IEDM.2017.8268357.

[45] M. Sun, M. Pan, X. Gao, T. Palacios, Vertical GaN power FET on bulk GaN substrate, 2016 74th Annual Device Research Conference (DRC), 2016, pp. 1–2, , https://doi.org/10.1109/DRC.2016.7548467.

[46] Y. Jo, D. Son, D. Lee, C. Won, J.H. Seo, I.M. Kang, J. Lee, First demonstration of GaN-based vertical nanowire FET with top-down approach, 73rd Ann. Device Res. Conf. (DRC) 2015 (2015) 35–36, https://doi.org/10.1109/DRC.2015.7175539.

[47] F. Yu, D. Rümmler, J. Hartmann, L. Caccamo, T. Schimpke, M. Strassburg, A.E. Gad, A. Bakin, H.-H. Wehmann, B. Witzigmann, H.S. Wasisto, A. Waag, Vertical architecture for enhancement mode power transistors based on GaN nanowires, Appl. Phys. Lett. 108 (2016) 213503, , https://doi.org/10.1063/1.4952715.

[48] F. Yu, S. Yao, F. Römer, B. Witzigmann, T. Schimpke, M. Strassburg, A. Bakin, H.W. Schumacher, E. Peiner, H.S. Wasisto, A. Waag, GaN nanowire arrays with nonpolar sidewalls for vertically integrated field-effect transistors, Nanotechnology 28 (2017) 095206, , https://doi.org/10.1088/1361-6528/aa57b6.

[49] Z. Hu, W. Li, K. Nomoto, M. Zhu, X. Gao, M. Pilla, D. Jena, H.G. Xing, GaN vertical nanowire and fin power MISFETs, Device Research Conference (DRC), 2017 75th Annual, IEEE, 2017, pp. 1–2 http://ieeexplore.ieee.org/abstract/document/7999511/ , Accessed date: 17 August 2017.

[50] A. Chaney, H. Turski, K. Nomoto, Q. Wang, Z. Hu, M. Kim, H.G. Xing, D. Jena, Realization of the first GaN based tunnel field-effect transistor, 2018 76th Device Research Conference (DRC), 2018, pp. 1–3, , https://doi.org/10.1109/DRC.2018.8442249.

[51] D.-H. Son, Y.-W. Jo, J.H. Seo, C.-H. Won, K.-S. Im, Y.S. Lee, H.S. Jang, D.-H. Kim, I.M. Kang, J.-H. Lee, Low voltage operation of GaN vertical nanowire MOSFET, Solid State Electron. 145 (2018) 1–7, https://doi.org/10.1016/j.sse.2018.03.001.

[52] F. Yu, K. Strempel, M.F. Fatahilah, H. Zhou, F. Romer, A. Bakin, B. Witzigmann, H.W. Schumacher, H.S. Wasisto, A. Waag, Normally off vertical 3-D GaN nanowire MOSFETs with inverted p-GaN channel, IEEE Trans. Electron Devices 65 (2018) 2439–2445, https://doi.org/10.1109/TED.2018.2824985.

[53] H. Lu, A. Seabaugh, Tunnel field-effect transistors: state-of-the-art, IEEE J. Electron Devices Soc. 2 (2014) 44–49, https://doi.org/10.1109/JEDS.2014.2326622.

[54] K.A. Bertness, N.A. Sanford, A.V. Davydov, GaN nanowires grown by molecular beam epitaxy, IEEE J. Sel. Top. Quantum Electron. 17 (2011) 847–858, https://doi.org/10.1109/JSTQE.2010.2082504.

[55] V. Consonni, M. Hanke, M. Knelangen, L. Geelhaar, A. Trampert, H. Riechert, Nucleation mechanisms of self-induced GaN nanowires grown on an amorphous interlayer, Phys. Rev. B 83 (2011), https://doi.org/10.1103/PhysRevB.83.035310.

[56] V. Consonni, A. Trampert, L. Geelhaar, H. Riechert, Physical origin of the incubation time of self-induced GaN nanowires, Appl. Phys. Lett. 99 (2011) 033102, , https://doi.org/10.1063/1.3610964.

[57] J. Ristić, E. Calleja, S. Fernández-Garrido, L. Cerutti, A. Trampert, U. Jahn, K.H. Ploog, On the mechanisms of spontaneous growth of III-nitride nanocolumns by plasma-assisted molecular beam epitaxy, J. Cryst. Growth 310 (2008) 4035–4045, https://doi.org/10.1016/j.jcrysgro.2008.05.057.

[58] K.A. Bertness, N.A. Sanford, J.M. Barker, J.B. Schlager, A. Roshko, A.V. Davydov, I. Levin, Catalyst-free growth of GaN nanowires, J. Electron. Mater. 35 (2006) 576–580, https://doi.org/10.1007/s11664-006-0102-4.

[59] R.K. Debnath, R. Meijers, T. Richter, T. Stoica, R. Calarco, H. Lüth, Mechanism of molecular beam epitaxy growth of GaN nanowires on Si(111), Appl. Phys. Lett. 90 (2007) 123117, , https://doi.org/10.1063/1.2715119.

[60] M.A. Sanchez-Garcia, E. Calleja, E. Monroy, F.J. Sanchez, F. Calle, E. Muñoz, R. Beresford, The effect of the III/V ratio and substrate temperature on the morphology and properties of GaN- and AlN-layers grown by molecular beam epitaxy on Si(111), J. Cryst. Growth 183 (1998) 23–30, https://doi.org/10.1016/S0022-0248(97)00386-2.

[61] M. Yoshizawa, A. Kikuchi, M. Mori, N. Fujita, K. Kishino, Growth of self-organized GaN nanostructures on Al2O3(0001) by RF-radical source molecular beam epitaxy, Jpn. J. Appl. Phys. 36 (1997) L459, https://doi.org/10.1143/JJAP.36.L459.

[62] R. Koester, J.S. Hwang, C. Durand, D. Le Si Dang, J. Eymery, Self-assembled growth of catalyst-free GaN wires by metal–organic vapour phase epitaxy, Nanotechnology. 21 (2010) 015602, , https://doi.org/10.1088/0957-4484/21/1/015602.

[63] H. Sekiguchi, K. Kishino, A. Kikuchi, Ti-mask selective-area growth of GaN by RF-plasma-assisted molecular-beam epitaxy for fabricating regularly arranged InGaN/GaN nanocolumns, Appl. Phys. Express 1 (2008) 124002, , https://doi.org/10.1143/APEX.1.124002.

[64] J. Hartmann, F. Steib, H. Zhou, J. Ledig, L. Nicolai, S. Fündling, T. Schimpke, A. Avramescu, T. Varghese, A. Trampert, M. Straßburg, H.-J. Lugauer, H.-H. Wehmann, A. Waag, Study of 3D-growth conditions for selective area MOVPE of high aspect ratio GaN fins with non-polar vertical sidewalls, J. Cryst. Growth 476 (2017) 90–98, https://doi.org/10.1016/j.jcrysgro.2017.08.021.

[65] K. Kishino, T. Hoshino, S. Ishizawa, A. Kikuchi, Selective-area growth of GaN nanocolumns on titanium-mask-patterned silicon (111) substrates by RF-plasma-assisted molecular-beam epitaxy, Electron. Lett. 44 (2008) 819, https://doi.org/10.1049/el:20081323.

[66] A. Bengoechea-Encabo, F. Barbagini, S. Fernandez-Garrido, J. Grandal, J. Ristic, M.A. Sanchez-Garcia, E. Calleja, U. Jahn, E. Luna, A. Trampert, Understanding the selective area growth of GaN nanocolumns by MBE using Ti nanomasks, J. Cryst. Growth 325 (2011) 89–92, https://doi.org/10.1016/j.jcrysgro.2011.04.035.

[67] K. Kishino, H. Sekiguchi, A. Kikuchi, Improved Ti-mask selective-area growth (SAG) by rf-plasma-assisted molecular beam epitaxy demonstrating extremely uniform GaN nanocolumn arrays, J. Cryst. Growth 311 (2009) 2063–2068, https://doi.org/10.1016/j.jcrysgro.2008.11.056.

[68] T. Schumann, T. Gotschke, F. Limbach, T. Stoica, R. Calarco, Selective-area catalyst-free MBE growth of GaN nanowires using a patterned oxide layer, Nanotechnology 22 (2011) 095603, , https://doi.org/10.1088/0957-4484/22/9/095603.

[69] A. Urban, J. Malindretos, J.-H. Klein-Wiele, P. Simon, A. Rizzi, Ga-polar GaN nanocolumn arrays with semipolar faceted tips, New J. Phys. 15 (2013) 053045, , https://doi.org/10.1088/1367-2630/15/5/053045.

[70] S. Li, S. Fündling, Ü. Sökmen, R. Neumann, S. Merzsch, P. Hinze, T. Weimann, U. Jahn, A. Trampert, H. Riechert, E. Peiner, H.-H. Wehmann, A. Waag, GaN nanorods and LED structures grown on patterned Si and AlN/Si substrates by selective area growth, Phys. Status Solidi C 7 (2010) 2224–2226, https://doi.org/10.1002/pssc.200983457.

[71] T.-Y. Tang, W.-Y. Shiao, C.-H. Lin, K.-C. Shen, J.-J. Huang, S.-Y. Ting, T.-C. Liu, C.C. Yang, C.-L. Yao, J.-H. Yeh, T.-C. Hsu, W.-C. Chen, H.-C. Hsu, L.-C. Chen, Coalescence overgrowth of GaN nanocolumns on sapphire with patterned metal organic vapor phase epitaxy, J. Appl. Phys. 105 (2009) 023501, , https://doi.org/10.1063/1.3065527.

[72] S. Haffouz, B. Beaumont, P. Gibart, Effect of magnesium and silicon on the lateral overgrowth of GaN patterned substrates by metal organic vapor phase epitaxy, MRS Int. J. Nitride Semicond. Res. 3 (1998), https://doi.org/10.1557/S1092578300000806.

[73] J. Hartmann, X. Wang, H. Schuhmann, W. Dziony, L. Caccamo, J. Ledig, M.S. Mohajerani, T. Schimpke, M. Bähr, G. Lilienkamp, W. Daum, M. Seibt, M. Straßburg, H.-H. Wehmann, A. Waag, Growth mechanisms of GaN microrods for 3D core-shell LEDs: the influence of silane flow: growth mechanisms of GaN microrods for 3D core-shell LEDs, Phys. Status Solidi A 212 (2015) 2830–2836, https://doi.org/10.1002/pssa.201532316.

[74] W. Song, R. Wang, X. Wang, D. Guo, H. Chen, Y. Zhu, L. Liu, Y. Zhou, Q. Sun, L. Wang, S. Li, *a* -Axis GaN/AlN/AlGaN Core–Shell heterojunction microwires as normally off high Electron mobility transistors, ACS Appl. Mater. Interfaces 9 (2017) 41435–41442, https://doi.org/10.1021/acsami.7b12986.

[75] J. Hartmann, F. Steib, H. Zhou, J. Ledig, S. Fündling, F. Albrecht, T. Schimpke, A. Avramescu, T. Varghese, H.-H. Wehmann, M. Straßburg, H.-J. Lugauer, A. Waag, High aspect ratio GaN Fin microstructures with nonpolar sidewalls by continuous mode metalorganic vapor phase epitaxy, Cryst. Growth Des. 16 (2016) 1458–1462, https://doi.org/10.1021/acs.cgd.5b01598.

[76] D. Paramanik, A. Motayed, G.S. Aluri, J.-Y. Ha, S. Krylyuk, A.V. Davydov, M. King, S. McLaughlin, S. Gupta, H. Cramer, Formation of large-area GaN nanostructures with controlled geometry and morphology using top-down fabrication scheme, J. Vac. Sci. Technol. B Nanotechnol. Microelectron. 30 (2012) 052202, , https://doi.org/10.1116/1.4739424.

[77] C.H. Chiu, T.C. Lu, H.W. Huang, C.F. Lai, C.C. Kao, J.T. Chu, C.C. Yu, H.C. Kuo, S.C. Wang, C.F. Lin, T.H. Hsueh, Fabrication of InGaN/GaN nanorod light-emitting diodes with self-assembled Ni metal islands, Nanotechnology 18 (2007) 445201, , https://doi.org/10.1088/0957-4484/18/44/445201.

[78] Y.D. Wang, S.J. Chua, S. Tripathy, M.S. Sander, P. Chen, C.G. Fonstad, High optical quality GaN nanopillar arrays, Appl. Phys. Lett. 86 (2005) 071917, , https://doi.org/10.1063/1.1861984.

[79] B.J. Kim, H. Jung, H.Y. Kim, J. Bang, J.H. Kim, Fabrication of GaN nanorods by inductively coupled plasma etching via SiO2 nanosphere lithography, Thin Solid Films 517 (2009) 3859–3861, https://doi.org/10.1016/j.tsf.2009.01.144.

[80] M.F. Fatahilah, P. Puranto, F. Yu, J. Langfahl-Klabes, A. Felgner, Z. Li, M. Xu, F. Pohlenz, K. Strempel, E. Peiner, U. Brand, A. Waag, H.S. Wasisto, Traceable nanomechanical metrology of GaN micropillar array, Adv. Eng. Mater. (2018), https://doi.org/10.1002/adem.201800353.

[81] R. Debnath, J.-Y. Ha, B. Wen, D. Paramanik, A. Motayed, M.R. King, A.V. Davydov, Top-down fabrication of large-area GaN micro- and nanopillars, J. Vac. Sci. Technol. B 32 (2014) 021204, , https://doi.org/10.1116/1.4865908.

[82] H.S. Wasisto, K. Huang, S. Merzsch, A. Stranz, A. Waag, E. Peiner, Finite element modeling and experimental proof of NEMS-based silicon pillar resonators for nanoparticle mass sensing applications, Microsyst. Technol. 20 (2014) 571–584, https://doi.org/10.1007/s00542-013-1992-8.

[83] H.S. Wasisto, S. Merzsch, A. Stranz, A. Waag, E. Uhde, T. Salthammer, E. Peiner, Silicon resonant nanopillar sensors for airborne titanium dioxide engineered nanoparticle mass detection, Sensors Actuators B Chem. 189 (2013) 146–156, https://doi.org/10.1016/j.snb.2013.02.053.

[84] R. Cheung, R.J. Reeves, S.A. Brown, E. van der Drift, M. Kamp, Effects of dry processing on the optical properties of GaN, J. Appl. Phys. 88 (2000) 7110–7114, https://doi.org/10.1063/1.1328780.

[85] J. Liu, J. Huang, X. Gong, J. Wang, K. Xu, Y. Qiu, D. Cai, T. Zhou, G. Ren, H. Yang, A practical route towards fabricating GaN nanowire arrays, CrystEngComm. 13 (2011) 5929–5935, https://doi.org/10.1039/C1CE05292F.

[86] K.-S. Im, C.-H. Won, S. Vodapally, R. Caulmilone, S. Cristoloveanu, Y.-T. Kim, J.-H. Lee, Fabrication of normally-off GaN nanowire gate-all-around FET with top-down approach, Appl. Phys. Lett. 109 (2016) 143106, , https://doi.org/10.1063/1.4964268.

[87] Q. Li, J.B. Wright, W.W. Chow, T.S. Luk, I. Brener, L.F. Lester, G.T. Wang, Single-mode GaN nanowire lasers, Opt. Express 20 (2012) 17873–17879, https://doi.org/10.1364/OE.20.017873.

[88] G. Doundoulakis, A. Adikimenakis, A. Stavrinidis, K. Tsagaraki, M. Androulidaki, F. Iacovella, G. Deligeorgis, G. Konstantinidis, A. Georgakilas, Nanofabrication of normally-off GaN vertical nanowire MESFETs, Nanotechnol. (2019), https://doi.org/10.1088/1361-6528/ab13d0.

[89] D. Zhuang, J.H. Edgar, Wet etching of GaN, AlN, and SiC: a review, Mater. Sci. Eng. R. Rep. 48 (2005) 1–46, https://doi.org/10.1016/j.mser.2004.11.002.

[90] M. Elwenspoek, On the mechanism of anisotropic etching of silicon, J. Electrochem. Soc. 140 (1993) 2075–2080, https://doi.org/10.1149/1.2220767.

[91] L. Bahrig, S.G. Hickey, A. Eychmüller, Mesocrystalline materials and the involvement of oriented attachment – a review, CrystEngComm. 16 (2014) 9408–9424, https://doi.org/10.1039/C4CE00882K.

[92] D.P. Woodruff, How does your crystal grow? A commentary on Burton, Cabrera and Frank (1951) 'the growth of crystals and the equilibrium structure of their surfaces', Philos. Trans. A Math. Phys. Eng. Sci. 373 (2015), https://doi.org/10.1098/rsta.2014.0230.

[93] B. Leung, M.-C. Tsai, G. Balakrishnan, C. Li, S.R.J. Brueck, J.J. Figiel, P. Lu, G.T. Wang, Highly anisotropic crystallographic etching for fabrication of high-aspect ratio GaN nanostructures, 18th International Conference on Metal Organic Vapor Phase Epitaxy (IC-MOVPE 2016), San Diego, CA, 2016, p. 45.

[94] D. Li, M. Sumiya, S. Fuke, D. Yang, D. Que, Y. Suzuki, Y. Fukuda, Selective etching of GaN polar surface in potassium hydroxide solution studied by x-ray photoelectron spectroscopy, J. Appl. Phys. 90 (2001) 4219–4223, https://doi.org/10.1063/1.1402966.

[95] Q. Li, K.R. Westlake, M.H. Crawford, S.R. Lee, D.D. Koleske, J.J. Figiel, K.C. Cross, S. Fathololoumi, Z. Mi, G.T. Wang, Optical performance of top-down fabricated InGaN/GaN nanorod light emitting diode arrays, Opt. Express 19 (2011) 25528–25534, https://doi.org/10.1364/OE.19.025528.

[96] M. Ruzzarin, M. Meneghini, D. Bisi, M. Sun, T. Palacios, G. Meneghesso, E. Zanoni, Instability of dynamic- Ron and threshold voltage in GaN-on-GaN vertical field-effect transistors, IEEE Trans. Electron Devices. 64 (2017) 3126–3131, https://doi.org/10.1109/TED.2017.2716982.

[97] K. Tomioka, M. Yoshimura, T. Fukui, A III–V nanowire channel on silicon for high-performance vertical transistors, Nature 488 (2012) 189–192, https://doi.org/10.1038/nature11293.

[98] K.-S. Im, J.H. Seo, Y.J. Yoon, Y.I. Jang, J.S. Kim, S. Cho, J.-H. Lee, S. Cristoloveanu, J.-H. Lee, I.M. Kang, GaN junctionless trigate field-effect transistor with deep-submicron gate length: characterization and modeling in RF

regime, Jpn. J. Appl. Phys. 53 (2014) 118001, , https://doi.org/10.7567/JJAP.53.118001.
[99] Y.-W. Jo, D.-H. Son, C.-H. Won, K.-S. Im, J.H. Seo, I.M. Kang, J.-H. Lee, AlGaN/GaN FinFET with extremely broad transconductance by side-wall wet etch, IEEE Electron Device Lett. 36 (2015) 1008–1010, https://doi.org/10.1109/LED.2015.2466096.
[100] K. Zhang, Y. Kong, G. Zhu, J. Zhou, X. Yu, C. Kong, Z. Li, T. Chen, High-linearity AlGaN/GaN FinFETs for microwave power applications, IEEE Electron Device Lett. 38 (2017) 615–618, https://doi.org/10.1109/LED.2017.2687440.
[101] G. Sabui, V.Z. Zubialevich, P. Pampili, M. White, P.J. Parbrook, M. McLaren, M. Arredondo-Arechavala, Z.J. Shen, (Invited) Simulation study of high voltage vertical GaN nanowire field effect transistors, ECS Trans. 80 (2017) 69–85, https://doi.org/10.1149/08007.0069ecst.
[102] A. Lidow, J. Strydom, M.D. Rooij, D. Reusch, GaN technology overview, GaN Transistors for Efficient Power Conversion, John Wiley & Sons, Ltd, 2014, pp. 1–18, , https://doi.org/10.1002/9781118844779.ch1.
[103] Y. Zhang, A. Dadgar, T. Palacios, Gallium nitride vertical power devices on foreign substrates: a review and outlook, J. Phys. D. Appl. Phys. 51 (2018) 273001, , https://doi.org/10.1088/1361-6463/aac8aa.
[104] S. Arulkumaran, G.I. Ng, C.M. Manojkumar, K. Ranjan, K.L. Teo, O.F. Shoron, S. Rajan, S.B. Dolmanan, S. Tripathy, In0.17Al0.83N/AlN/GaN Triple T-shape Fin-HEMTs with gm = 646 mS/mm, ION = 1.03 A/mm, IOFF = 1.13 μA/mm, SS = 82 mV/dec and DIBL = 28 mV/V at VD = 0.5 V, 2014 IEEE International Electron Devices Meeting, IEEE, San Francisco, CA, USA, 2014, pp. 25.6.1–25.6.4, , https://doi.org/10.1109/IEDM.2014.7047109.
[105] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, K. Boutros, 1200-V normally off GaN-on-Si field-effect transistors with low dynamic on -resistance, IEEE Electron Device Lett. 32 (2011) 632–634, https://doi.org/10.1109/LED.2011.2118190.
[106] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M.V. Hove, M. Germain, G. Borghs, Low on-resistance high-breakdown normally off AlN/GaN/AlGaN DHFET on Si substrate, IEEE Electron Device Lett. 31 (2010) 111–113, https://doi.org/10.1109/LED.2009.2037719.
[107] I. Hwang, H. Choi, J. Lee, H.S. Choi, J. Kim, J. Ha, C. Um, S. Hwang, J. Oh, J. Kim, J.K. Shin, Y. Park, U. Chung, I. Yoo, K. Kim, 1.6kV, 2.9 mΩ.cm^2 normally-off p-GaN HEMT device, 2012 24th International Symposium on Power Semiconductor Devices and ICs, 2012, pp. 41–44, , https://doi.org/10.1109/ISPSD.2012.6229018.
[108] N. Ikeda, R. Tamura, T. Kokawa, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, Over 1.7 kV normally-off GaN hybrid MOS-HFETs with a lower on-resistance on a Si substrate, 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, 2011, pp. 284–287, , https://doi.org/10.1109/ISPSD.2011.5890846.
[109] K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto, H. Shimawaki, A normally-off GaN FET with high threshold voltage uniformity using a novel piezo neutralization technique, 2009 IEEE International Electron Devices Meeting (IEDM), 2009, pp. 1–4, , https://doi.org/10.1109/IEDM.2009.5424398.
[110] M. Ishida, T. Ueda, T. Tanaka, D. Ueda, GaN on Si technologies for power switching devices, IEEE Trans. Electron Devices 60 (2013) 3053–3059, https://doi.org/10.1109/TED.2013.2268577.
[111] Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang, K.J. Chen, 600-V normally off SiN/AlGaN/GaN MIS-HEMT with large gate swing and low current collapse, IEEE Electron Device Lett. 34 (2013) 1373–1375, https://doi.org/10.1109/LED.2013.2279846.
[112] M. Wang, Y. Wang, C. Zhang, C.P. Wen, J. Wang, Y. Hao, W. Wu, B. Shen, K.J. Chen, Normally-off hybrid Al2O3/GaN MOSFET on silicon substrate based on wet-etching, 2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD), 2014, pp. 253–256, , https://doi.org/10.1109/ISPSD.2014.6856024.
[113] Qi Zhou, Bowen Chen, Yang Jin, Sen Huang, Ke Wei, Xinyu Liu, Xu Bao, Jinyu Mou, Bo Zhang, High-performance enhancement-mode Al_2O_3/AlGaN/GaN-on-Si MISFETs with 626 MW/cm^2 figure of merit, IEEE Trans. Electron Devices 62 (2015) 776–781, https://doi.org/10.1109/TED.2014.2385062.
[114] H. Nie, Q. Diduck, B. Alvarez, A.P. Edwards, B.M. Kayes, M. Zhang, G. Ye, T. Prunty, D. Bour, I.C. Kizilyalli, 1.5-kV and 2.2-mΩ.cm^2 vertical GaN transistors on bulk-GaN substrates, IEEE Electron Device Lett. 35 (2014) 939–941, https://doi.org/10.1109/LED.2014.2339197.
[115] T. Oka, T. Ina, Y. Ueno, J. Nishii, 1.8 mΩ·cm^2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation, Appl. Phys. Express 8 (2015) 054101, , https://doi.org/10.7567/APEX.8.054101.
[116] D. Ji, S. Chowdhury, Design of 1.2 kV power switches with low R_{ON} using GaN-based vertical JFET, IEEE Trans. Electron Devices 62 (2015) 2571–2578, https://doi.org/10.1109/TED.2015.2446954.
[117] B.J. Baliga, Gallium nitride devices for power electronic applications, Semicond. Sci. Technol. 28 (2013) 074011, , https://doi.org/10.1088/0268-1242/28/7/074011.
[118] B.J. Baliga, Power semiconductor device figure of merit for high-frequency applications, IEEE Electron Device Lett 10 (1989) 455–457, https://doi.org/10.1109/55.43098.
[119] W. Li, K. Nomoto, K. Lee, S. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, H.G. Xing, Development of GaN vertical trench-MOSFET with MBE regrown channel, IEEE Trans. Electron Devices 65 (2018) 2558–2564, https://doi.org/10.1109/TED.2018.2829125.
[120] Y. Cheng, M.-C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P.K. Ko, C. Hu, A physical and scalable – model in BSIM3v3 for analog/digital circuit simulation, IEEE Trans. on Electron Devices 44 (1997) 11.
[121] S. Vodapally, C.G. Theodorou, Y. Bae, G. Ghibaudo, S. Cristoloveanu, K.-S. Im, J.-H. Lee, Comparison for 1/ f noise characteristics of AlGaN/GaN FinFET and planar MISHFET, IEEE Trans. Electron Devices 64 (2017) 3634–3638, https://doi.org/10.1109/TED.2017.2730919.
[122] S. Vodapally, Y.I. Jang, I.M. Kang, I.-T. Cho, J.-H. Lee, Y. Bae, G. Ghibaudo, S. Cristoloveanu, K.-S. Im, J.-H. Lee, 1/f-noise in AlGaN/GaN nanowire omega-FinFETs, IEEE Electron Device Lett. 38 (2017) 252–254, https://doi.org/10.1109/LED.2016.2645211.
[123] V. Sindhuri, D.-H. Son, D.-G. Lee, S. Sakong, Y.-H. Jeong, I.-T. Cho, J.-H. Lee, Y.-T. Kim, S. Cristoloveanu, Y. Bae, K.-S. Im, J.-H. Lee, 1/f noise characteristics of AlGaN/GaN FinFETs with and without TMAH surface treatment, Microelectron. Eng. 147 (2015) 134–136, https://doi.org/10.1016/j.mee.2015.04.023.
[124] M. Ruzzarin, M. Meneghini, C. De Santi, G. Meneghesso, E. Zanoni, M. Sun, T. Palacios, Degradation of vertical GaN FETs under gate and drain stress, 2018 IEEE International Reliability Physics Symposium (IRPS), IEEE, Burlingame, CA, 2018, , https://doi.org/10.1109/IRPS.2018.8353579 4B.1-1–4B.1-5.
[125] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K.J. Chen, B. Zhang, Enhancement-mode operation of nanochannel array (NCA) AlGaN/GaN HEMTs, IEEE Electron Device Lett. 33 (2012) 354–356, https://doi.org/10.1109/LED.2011.2179003.
[126] N. Kaushik, D.M.A. Mackenzie, K. Thakar, N. Goyal, B. Mukherjee, P. Boggild, D.H. Petersen, S. Lodha, Reversible hysteresis inversion in MoS2 field effect transistors, Npj 2D Mater. Appl. 1 (2017), https://doi.org/10.1038/s41699-017-0038-y.
[127] N.R. Brinkmann, G.S. Tschumper, H.F. Schaefer, Electron affinities of the oxides of aluminum, silicon, phosphorus, sulfur, and chlorine, J. Chem. Phys. 110 (1999) 6240–6245, https://doi.org/10.1063/1.478528.
[128] J.P. Fitts, X. Shang, G.W. Flynn, T.F. Heinz, K.B. Eisenthal, Electrostatic surface charge at aqueous/α-Al_2O_3 single-crystal interfaces as probed by optical second-harmonic generation, J. Phys. Chem. B 109 (2005) 7981–7986, https://doi.org/10.1021/jp040297d.
[129] J. Kuzmik, R. Javorka, A. Alam, M. Marso, M. Heuken, P. Kordos, Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method, IEEE Trans. Electron Devices 49 (2002) 1496–1498, https://doi.org/10.1109/TED.2002.801430.
[130] Y. Avenas, L. Dupont, Z. Khatir, Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters – a review, IEEE Trans. Power Electron. 27 (2012) 3081–3092, https://doi.org/10.1109/TPEL.2011.2178433.
[131] B. Chervonni, O. Aktushev, E. Ojalvo, Y. Knafo, Y. Turkulets, I. Shalish, Fast estimation of channel temperature in GaN high electron mobility transistor under RF operating conditions, Semicond. Sci. Technol. 33 (2018) 095024, , https://doi.org/10.1088/1361-6641/aad539.
[132] J.D. Albrecht, R.P. Wang, P.P. Ruden, M. Farahmand, K.F. Brennan, Electron transport characteristics of GaN for high temperature device modeling, J. Appl. Phys. 83 (1998) 4777–4781, https://doi.org/10.1063/1.367269.
[133] J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, P. Fay, High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination, Appl. Phys. Lett. 113 (2018) 023502, , https://doi.org/10.1063/1.5035267.
[134] S. Yang, S. Liu, C. Liu, Z. Tang, Y. Lu, K.J. Chen, Thermally induced threshold voltage instability of III-nitride MIS-HEMTs and MOSC-HEMTs: underlying mechanisms and optimization schemes, 2014 IEEE International Electron Devices Meeting, IEEE, San Francisco, CA, USA, 2014, pp. 17.2.1–17.2.4, , https://doi.org/10.1109/IEDM.2014.7047069.
[135] J. Ma, E. Matioli, Improved electrical and thermal performances in nanostructured GaN devices, 2016 International Conference on IC Design and Technology (ICICDT), IEEE, Ho Chi Minh City, 2016, pp. 1–4, , https://doi.org/10.1109/ICICDT.2016.7542061.
[136] R. Gaska, J. Yang, A. Osinsky, M.A. Khan, M.S. Shur, Novel high power AlGaN/GaN HFETs on SiC substrates, International Electron Devices Meeting, IEDM Technical Digest, 1997, pp. 565–568, , https://doi.org/10.1109/IEDM.1997.650449.
[137] M.J. Tadjer, T.J. Anderson, J.C. Gallagher, P.E. Raad, P. Komarov, A.D. Koehler, K.D. Hobart, F.J. Kub, Thermal performance improvement of GaN-on-diamond high electron mobility transistors, 2018 76th Device Research Conference (DRC), IEEE, Santa Barbara, CA, USA, 2018, pp. 1–2, , https://doi.org/10.1109/DRC.2018.8442138.
[138] J. Ma, E. Matioli, Slanted tri-gates for high-voltage GaN power devices, IEEE Electron Device Lett. 38 (2017) 1305–1308, https://doi.org/10.1109/LED.2017.2731799.
[139] K.-S. Im, G. Atmaca, C.-H. Won, R. Caulmilone, S. Cristoloveanu, Y.-T. Kim, J.-H. Lee, Current collapse-free and self-heating performances in normally off GaN nanowire GAA-MOSFETs, IEEE J. Electron Devices Soc. 6 (2018) 354–359, https://doi.org/10.1109/JEDS.2018.2806930.
[140] H. Kamrani, F. Yu, K. Frank, K. Strempel, M.F. Fatahilah, H.S. Wasisto, F. Römer, A. Waag, B. Witzigmann, Thermal performance analysis of GaN nanowire and fin-shaped power transistors based on self-consistent electrothermal simulations, Microelectron. Reliab. 91 (2018) 227–231, https://doi.org/10.1016/j.microrel.2018.10.007.
[141] D.S. Lee, H. Wang, A. Hsu, M. Azize, O. Laboutin, Y. Cao, J.W. Johnson, E. Beam, A. Ketterson, M.L. Schuette, P. Saunier, T. Palacios, Nanowire channel InAlN/GaN HEMTs with high linearity of g_m and f_T, IEEE Electron Device Lett. 34 (2013) 969–971, https://doi.org/10.1109/LED.2013.2261913.
[142] D.S. Lee, H. Wang, A. Hsu, M. Azize, O. Laboutin, Y. Cao, W. Johnson, E. Beam, A. Ketterson, M. Schuette, P. Saunier, High linearity nanowire channel GaN

HEMTs, Device Research Conference (DRC), 2013 71st Annual, IEEE, 2013, pp. 195–196 http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6633860 , Accessed date: 20 October 2016.
[143] T. Fang, R. Wang, H. Xing, S. Rajan, D. Jena, Effect of optical phonon scattering on the performance of GaN transistors, IEEE Electron Device Lett. 33 (2012) 709–711, https://doi.org/10.1109/LED.2012.2187169.
[144] Jie Liu, Y. Zhou, R. Chu, Y. Cai, K.J. Chen, K.M. Lau, Highly linear Al/sub 0.3/Ga/sub 0.7/N-Al/sub 0.05/Ga/sub 0.95/N-GaN composite-channel HEMTs, IEEE Electron Device Lett 26 (2005) 145–147, https://doi.org/10.1109/LED.2005.843218.
[145] T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, U.K. Mishra, Influence of the dynamic access resistance in the g_m and f_{-T} linearity of AlGaN/GaN HEMTs, IEEE Trans. Electron Devices. 52 (2005) 2117–2123, https://doi.org/10.1109/TED.2005.856180.
[146] D.W. DiSanto, C.R. Bolognesi, At-bias extraction of access parasitic resistances in AlGaN/GaN HEMTs: impact on device linearity and channel electron velocity, IEEE Trans. Electron Devices. 53 (2006) 2914–2919, https://doi.org/10.1109/TED.2006.885663.
[147] R.J. Trew, Yueying Liu, L. Bilbro, Weiwei Kuang, R. Vetury, J.B. Shealy, Nonlinear source resistance in high-voltage microwave AlGaN/GaN HFETs, IEEE Trans. Microw. Theory Tech. 54 (2006) 2061–2067, https://doi.org/10.1109/TMTT.2006.873627.
[148] K. Shinohara, C. King, A.D. Carter, E.J. Regan, A. Arias, J. Bergman, M. Urteaga, B. Brar, GaN-based field-effect transistors with laterally gated two-dimensional electron gas, IEEE Electron Device Lett. 39 (2018) 417–420, https://doi.org/10.1109/LED.2018.2797940.
[149] T.-T. Liu, K. Zhang, G.-R. Zhu, J.-J. Zhou, Y.-C. Kong, X.-X. Yu, T.-S. Chen, Influence of fin architectures on linearity characteristics of AlGaN/GaNFinFETs, Chinese Physics B. 27 (2018) 047307, , https://doi.org/10.1088/1674-1056/27/4/047307.
[150] S. Joglekar, U. Radhakrishna, D. Piedra, D. Antoniadis, T. Palacios, Large signal linearity enhancement of AlGaN/GaN high electron mobility transistors by device-level Vt engineering for transconductance compensation, 2017 IEEE International Electron Devices Meeting (IEDM), IEEE, San Francisco, CA, 2017, pp. 25.3.1–25.3.4, , https://doi.org/10.1109/IEDM.2017.8268457.

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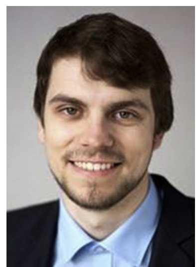

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