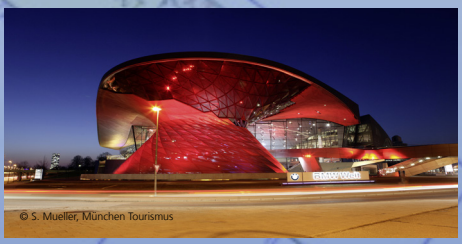
17TH IEEE INTERNATIONAL NEWCAS CONFERENCE

NEWCAS 2019

June 23 - 26

Munich, Germany



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Dr ès sc. Erkan Isa

IEEE NEWCAS2019
General Co-Chair

Professor Mohamad Sawan

IEEE NEWCAS2019
General Co-Chair

On behalf of the Organizing Committee and Fraunhofer EMFT, we are happy to welcome you in Munich, the capital of Bavaria, for the 17th International IEEE NEWCAS Conference. We created an excellent program this year, including superb tutorials, outstanding keynote talks, technical sessions and wonderful social and networking events.

Conference highlights include:

Tutorials (Sunday, June 23th):

- Systematic design of low-power Analog/RF CMOS circuits using the Inversion Coefficient
  by Prof. Christian Enz (EPFL), Prof. Willy Sansen (KU Leuven) and Prof. Thierry Taris (University of Bordeaux)
- Spread-spectrum techniques for mitigation of inband jammers in RF transceivers
  by Prof. Ramesh Harjani, University of Minnesota
- An Efficient Solution to Simulate Mixed-Signal Circuits in C
  by Prof. Yves Leduc, Associate member, Polytech Lab, University of Nice Sophia-Antipolis

- Amplifier Efficiency vs Linearity: what physics does and does not allow?
  by Prof. Dr. Earl McCune, TU Delft
- Things you always wanted to know about the bioelectricity of living cells and their marriage with electronics – but never dared to study
  by Prof. Dr. Joachim Wegener, Fraunhofer EMFT, Prof. Dr. Sven Ingebrandt, RWTH Aachen
- Design and mitigation methodologies of COTS FPGAs for Aerospace Missions
  by Assoc. Prof. Luca Sterpone, Politecnico di Torino

Keynotes (Monday, June 24th to Wednesday, June 26th):

- Quantum Computing: From Curiosity to First Useful Applications
  by Dr. Alessandro Curioni, Vice President Europe and Director IBM Research, Zurich, Switzerland
- Mixed-Signal Techniques for Embedded Machine Learning Systems
  by Professor Boris Murmann, Stanford University, USA
- Tiny AI – How sensors become truly smart
  by Wolfgang Furtner, Infineon, Munich, Germany
- Kalray's MPPA® Manycore Processor: At the Heart of Intelligent Systems
  by Dr. Benoît Dupont de Dinechin, CTO Kalray

Special session "SOI Ecosystem for 5G" (Monday, June 24th):

- Opening Keynote: 5G Ecosystems
  by Dr. Carlos Mazure, SOI Consortium Executive Director & EVP Soitec
- Foundry Vision: 5G Ecoystem in Europe and Beyond: The Globalfoundries Perspective
  by Dr. Gary Patton, Globalfoundries CTO and SVP, Design Enablement and R&D
- End-User: Airbus vision
  by Dr. Dominic Schupke, Airbus Wireless Communications

Technical Program (June 24th to 26th): 14 regular and 4 special technical sessions consisting of lecture presentations (2 parallel sessions each day) and one poster and demonstrator session on Tuesday.

Social and Networking Events (June 24th to 26th): With the social program, we invite you to get in touch with the Bavarian way of life: Join our Welcome Event at the famous Munich Hofbräuhaus, right in the heart of Munich city center. On Tuesday, we will enjoy a Networking Event where academia and industry will find an excellent opportunity to exchange ideas and foster the future collaboration based on solid scientific results.

This year, a total of 193 technical papers were submitted to NEWCAS from 36 countries in Europe, America, Africa and Asia. The technical program committee members solicited and received 707 expert reviews (average of 3,6 reviews per paper) in a timely manner. We would like to warmly thank the Technical Program Committee members and all the reviewers, consisting of 251 individuals in total. We apologize in advance that we cannot list all of the involved persons.

Out of the submitted papers we selected, 82 regular papers resulting in the acceptance rate of 46,3% for the regular submissions. We rounded up the program by accepting 16 paper contributions in 4 focused special sessions: 5G, SOI based RF and mm-wave design, EDA and security of systems. The special sessions also incorporate for the sake of completeness, four invited leading industrial presentations of the state of the art in the research fields, showing the both sides of the coin: academia and industry. Continuing the tradition from the NEWCAS 2018, this year, the technical committee will select the very few top quality papers and invite their authors to submit an extended version of their work to the special issue of IEEE Transactions on Circuits and Systems I journal.

Finally, we would like to give our sincere thanks for their contribution to the Organizing Committee, the Technical Program Committee, the Keynote- and Tutorials-speakers, the Session Chairs, the reviewers and all authors who will share their scientific work. NEWCAS 2019 would not have been possible without the time and effort of many people. In that respect, NEWCAS, since its creation 17 years ago, serves as a bond among many existing and new members of this community, enabling exchange of scientific ideas and allowing us to meet and discuss the novel developments once in a year with a fresh start. Special thanks goes to our sponsors for making this event possible with their generous contributions; they are all acknowledged in the program.

Enjoy NEWCAS 2019 conference and your stay in Munich, Bavaria!

General Co-Chairs

Dr ès sc. Erkan Isa, Fraunhofer EMFT, Germany
Prof. Mohamad Sawan, Westlake University, China

Welcome Reception Sponsor

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The Fraunhofer-Gesellschaft is the leading organization for applied research in Europe. Its research activities are conducted by 72 institutes and research units at locations throughout Germany. The Fraunhofer-Gesellschaft employs a staff of more than 26,600, who work with an annual research budget totaling 2.6 billion euros.

Fraunhofer EMFT conducts cutting-edge applied research on sensors and actuators for people and the environment. The over hundred employees in the three locations in Munich, Oberpfaffenhofen and Regensburg possess impressive long-term experience and wide-ranging know-how in the fields of **microelectronics and microsystem technology**. Fraunhofer EMFT is equipped with extensive technological facilities in these areas, including e.g. semiconductor technology, development of low-noise components, foil electronics, thin silicon, **IC design and system integration**.

One research focus at Fraunhofer EMFT is **innovative sensor solutions** that can be individually tailored to our customers' needs and requirements. With their broad technological expertise, Fraunhofer EMFT scientists develop novel, high-performance sensors, design robust, secure and fast sensor networks and create system solutions that enable the sensors to interact perfectly with their environment. In this area, in-house developments are sometimes combined with existing solutions.

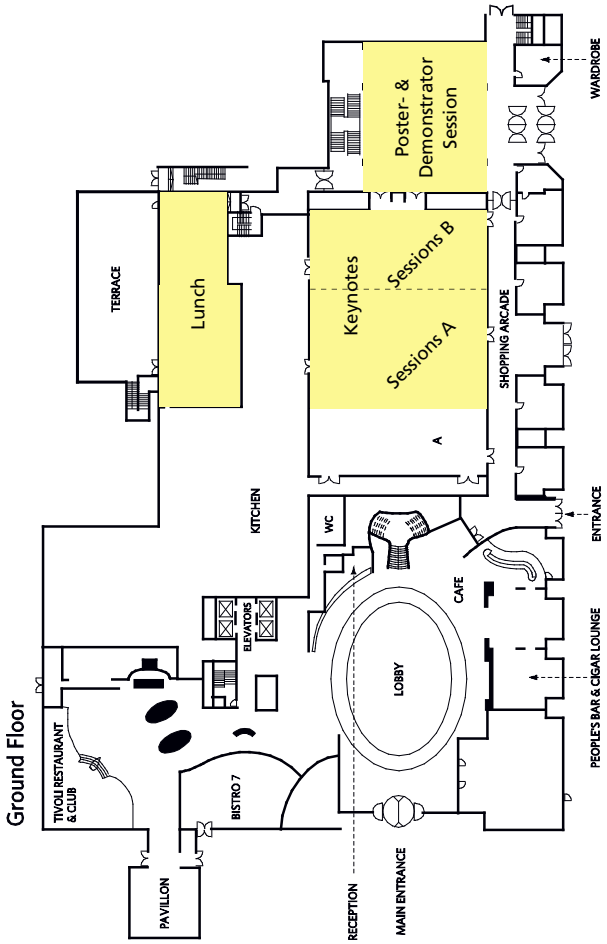
Precise **micro dosage of gases and liquids** to the nearest nanoliter is a central and longstanding area of expertise at Fraunhofer EMFT, covering a broad range of applications – from medical technology through to industrial applications and consumer electronics. Piezo-electrically powered micro-pumps are at the heart of these micro dosing systems. The Fraunhofer EMFT team possesses extensive expertise and practical experience in the design of microdosing systems with MEMS actuators and driver ASICs. On this basis, it is possible to adapt the technological parameters in terms of dosage precision, counter-pressure resistance, size, energy consumption, particle resistance, bubble tolerance and free-flow protection to the requirements in question.

Safe and secure electronic systems are essential to sensitive applications in areas such as medical technology, the automotive industry and aerospace technology. In its R&D activities, Fraunhofer EMFT pursues the goal of enabling so-called zero-defect systems. Focus areas here include failure analyses and characterization of electronic modules and systems, development of novel ESD test and protection concepts and the monitoring of electrical connections using "intelligent" plugs. For protection of electronic systems from manipulation and unwanted access software-base solutions are often no longer sufficient. Fraunhofer EMFT collaborates with partners and customers on novel concepts for hardware security, e.g. based on Physical Unclonable Functions.

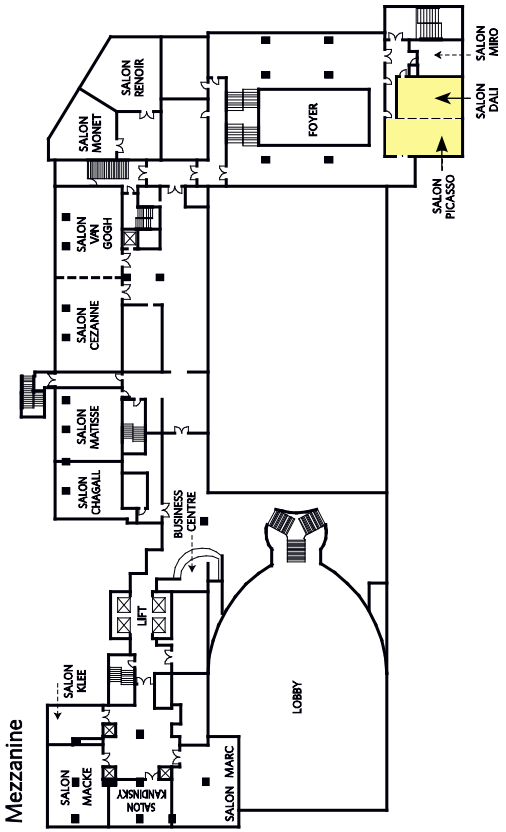
Interdisciplinary collaboration and a wide-ranging partner network are key factors in terms of our strategy of gearing Fraunhofer EMFT more towards all-inclusive solutions than single technologies. The capacity to look beyond a narrow context and integrate a variety of perspectives has repeatedly enabled us to arrive at innovative yet practically feasible solutions.

Local Organizer

Hilton Munich Park Hotel, Ground Floor



Hilton Munich Park Hotel, Mezzanine Floor



TUTORIALS

Fraunhofer EMFT, Hansastrasse 27c, 80686 Munich
You can find the registration desk and the meeting rooms on the 2nd floor. The registration desk is open:

Sunday, June 23	8:30 - 17:30

You must wear your badge at all times to identify yourself and gain access to the booked sessions.

Every room is equipped with a computer and a projector. Should you need any technical assistance, please contact the registration desk prior to your presentation.

CONFERENCE

Hilton Munich Park Hotel, Am Tucherpark 7, 80538 Munich
REGISTRATION DESK in the conference break area, as signposted by the Hilton:

Monday, June 24	08:00 - 15:30
Tuesday, June 25	08:00 - 15:30
Wednesday, June 26	08:00 - 15:30

You must wear your conference badge at all times to identify yourself and gain access to the booked sessions and events.There are no seat reservations, it is first come, first served policy, exceptions will be made only for handicapped participants in wheelchairs.

SPEAKER INFORMATION

Please find detailed instructions for presentations on the conference webpage in terms of duration, contact with session chair, preparation such as presentation slides, upload, technical support and equipment.

POSTER SESSIONS INFORMATION

The placement of your poster (1 panel side, sized DinA0 = 841mm (width) x 1189mm (high)) will be marked on the panel with your paper or demonstrator number as stated in the conference program. Please stay nearby your poster during the session to answer the questions and/or discuss with interested attendees. Place your poster (one big or several smaller ones) during the break before the session, you have to remove it after the session! The posters not removed will be discarded.

WELCOME EVENT – June 24th

Hofbräuhaus, Am Platzl 9, 80331 Munich, subsequent to the conference until 22:00

We provide bus transport to the restaurant for registered participants subsequent to the conference. Pick up place is the conference break area right after the sessions, follow the instructions of the organisers at the front desk. On-site choose your place for the seated dinner - individual walk back to the hotel (ca. 20 minutes).

NETWORKING RECEPTION – June 25th

Hilton Munich Park, Am Tucherpark 7, 80538 Munich, subsequent to the conference until 21:30.

Stand-up reception with snacks and beverages in the conference break area right after the sessions.

General Information

The IEEE NEWCAS2019 organizing committee extends its warmest thanks to the following organizations for their generous contributions and efforts:

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- Benoit Gosselin, Université Laval, Canada

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- Benoit Gosselin, Laval University, Canada

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Track Chair: Jean-Baptiste Begueret, University of Bordeaux, France

Track 2: Digital and mixed-signal circuit design

Track Chair: Thomas Ussmüller, Universität Innsbruck, Institut für Mechatronik, Austria

Track 3: CAD and design tools

Track Chair: Yves Leduc, Assoc. Member, Polytech Lab of University of Nice Sophia-Antipolis, France

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Track Chair: Yvon Savaria, Polytechnique Montréal, Canada

Track 5: Microsystems, sensors and actuators

Track Chair: Shuenn-Yuh Lee, National Cheng Kung University, Taiwan

Track 6: Imaging and image sensors

Track Chair: Takashi Tokuda, Nara Institute of Science and Technology (NAIST), Japan

Track 7: Test and verification

Track Chair: Horst Gieser, Fraunhofer EMFT, Germany

Track 8: Biomedical circuits and systems

Track Chair: Franck Badets, CEA-Leti, France

Track 9: Communication, microwaves and RF

Track Chair: Frederic Nabki, École de technologie supérieure, Canada

Track 10: Device modeling

Track Chair: Martin Claus, Infineon Technologies AG, Germany

Track 11: Data and signal processing

Track Chair: Daniel Massicotte, Université du Québec à Trois-Rivières, Canada

Track 12: Energy harvesting/scavenging and power management

Track Chair: Frank Vanselow, Fraunhofer EMFT, Germany

Track 13: Low-power and low-voltage design techniques

Track Chair: Harald Pretl, Johannes Kepler University & Intel, Austria

Track 14: Neural networks and neuromorphic circuits

Track Co-Chair: Jean Pierre David, Polytechnique Montréal, Canada

Track Co-Chair: Amey Kulkarni, NVIDIA, USA

Track 15: Computer architectures and memories

Track Chair: Tinoosh Mohsenin, University of Maryland, Baltimore County, USA

Track 16: Emerging technologies

Track Chair: Jean-Michel Sallese, École polytechnique fédérale de Lausanne, Switzerland

Track 17: Special sessions

Track Co-Chair: Didier Belot, CEA-Leti, France

Track Co-Chair: Oliver Bringmann, Eberhard Karls University of Tübingen, Germany

Technical Program Committee

Keynote 1

Dr. Alessandro Curioni

Vice President Europe and Director IBM Research, Zurich, Switzerland

Monday, June 24th
9:00 am - 10:00 am

Room A + B

Chair: Prof. Linus Maurer, Fraunhofer EMFT, Germany

Quantum Computing: From Curiosity to First Useful Applications

Abstract: There's no denying it – we're approaching the dawn of the commercial quantum era – a formative period when quantum computing and its early use cases rapidly develop as we go from becoming quantum ready to the ultimate goal of quantum advantage. While quantum computing is still in its infancy, developers, scientists, academics, and professionals are already exploring how quantum computing may address today's unsolvable problems in industries such as financial services, automotive and chemistry. This presentation will share the status of the research and highlight some early success.

Alessandro Curioni is an IBM Fellow, Vice President of IBM Europe and director of the IBM Research Lab in Zurich, Switzerland. He was also recently appointed as the Watson IoT Research Relationship Executive.

Dr. Curioni is an internationally recognized leader in the area of high-performance computing and computational science, where his innovative thinking and seminal contributions have helped solve some of the most complex scientific and technological problems in healthcare, aerospace, consumer goods and electronics. He was a member of the winning team recognized with the prestigious Gordon Bell Prize in 2013 and 2015.

Dr. Curioni received his undergraduate degree in Theoretical Chemistry and his PhD from Scuola Normale Superiore, Pisa, Italy. He started at IBM Research – Zurich as a PhD student in 1993 before officially joining as a research staff member in 1998. His most recent position was Head of the Cognitive Computing and Computational Sciences department.

Keynote Speakers

Keynote 2

Professor Boris Murmann
Stanford University, USA

Tuesday, June 25th
9:00 am - 10:00 am

Room A + B
Chair: Prof. Mohamad Sawan, Westlake University, China

Mixed-Signal Techniques for Embedded Machine Learning Systems

Abstract: Over the past decade, machine learning algorithms have been deployed in many cloud-centric applications such as speech recognition, face identification, and photo search. As this rise of machine learning applications continues, it is clear that some of these algorithms must move "closer to the sensor," thereby eliminating the latency of cloud access and providing a scalable solution that avoids the large energy cost per bit transmission through the network. In this talk, we will discuss mixed-signal techniques for the design of moderate-complexity, low-power inference algorithms. Specific examples include energy-efficient feature extraction for image and audio processing and custom mixed-signal convolutional neural networks.

Boris Murmann is a Professor of Electrical Engineering at Stanford University.

He joined Stanford in 2004 after completing his Ph.D. degree in electrical engineering at the University of California, Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Since 2004, he has worked as a consultant with numerous Silicon Valley companies.

Dr. Murmann's research interests are in mixed-signal integrated circuit design, with special emphasis on sensor interfaces, data converters and custom circuits for embedded machine learning. In 2008, he was a co-recipient of the Best Student Paper Award at the VLSI Circuits Symposium and a recipient of the Best Invited Paper Award at the IEEE Custom Integrated Circuits Conference (CICC). He received the Agilent Early Career Professor Award in 2009 and the Friedrich Wilhelm Bessel Research Award in 2012.

He has served as an Associate Editor of the IEEE Journal of Solid-State Circuits, an AdCom member and Distinguished Lecturer of the IEEE Solid-State Circuits Society, as well as the Data Converter Subcommittee Chair and the Technical Program Chair of the IEEE International Solid-State Circuits Conference (ISSCC). He is the founding faculty co-director of the Stanford SystemX Alliance and the faculty director of Stanford's System Prototyping Facility (SPF). He is a Fellow of the IEEE.

Keynote Speakers

Keynote 3

Wolfgang Furtner
Infineon AG, Munich, Germany

Tuesday, June 25th
10:00 am - 11:00 am

Room A + B
Chair: Prof. Mohamad Sawan, Westlake University, China

Tiny AI – how sensors become truly smart

Abstract: Artificial Intelligence and Machine learning enable numerous new use cases for sensors. Many of today's smart solutions depend on cloud intelligence. For making sensors ubiquitous some amount of local intelligence is required. But how do we make AI available for small embedded systems?

This talk gives on overview about sensor technology beyond audio and vision and the related Machine Learning techniques. It outlines how ML algorithms are optimized for embedded architectures. Low power inference methods and architectures are discussed and an outlook to new neural acceleration technology is provided.

Wolfgang Furtner studied electrical engineering / data processing technology at the Polytechnical University Munich, Germany.

Since 1995 he worked at Philips Semiconductors (now NXP) architecting graphics processing units (GPUs) and flat TV processors.

Since 2006 he is with Infineon as a system architect form embedded computing. He holds the technical lead position of a senior principal for concept and system engineering.

His area of work includes embedded architectures for artificial intelligence and machine learning, in particular focusing on edge computing and smart sensors.

He is active in international standardization (IEC, Mipi) and knowledgeable in automated code generation and rapid prototyping.

Keynote Speakers

Keynote 4

Dr. Benoît Dupont de Dinechin
CTO, Kalray , France

Wednesday, June 26th
9:00 am - 10:00 am

Room A + B
Chair: Dr ès sc. Erkan Isa, Fraunhofer EMFT, Germany

Kalray's MPPA® Manycore Processor: At the Heart of Intelligent Systems

Abstract: Intelligent systems can be defined as cyber-physical systems with integration of high-integrity functions, such as control-command, along with high-performance functions, in particular signal processing, image processing and machine learning. Such intelligent systems are required by defense and aerospace applications, and by automated vehicles.

The Kalray MPPA3 manycore processor is designed as a building block for such intelligent systems. Its architecture comprises multiple compute units connected by on-chip global fabrics to external memory systems and network interfaces. Selecting compute units assembled from fully programmable cores, a large local memory and an asynchronous data transfer engine enables to match the high performance and energy efficiency of GPGPU processors, while avoiding their limitations.

For the high-performance functions, we illustrate how the MPPA3 processor accelerates deep learning inference by distributing computations across compute units and cores, and by offloading tensor operations to the tightly coupled coprocessor connected to each core. For the high-integrity functions, we present a model-based systems engineering approach based on multicore code generation from the synchronous-reactive language SCADE Suite from Ansys.

Benoît Dupont de Dinechin is the Chief Technology Officer of Kalray. He is the Kalray VLIW core main architect, and the co-architect of the Multi-Purpose Processing Array (MPPA) processor. Benoît also defined the Kalray software roadmap and contributed to its implementation. Before joining Kalray, Benoît was in charge of Research and Development of the STMicroelectronics Software, Tools, Services division, and was promoted to STMicroelectronics Fellow in 2008. Prior to STMicroelectronics, Benoît worked at the Cray Research park (Minnesota, USA), where he developed the software pipeliner of the Cray T3E production compilers. Benoît earned an engineering degree in Radar and Telecommunications from the Ecole Nationale Supérieure de l'Aéronautique et de l'Espace (Toulouse, France), and a doctoral degree in computer systems from the University Pierre et Marie Curie (Paris) under the direction of Prof. P. Feautrier. He completed his post-doctoral studies at the McGill University (Montreal, Canada) at the ACAPS laboratory led by Prof. G. R. Gao.

Benoît authored 14 patents in the area of computer architecture, and published over 55 conference papers, journal articles and book chapters in the areas of parallel computing, compiler design and operations research.

Keynote Speakers

A1L-A / Neuromorphic Circuits & Neural Networks Session

Monday, June 24th
10:30 am - 12:00 noon

Room A
Chairs: Shahriar Mirabbasi, Mounir Boukadoum

A Semi-Serial Topology for Compact and Fast IMPLY-Based Memristive Full Adders

Nima Taherinejad, Theophile Delaroche, David Radakovits, Shahriar Mirabbasi

Abstract: Memristive systems are among the emerging technologies that hold a great promise. They are compact, CMOS compatible, easy to fabricate and can serve for storage as well as computation purposes. Adders are one of the most basic and critical building blocks of any computing system. One of the main application areas of memristors is in Material Implication (IMPLY) based logic. IMPLY-based adders are implemented either in serial, which has a compact implementation but needs many steps for calculation, or in parallel, which is fast, however, requires a large number of memristors. In this paper we propose an IMPLY-based adder topology and its respective addition algorithm which is 54-to-65% faster than serial adders and requires 46-to-76% less memristors than parallel adders. This topology is a favorable candidate for applications where neither speed, nor cost (i.e., area or number of memristors) could be compromised to gain the required performance.

A Programmable Calculation Unit Employing Memcapacitor-Based Neuromorphic Circuit

Yan Chen, Jing Zhang, Yingjie Zhang, Renyuan Zhang, Mutsumi Kimura, Yasuhiko Nakashima

Abstract: An efficient calculation unit is developed based on programmable neuromorphic circuit for implementing mathematical functions. To retrieve specific function approximately, the regression algorithm through neural network (NN) is realized by a compact analog circuitry. The memcapacitor technology is associated to Neuron-MOS structure, which couples multiple memcapacitors on the floating gate of a transistor for multiply-accumulation operation. Synapse of NN are emulated by memcapacitor which can post-fabrication programmable due to the memristive characteristics of memcapacitor. For proof-of-concept, the calculator for two-operand computations is achieved with 461 devices, which retrieves functions with the maximum inaccuracy of 7.8% and energy of 50.5 pJ.

Activated Current Sensing Circuit for Resistive Neuromorphic Networks

Mohammed Fouda, Ahmed Eltawil, Fadi Kurdahi

Abstract: Recently, resistive-based neural networks have been adopted to build deep learning architectures, where the small area footprint RRAMs (memristors) enables unprecedentedly large neural networks. In this work, we introduce a current sensing circuit and an integrated activation function for resistive neural networks for the first time. This circuit is vital since it is replicated hundreds of times at the outputs of the neurons and thus should be low power and ultra-compact. The proposed circuit is designed using TSMC65nm. The circuit is based on the current conveyor principle and a simple inverter to create the required activation function. The obtained response is curve-fitted to hyperbolic tangent and sigmoid functions to get the accurate expression for the nonlinear function used to design the training technique of the entire neural network. Finally, the proposed circuit is tested in a four-bit neural network based ADC.

Abstracts

A Capacitor-Less CMOS Neuron Circuit for Neuromemristive Networks

Hassan Aziza, Mathieu Moreau, Annie Perez, Arnaud Virazel, Patrick Girard

Abstract: CMOS neuron circuits used to implement neuromorphic chips require extensive circuitry to program the memristive cell, thus eliminating most of the density advantage gained by the adoption of memristive synapses. This paper presents a CMOS neuron circuit that provides a compact and cost-efficient programming interface in which semiconductor capacitors are replaced by a memristive device. The neuron circuit also features an adjustable firing threshold with a strict control of the power consumption during the learning process.

Inequality Constrained Operations Design for Memristor-Only Stateful Logic Within Crossbar Array

Zhwei Li, Haijun Liu, Nan Li, Qingjiang Li, Sen Liu, Hui Xu

Abstract: The huge demand of computing capability in the era of big data issues a challenge for the conventional CMOS hardware and the von Neumann architecture. one of the promising solutions is the memristor based logic-in-memory scheme, where the stateful logic operations are performed in situ within a crossbar array, thus eliminating the data transfer to a processor. However, the current proposed memristor-only stateful logic design only allows limited logic function gates mapping to the crossbar array. This paper studies the universal case of memristor-only stateful logic. And through the analysis of inequality constraints, a theoretical framework is derived, which assist the exploration the complete optimal operation design. The result shows 7 logic gates could be realized in one pulse step based on memristor-only stateful logic in this design, and the most complex logic gates is XOR operation, which requires 3 steps, 4 memristor devices.

A1L-B / Robust & Reliable Circuit Design Session

Monday, June 24th
10:30 am - 12:00 noon

Room B

Chair: Fakhreddine Ghaffari

3A Fault Tolerant Low Side Driver Circuit Design Using Design FMEA for Automotive Applications

Sri Navaneeth Easwaran, Martin Mollat, Deepak Sreedharan, Samir Camdzic, Sunil Venugopal Kashyap, Robert Weigel

Abstract: Electronic components in Automotive have to be fault tolerant and need to fulfill system safety requirements. One such safety system is the Airbag Control Unit (ACU) with integrated Squib Drivers that deploys airbags. The safety critical part of these drivers is the High Side and Low Side powerFETs with its pre-drivers. Airbags needed for driver safety can end up fatal if deployed inadvertently. Therefore, components used in ACU have to fulfill the highest system Automotive Safety Integrity Level (ASIL), ASIL-D. This paper describes a systematic design Failure Mode Effect Analysis (FMEA) design methodology for the low side driver that resulted in a unique safety architecture to prevent inadvertent activation in unpowered state. In the powered state, the current is regulated to 3A and is stable for wide inductive load range.

Substrate Coupling in a Fully Integrated Three-State High Voltage Inverter

Katrin Hirmer, Klaus Hofmann

Abstract: Substrate coupling is a major issue for high voltage (HV) integrated circuits (IC). Prediction during the design phase is essential to prevent failures of fabricated ICs. A fully integrated three-state inverter with up ±300V is fabricated in a 1µm process. Double-diffused MOS transistors within the output stage are capacitively coupling

Abstracts

onto the handle wafer of a Silicon-on-insulator wafer. A substrate network for the capacitive coupling of switching HV to low voltage nodes is presented. Technology computer aided design simulations as well as measurements prove the IC design prediction of substrate coupling for low frequency operation.

Electronic System Level Design of Heterogeneous Systems: a Motor Speed Control System Case Study

Breytner Joseph Fernández-Mesa, Liliana Andrade, Frédéric Pétrot

Abstract: Although SystemC and its AMS extensions are widely promoted for the design of heterogeneous systems, very few complete cases studies are actually available. In this work, we present a digital and an analog version of a motor speed controller, and detail various modeling approaches. In the digital version, the executable specification is refined to a TLM virtual prototype that runs SW code on a QEMU emulated RISC-V, to study the effect of HW/SW design decisions on the physical system dynamics. In the analog version, the controller equation is mapped to a SystemC AMS model and refined from the discrete-time to the continuous-time domain. By simulating this system, we illustrate the effectiveness of SystemC and SystemC AMS for heterogeneous design space exploration. The example is available at github.com/newcas2019/motor_control.

MAGIC: a Wear-Leveling Circuitry to Mitigate Aging Effects in Sense Amplifiers of SRAMs

Alexandra Listl, Daniel Mueller-Gritschneder, Ulf Schlichtmann

Abstract: Many embedded systems such as automotive and industrial Micro-Controller Units (MCUs) use on-chip SRAM as main data memory of the embedded processor. However, SRAMs are increasingly susceptible to reliability threats such as Bias Temperature Instability (BTI) due to the continuous trend of technology shrinking. BTI leads to a significant performance degradation, especially in the Sense Amplifiers (SAs) of SRAMs, where failures are fatal, since the data of a whole column is destroyed. In this paper we present the Mitigation of AGIng Circuitry (MAGIC), a low-cost circuitry to effectively mitigate aging in SAs by wear-leveling. The circuitry consists of an array of XOR gates and a counter. MAGIC modifies the mapping of SRAM banks to physical addresses. Updating the counter value distributes the stress of highly used addresses, e.g., corresponding to program stack data, onto the complete SRAM array. We evaluate the wear-out for on-chip SRAM data memory loads of a typical embedded application. MAGIC mitigates SA degradation up to 48% for three years of aging while introducing minimal area/performance overhead.

µW Pre-Processing Unit for Virtual Sensors Based on Tri-Axial Smart Accelerometers

Antonio De Vita, Gian Domenico Licciardo, Aldo Femia, Luigi Di Benedetto, Danilo Pau

Abstract: In this paper, for the first time in the literature, a custom circuit is proposed to process the heavy calculations needed to change in real-time the reference coordinate systems of vectors measured by tri-axial accelerometers, in order to make a pre-processing stage for the building of virtual sensors like linear and gravity accelerometers. To the purpose, a new "hardware friendly" algorithm has been derived which can be implemented in a more compact iterative structure to combine high accuracy and low power consumption, in order to conveniently integrate it into the circuitry of smart accelerometers. Synthesis with 65 nm CMOS std_cells returns a power dissipation of 0.89 uW and an area of about 0.024 mm^2 . Results are the current state-of-the-art for this kind of applications and they are very promising for the implementation in smart sensors for wearable applications.

Abstracts

SPECIAL SESSION
SOI Ecosystem for 5G

Monday, June 24th
1:30 pm - 3:00 pm

Room A + B

Chair: Prof. Christoph Kutter, Fraunhofer EMFT, Munich

Keynote: 5G Ecosystems

Dr. Carlos Mazure
SOI Consortium Executive Director

Dr. Carlos Mazure has led the development of strategic advanced technologies at Soitec since 2001. He works closely with academic research labs and Soitec customers and suppliers to develop new applications for Soitec's Smart Cut™ technology.

Prior to joining Soitec, Carlos Mazure served as executive vice president, business development at Infineon Technologies AG, where he was involved with the IBM-Infineon DRAM Development Alliance. His experience also includes work on BiCMOS-on-SOI high-performance components at Motorola Corp.

Mazure has filed more than 100 patents worldwide and is the author of 120 scientific papers. He holds two PhDs in physics, one from the University of Grenoble, France, and the other from the Technical University of Munich, Germany.

Foundry vision: 5G Ecoystem in Europe and Beyond: The Globalfoundries Perspective

Dr. Gary Patton
Globalfoundries CTO and SVP, Design Enablement and R&D

Dr. Gary Patton is the Chief Technology Officer and Senior Vice President of Design Enablement and Worldwide Research and Development at GlobalFoundries. He is responsible for GF's semiconductor technology R&D roadmap, operations, and execution.

Prior to joining GF, Dr. Patton was the Vice President of IBM's Semiconductor Research and Development Center - a position that he held for eight years where he was responsible for IBM's semiconductor R&D roadmap, operations, execution, and technology development alliances across multiple locations. Dr. Patton is a well-recognized industry leader in semiconductor technology R&D with over 30 years of semiconductor experience.

Dr. Patton received his B.S. degree in electrical engineering from UCLA and his M.S. and Ph.D. degrees in electrical engineering from Stanford University. He is a Fellow of the IEEE and recipient of the 2017 IEEE Frederik Philips Award.

He has co-authored over 70 technical papers, given numerous invited keynote and panel talks at major industry forums, and served on the IEEE Nishizawa Medal and Grove Field Award Committees.

Application: 5G for Aviation and Space

Dr. Dominic Schupke
Director of Research and innovation in Wireless Communications at Airbus

Dr. Dominic A. Schupke leads research and innovation in Wireless Communications at Airbus in Munich, Germany. Previously he was with Nokia/NSN, Siemens, and the Munich University of Technology (TUM). He received his Dipl.-Ing. degree from RWTH Aachen in 1998 and his Dr.-Ing. degree from TUM in 2004. Since April 2009 he has been teaching the course Network Planning at TUM.

Dominic authored or co-authored more than 120 journal and conference papers (Google Scholar h-index 29), as well as several patents. Three contributions received a best paper award.

His research focuses on reliable communication networks and network design. His research interests include network architectures and protocols, routing, recovery methods, availability analysis, critical infrastructures, security, virtualization, network optimization, and network planning. Dominic has been Editorial Board Member of the IEEE Communications Surveys and Tutorials since August 2010 and he was also Associate Editor of the IEEE/OSA Journal of Optical Communications and Networking from March 2009 to August 2013.

He was co-chair of the Conference on Design of Reliable Communication Networks (DRCN) in 2017 and of the Optical Fiber Communication Conference (OFC) in 2013. He served as TPC chair and TPC member for numerous conferences. Currently, he is TPC co-chair for DRCN 2019.

Dominic is Senior Member of IEEE, and member of Comsoc, VDE/ITG, and VDI. He was appointed to an IEEE ComSoc Distinguished Lecturer for 2013 and 2014. Dominic received the Outstanding Service Award of IEEE Optical Networking Technical Committee (ONTC) for Key Efforts in Industry Outreach, 2017.

Abstracts

A2L-A / SPECIAL SESSION
SOI based RF and mm-wave Design Session

Monday, June 24th
3:30 pm - 5:00 pm

Room A
Chair: Eric Kerhervé

Fully-Depleted SOI Technology for RF / mmWave aplications in & beyond the 5G era

presentation only

Maciej Wiatr, Globalfoundries

Abstract: With wider bandwidth, bigger capacity and higher reliability, the 5th generation (5G) of the mobile network is well on its way to significantly enhance and lower the costs of mobile broadband services available today. 5G is redefining a wide range of industries by providing a unifying platform for connecting old, new and future services. Due to the smaller parasitic and reduced gate resistance along with digital computational performance at low power, 22nm Fully-Depleted-SOI (22FDX®) technology becomes the technology of choice to fulfill this broad range of requirements. FDSOI-specific technology setup and design techniques allow the creation of RF/mmWave circuits with excellent characteristics for 5G applications. In this talk we will introduce both, the technology setup and examples of circuit designs demonstrating the capabilities of 22FDX® for the 5G era (and beyond).

FD-SOI for Automotive Radar

presentation only

Yvan Morandini, Soitec

Abstract: In the past, automotive radar system has been designed using SiGe process due to its available high FT/Fmax , lower noise and high breakdown voltage devices. However, to reduce the system costs, high level of integration is desired and CMOS bulk technology is an alternative. In this presentation, we will demonstrate FD-SOI technology capability to adress mm-wave automotive radar with high performances Power Amplifier (Psat > 17dBm and PAE>15%) and 40% lower digital power consumption compared to the bulk technology.

New Design Opportunities Exploiting FDSOI Technology for RF Power Amplifier and LNA Design

Frederic Hameau, Jennifer Zaini, Thierry Taris, Dominique Morche, Baudouin Martineau, Patrick Audebert

Abstract: To demonstrate the capacity of FDSOI technology, this paper presents two RF designs taking benefit of the advantages of the FDSOI. Specific process opportunities and body biasing are used to reduce area and improve RF performance. First, a WiFi PA with 1.8V thick oxide MOS is presented. This PA exhibits a 23dBm Psat output power and 8% PAE. Then an Low Power LNA is presented. Based on a boosted common gate architecture, this LNA has been implemented reaching 7.3dB Noise Figure (NF) under 0.6v power supply. This structure points out the potential of back biasing to reduce the power consumption.

A 2.5GHz LTE Doherty Power Amplifier in SOI-CMOS Technology

Marc Borremans, Paramartha Indirayanti, Carl De Ranter, Renaud Mourot, Rana Berro, Pascal Reynier, Damien Parat, Ayssar Serhan, Alexandre Giry, E. Mercier

Abstract: The need for RF Front-Ends Module (FEM) with reduced size and cost is driving research towards highly integrated Power Amplifiers (PA) with challenging linearity and efficiency requirements. To overcome efficiency challenges, the Doherty PA (DPA) architecture represents an attractive solution because of its high back-off efficiency and relatively simple structure. This paper presents a state-of-the art SOI CMOS DPA design implemented in a 0.13um SOI CMOS industrial process. At 2.5GHz, the 2-stage SOI CMOS DPA achieves a measured peak PAE of 57% at 32.7dBm output

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power under 3.4V voltage supply. At 1dB compression point, output power and PAE are 32.4dBm and 56% respectively. With a 10MHz LTE uplink signal, a linear output power of 29.4dBm is measured with a PAE of 48.8% at an ACLR level of -33dBc without using DPD.

Systematic Design of on-Chip Matching Networks for D-Band Circuits

Johan Nguyen, Xinyan Tang, Khaled Khalaf, Bjorn Debaillie, Piet Wambacq

Abstract: Design of mm-wave circuits operating above 100 GHz is challenging due to loading effects between different components, device and layout parasitics. In this work, we propose a systematic approach for multistage differential designs. This approach provides with accuracy the scattering parameters for every possible realization of the chosen matching network within a broad search space, hereby considering loading effects and matching constraints.

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Silver Sponsor

A2L-B / Efficient Image & Video Processing Session

Monday, June 24th
3:30 pm - 5:00 pm

Room B
Chairs: Daniel Massicotte, Benoit Gosselin

Maximizing the Power-Efficiency of the Approximate Pruned Modified Rounded DCT Exploiting Approximate Adder Compressors

Guilherme Paim, Leandro M. G. Rocha, Eduardo Costa, Sergio Bampi

Abstract: This paper proposes the use of approximate adder compressors for a low-power 8-point Modified Rounded Discrete Cosine Transform (MRDCT10) implementation. The algebraic approximation of the MRDCT was previously introduced in the literature, whose resultant matrix is only composed of 0, 1 and -1 values. Therefore, the MRDCT can be efficiently implemented using only adders and subtractors. We present an environment for the synthesis of the MRDCT in Cadence RTL Compiler tool. The synthesis reports are based on a set of real images as input vectors to obtain valid power results. Our results show that the use of approximate adder/subtractor compressors in hardwired state-of-the-art 8-point approximate MRDCT10 achieves savings ranging from 26% to 52.54% when compared with the macro function (+) from the tool.

Energy Savings with Non-Volatile Memory System for High Definition Video Encoders

Dieison Silveira, Ana Mativi, Marcelo Porto, Sergio Bampi

Abstract: This paper presents an evaluation of different schemes with data reuse using different memory technologies in the memory hierarchy, including NVMs, such as: PCRAM, ReRAM and STTRAM. Our results show that schemes composed by DRAM and NVM present energy savings of 43%, on average, when compared to conventional DRAM and SRAM schemes. Furthermore, the best results were obtained with ReRAM as external memory and ReRAM or STTRAM as the scratch-pad memory, such configurations reach a total memory energy consumption reduction of 89% and 87%, respectively, when compared to the conventional configuration of external DRAM and on-chip SRAM memories.

Wireless Capsule Endoscopic Image Enhancement Method Based on Histogram Correction and Unsharp Masking in Wavelet Domain

Mingzhu Long, Xiang Xie, Guolin Li, Zhihua Wang

Abstract: In this paper, a method based on histogram correction and unsharp masking in the wavelet domain is proposed to improve the contrast and reveal details of endoscopic images. the hsi color space is adopted for color naturalness, and a logarithm based histogram correction method (lhcm) is proposed to improve the contrast and avoid aritifacts. details are further enhanced by unsharp masking. experimental results show that performance of the proposed method is better compared with the state-of-art methods. it can be applied to general images and have good effects as well.

Exploring Motion Vector Cost with Partial Distortion Elimination in Sum of Absolute Differences for HEVC Integer Motion Estimation

Brunno Abreu, Mateus Grellert, Guilherme Paim, Thomas Fontanari, Leandro M. G. Rocha, Eduardo Costa, Sergio Bampi

Abstract: Integer Motion Estimation (IME) is one of the most costly steps in the video coding process, being responsible for 60% Of the total encoding time. Two parameters are considered when calculating the redundancies (distortion) between video blocks: Sum of Absolute Differences (SAD) and motion vector cost (MVcost). Partial Distortion Elimination (PDE) techniques may be used to

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optimize the calculation of the SAD unit itself, in order to avoid the computation of candidates that will certainly not be Selected in the IME. This paper proposes an optimization in the distortion calculation by taking advantage of the PDE technique in the SAD operation by including the MVcost, to save even more cycles when compared to standard PDE usage, considering the High-Efficiency Video Coding (HEVC) standard. We found out that the inclusion of MVcost in the distortion cost achieves a quality increase of up to 1.28%. We compare three versions: MVcost before/after SAD using a multiplexer, and before SAD using a CSA.

Distributed Embedding Approach for Max-Plus Algebra-Based Morphological Wavelet Transform Watermarking

Takeshi Kumaki, Tomohiro Fujita, Takeshi Ogura, P.S. Venugopala

Abstract: This paper presents distributed embedding approach for the max-plus algebra-based morphological wavelet transform watermarking. Distributed embedding approach uses low- and high-frequency-included signal groups after decomposition process for embedding information bits. During experiments, benchmark images processed by the distributed approach using the MMT watermarking are of improved image quality up to 1.18 and 1.14 on PSNR and SSIM, respectively. Furthermore, this approach obtains better results in comparison with related works.

A3L-A / SPECIAL SESSION: 5G and beyond: from Material to Systems Session

Monday, June 24th
5:00 pm - 6:30 pm

Room A

Chair: Linus Maurer

SOI for 5G RF Systems – Challenges and Solutions

presentation only

Yvan Morandini, Soitec

Abstract: 5G new frequencies and techniques (carrier aggregation, MIMO, beam forming) add considerable challenges to new RF Front End designs and their implementation. For 5G sub 6GHz, there is a significant increase of the number of RF blocks (antennas, antenna tuners, filters, switches, low noise amplifiers and power amplifiers) that need to co-exist without increasing interference and/or footprint. In parallel, SoC integration for 5G mm-wave has become a high value added option easing design and implementation of highly complex RF functions. In this presentation, we will highlight the role of RF-SOI and FD-SOI substrates helping achieving identified stringent technical requirements introduced by 5G current and future standards.

Going from a 5G Vision to Real Implementation

Fredrik Tillman, Sven Mattisson, Ericsson

Abstract: In this paper we review existing market deployments and predictions for the coming years. Examples of 5G scenarios are given and implications on the transceiver hardware are examined with respect to building practice, antenna integration, and cost. The continuation of the first 5G NR standard is further discussed and design considerations affecting commercial realizations presented.

Abstracts

Design of a 28 GHz Differential GaAs Power Amplifier with Capacitive Neutralization for 5G mm-Wave Applications

Dongyang Yan, Mark Ingels, Giovanni Mangraviti, Yao Liu, Bertrand Parvais, Niamh Waldron, Nadine Collaert, Piet Wambacq

Abstract: This paper describes the design of a 28 GHz power amplifier (PA) in a commercial GaAs mHEMT technology using concepts that are typical for mm-wave CMOS design. Simulations show a 1dB output compression point of around 23 dBm with a 30% power-added efficiency (PAE) at 28 GHz, while providing a gain of 12 dB. Comparison with the performance of a similar 28 GHz fully-depleted Silicon-On-Insulator (FDSOI) PA shows an increase of the compression point with 10 dB while efficiency is comparable. The high compression point of this GaAs PA offers a margin for system optimization such as a reduction of the number of antennas for beamforming.

DoA Estimation Using Reconfigurable Antennas in Millimiter-Wave Frequency 5G Systems

Mateusz Rzymowski, Kamil Trzebiatowski, Krzysztof Nyka, Lukasz Kulas

Abstract: To achieve low latency and high throughputs, future 5G systems will have to utilize complex antenna systems able to provide beamforming and direction-of-arrival (DoA) estimation capabilities. Most of the concepts available in the literature rely on analog or digital beamforming, which is well developed and can be used both at a base station and in a user terminal. However, in applications, in which energy-efficiency or cost is one of the key concerns, the use of traditional beamforming systems is limited. To overcome this limitation, reconfigurable antennas can be used as they rely on a simple but effective concept, in which a transceiver is connected to a single input port and beamforming capabilities are enabled by a number of passive elements electronically switched via transceiver's digital input-output ports. In the article, we show how simple single-input mm-wave reconfigurable antenna can be used to provide not only beamforming but also DoA capabilities relying on received signal strength measurements. Therefore, the proposed approach can be applied in future 5G millimeter-wave nodes or gateways, in which low-cost and power-efficiency are important.

Design of a D-Band Transformer-Based Neutralized Class-AB Power Amplifier in Silicon Technologies

Xinyan Tang, Alaaeldien Medra, Johan Nguyen, Khaled Khalaf, Björn Debaillie, Piet Wambacq

Abstract: High-speed wireless communication in the post-5G era will likely make use of frequency bands above 100 GHz. This poses challenges to IC design in silicon technologies. This paper presents a general comparison of a D-band transformer-based Class-AB power amplifier with cross-coupled capacitive neutralization in three advanced silicon technologies: bulk CMOS, fully-depleted SOI, and SiGe BiCMOS. Each of these technologies has its own prospects and disadvantages. A comparison of performance parameters is made such as the maximum available power gain Gmax, saturation power Psat, drain efficiency DE and power added efficiency PAE after properly sizing the transistors to reach an optimum load resistance Ropt. Further, a 140 GHz 4-stage power amplifier is fabricated in a 28 nm bulk CMOS process as a reference. Its design considerations, layout parasitics analysis, and layout techniques are discussed as well.

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A3L-B / Digital Circuits & Designs for Digital Systems Session

Monday, June 24th
5:00 pm - 6:30 pm

Room B
Chair: Yvon Savaria

High-Level Availability Analysis of FPGA-Based Time-Sensitive Networks

Ayman Atallah, Ghaith Bany Hamad, Otmane Ait Mohamed, Mounir Boukadoum

Abstract: In this paper, we investigate the availability of FPGA-based TSN under a harsh radiation environment. In particular, we propose a framework to evaluate the communication availability of FPGA-based TSN components and investigate the impact of periodic repair mechanisms, such as periodic reconfiguration, on the communication availability. To achieve our goal, we propose a new Priced Timed Automata (PTA) model of TSN network to capture the impact of periodic repair on communication reliability. As a result, the proposed framework allows the designer to set up the appropriate repair cycle according to the application criticality and required system reliability.

The Probabilistic Finite Alphabet Iterative Decoder for Low-Density Parity-Check Codes

Fakhreddine Ghaffari, Khoa Le, David Declercq

Abstract: We propose in this paper a new approach of applying the Non-Surjective Finite Alphabet Iterative Decoder (NS-FAID) for the Low-Density Parity-Check (LDPC) decoding. Differently from the NS-FAID which applies a fixed nonlinear function by using a fixed Look-Up-Table (LUT) on the variable node messages, the proposed method, called Probabilistic FAID (PFAID), uses more than one LUT in a probabilistic way. By using the density evolution, we show that this method provides a significant improvement in performance compared to the NSFAID and the traditional MS. The advantage of PFAID is shown by the fact that, a PFAID with low message quantization level can reach or even surpass the performance of the higher level quantization MS decoder. Furthermore, we show that PFAID can be efficiently implemented with no hardware overhead compared to Min-Sum (MS) or NS-FAID with the same message quantization level. The hardware complexity analysis and decoding simulation performance are provided as superiority evidences of PFAID over the referenced benchmarks.

Accurate and Efficient Interdependent Timing Model for Flip-Flop in Wide Voltage Region

Peng Cao, Zhiyuan Liu, Jingjing Guo, Haoyu Pang, Jiangping Wu, Jun Yang

Abstract: The interdependency of the setup and hold constraints and the clock-to-q (c2q) delay for flip-flops (FF) has been studied in static timing analysis (STA) to facilitate timing closure and improve circuit performance. Circuits operating in near-threshold voltage (NTV) region obtains remarkable energy efficiency improvement but poses severe challenge to the interdependent timing modelling due to its significant nonlinear relation and much wider constraint range compared with super-threshold voltage (STV) region. In this paper, an accurate and efficient modelling approach is proposed by employing artificial neuron network (ANN) to characterize the interdependency among the setup time, hold time and c2q delay of FF for in wide voltage region. Experimental results show the prediction errors of c2q delay with varied setup and hold constraints are lower than 2.1% and 1.8% in NTV and STV regions respectively with 3.51× and 1.09× accuracy improvement compared with the prior work. Besides the advantage in accuracy, the modelling efficiency is validated by 1.41×/1.10× simulation cost reduction and 21.08×/4.14× library storage saving for NTV/STV domain.

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Efficient Arbitrary Sample Rate Conversion for Multi-Standard Digital Front-Ends

Ali Zeineddine, Stéphane Paquelet, Amor Nafkha, Pierre-Yves Jezequel, Christophe Moy

Abstract: In this paper, we study the hardware implementation of arbitrary sample rate conversion (ASRC) using recently proposed variable fractional delay filter (V-FDF) structures. The most commonly used solution to implement V-FDFs has been the Farrow structure for the last three decades. In this work, we develop and compare the implementations of different recently proposed V-FDF options based on the Newton structure. These implementations are done on both ASIC and FPGA targets. The obtained results show that the recently proposed solutions offer better ASRC performance while using up to 3 times less resources relatively to the classical Farrow structure. The generic nature of these filters make them suited for a large number of standards.

Generic Hardware of Fractional Order Multi-Scrolls Chaotic Generator Based on FPGA

Merna Roshdy, Mohammed F. Tolba, Lobna Said, Ahmed Madian, Ahmed G. Radwan

Abstract: Exploring the implementation of fractional calculus is essential to be adequately used in several applications. This pa- per introduces an FPGA design methodology of fractional order multi-scrolls chaotic system based on FPGA. Hardware resources comparison proves the efficiency of the proposed system. The designs are simulated using Xilinx ISE 14.7 and realized on FPGA Xilinx Artix 7. Different interesting attractors are realized under various parametric changes with distinct step sizes for different fractional-orders. To verify the proposed fractional order multi- scrolls chaotic system on FPGA, an oscilloscope experimental results have been added. The experimental results show a good performance compared with MATLAB simulations and previous works.

B1P-C / Posters & Demonstrators Session

Tuesday, June 25th
11:00 am - 12:00 noon

Foyer (see floor plan page 8)

Chairs: Linus Maurer, Benoit Gosselin

Adaptive Bivariate Function Generation Based on Chebyshev-Polynomials

Jochen Rust, Pascal Seidel, Steffen Paul

Abstract: In this paper an adaptive hardware architecture for high-performance bivariate numerical function approximation is presented. Orthogonal Chebyshev-Polynomials are exploited that cover incremental accuracy refinements. Additionally, switching between two numeric functions is easily deployable by changing the set of polynomial coefficients. For evaluation, different configurations of the proposed hardware function generator are implemented and analyzed considering three bivariate numeric functions. The resulting performance highlights this approach to be a powerful extension for bivariate function approximation.

Towards Accurate Camera-Less Eye Tracker Using Instrumented Contact Lens

Loïc Massin, Cyril Lahuec, Vincent Nourrit, Fabrice Seguin, Jean-Louis de Bougrenet

Abstract: This paper presents a camera-less eye tracker. Composed of 2 parts, an instrumented contact lens and spectacles, its principle consists in computing a barycenter based on the light intensity variations received from the spectacles onto the lens. To demonstrate both the method and the achieved accuracy it yields, a prototype lens fitted with 4 infrared sensors has been fabricated and tested. Based on measured photo-currents, simulations, both behavioral and at transistor level (AMS 0.35 µm CMOS), show

an accuracy of 0.1° can be achieved. Which is a significant improvement to the 1° camera-base eye trackers offer.

A Verilog-A Model of the Shuttle of an Electron in a Two Quantum-Dot System

Imran Bashir, Panagiotis Giounanlis, Elena Blokhina, Dirk Leipold, Krzysztof Pomorski, Robert Bogdan Staszewski

Abstract: We describe a model of the bi-directional tunneling motion, also referred to as "shuttle'', of an electron between two quantum dots operating at cryogenic temperatures. The model, written in Verilog-A, is simulated in a Cadence Spectre environment with interfacing elements that constitute a quantum experiment test bench. This method of simulating a quantum structure paves the way for the analysis of sophisticated quantum experiments over a large number of cells and top level SoC verification.

Sorn Arithmetic for MIMO Symbol Detection – Exploration of the Type-2 Unum Format

Moritz Bärthel, Pascal Seidel, Jochen Rust, Steffen Paul

Abstract: In this paper a new approach for a fast and low precision number format is explored. The SORN representation uses a fixed set of exact values and open intervals in between to represent real numbers on the digital layer. With SORN arithmetic operations can be carried out using simple lookup tables which results in a very fast and low-complex way of computing. The new arithmetic is applied to an exhaustive search algorithm for maximum likelihood symbol detection in a MIMO transmission environment. The algorithm is implemented in hardware and executed on a Zynq-7000 FPGA.

Construction of Delay-Driven GNR Routing Tree

Jin-Tai Yan, Chia-Heng Yen

Abstract: It is known that graphene nanoribbon (GNR) based devices and interconnects can be treated to be better alternative in nano-scale designs. In this paper, given a source pin and a set of target pins inside a GNR grid-based routing plane, based on the consideration of the wirelength and bending delay in graphene nanoribbon, an efficient routing algorithm can be proposed to construct a delay-driven GNR routing tree with minimizing the total wirelength for the target pins. Compared with Das's algorithm [10] on total wirelength and maximum source-to-target delay, the experimental results show that our proposed routing algorithm only uses 8.05% of the extra wirelength to reduce 23.13% of the maximum delay in the construction of a delay-driven GNR routing tree for 6 tested examples on the average.

A 900-MHz 1.25-dB Noise-Figure Differential-Output LNA with 12.5 dB/mW FoM

Atul Thakur, Sweta Agarwal, Shouri Chatterjee

Abstract: A 900 MHz LNA with balanced output and 12.5 dB/mW figure-of-merit (FoM) is presented. The architecture exploits the benefits of both inductive degeneration and noise cancellation which helps in achieving the optimum noise figure (NF). The LNA has a wideband gain and input matching is achieved using an off-chip inductor. Inductive degeneration and quality factor (Q) of the input matching network improves the NF of the LNA (with wideband gain) at a spot frequency. The transconductance of the core-LNA is fixed by a constant-gm circuit. Simulation results show that the LNA has a minimum NF of 1.25 dB at 900 MHz, transmission gain (S 21) of 33 dB, S11 of -19 dB at 900 MHz, IIP 2 of +2 dBm, and IIP 3 of -15 dBm. The LNA, designed in 180 nm CMOS, consumes 4.4 mA from a 1.8 V supply and has a negligible differential-gain error of 0.138 dB, at the input matched frequency. Balanced mixer on top of the LNA, resuing the LNA current, is implemented which shows promising NF of 2.5 dB.

Shared Wireless Link co-Design for Implantable Device with Far-Field Wireless Power Transfer

Vitor Silva, Hugo Dinis, Paulo Mendes

Abstract: Implantable devices are nowadays commonly used in medicine. However, these devices run mostly on

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batteries, leading to a finite lifetime due to the required batteries replacement. Since wireless power is almost available everywhere, a suitable way to avoid battery replacement would be to recharge them wirelessly using wireless power. As these implantable devices mostly features a single antenna, it must be shared to communicate and to receive power. In this way, a circuit that turns off the communication blocks and other circuits, while recharging, is needed. In this paper, an RF CMOS frontend with far-field wireless powering for implantable devices with a power management module will be presented. This circuit is able to control the front-end circuits when the battery reaches predefined operating voltages.

Exploring Schmitt Trigger Circuits for Process Variability Mitigation

Leonardo Moraes, Alexandra Zimpeck, Cristina Meinhardt, Ricardo Reis

Abstract: Process variability has become one of the major factors concerning variations in metrics, such as performance and energy consumption, due to the aggressive technology and voltage scaling. This work analyzes the impact on variability robustness of a Schmitt Trigger-based technique. Several works point that the considered technique helps to improve the variability robustness at the electrical level. The technique was applied on four Full Adder considering two different Schmitt Triggers designs at layout level using the 7nm FinFET technology node from ASAP7. Performance, energy and area are taken into account. Results show, in average, up to 36% and 45% improvement in delay and energy variability robustness, respectively.

Dark Count Rate Modeling in Single-Photon Avalanche Diodes for Space LIDAR Applications

Aymeric Panglosse, Philippe Martin-Gonthier, Olivier Marcelot, Cédric Virmontois, Olivier Saint-Pé, Pierre Magnan

Abstract: In this paper, we present a model to simulate accurately the Dark Count Rate (DCR) for Single Photon Avalanche Diode (SPAD) in Complementary Metal-Oxide Semiconductor (CMOS) technology. The model development has been driven by the necessity to comply with the specifications of SPAD used for future space LIDAR applications. To evaluate the DCR, the model is based on a combination of measurements to acquire data related to trap population, Technology CAD (TCAD) simulations and a Matlab routine.

GCoL – a General Co-Simulator Applied to Wireless Sensor Networks and RTL Design

Grégory Calegari Marchesan, Everton Carara, Cristian Müller, Leonardo Oliveira

Abstract: Standard wireless sensor systems and IoT devices demand application-oriented designs due to severe power constraints. We present GCoL, a framework that replaces traditional created virtual sensor nodes with a physical hardware description in a wireless sensor network simulation. It comprises a simple but efficient configuration script, scenario interface for deployment nodes and related graphical and data reports. The hardware-software co-simulation guarantees the accurate emulation of an embedded algorithm. The overall power consumption and timing of intended application can be acquired through any traditional ASIC flow. The proposed system is capable of simulating dedicated hardware through a wireless sensor network environment designed with Matlab which provides suitable libraries for digital signal processing and control algorithm behavior simulation. The platform takes advantage of robustness communication toolboxes and graphical user interface of Matlab to aid users to develop, improve and better create specific hardware applications which will be later executed on the nodes.

Abstracts

Using Deep Learning Approaches to Overcome Limited Dataset Issues Within Semiconductor Domain

Milad Omrani Tamrin, Sebastien Henwood, Jean-Francios Dubois, Jean-Jules Brault, Saad Chidami, Samuel-Jean Bassetto

Abstract: Today, in semiconductor manufacturing, wafer failures are frequent problems with the production lines. To increase the production yield, images are the most important pieces of data used to detect defect-free wafers. However, there are many tools that can be installed specifically to monitor production lines, inspect mapped defects and detect the main causes of die failures by using wafers images during the semiconductor manufacturing process. The underlying objective is to overcome the need for a physical check on the wafer which are in most cases too long. Thus, the need to have a design that will measure and detect these visual faults in an automated fashion is a big challenge for the industry. Recently, deep learning approaches have proven to be a suitable way to overcome this issue. However, they rely on the availability of sufficiently representative datasets which is not our case: data on anomalies is scarce. The goal of this paper is to evaluate the state of the art deep learning methodology such as GAN and VAE to overcome this challenge.

An RNN-Based Speech Enhancement Method for a Binaural Hearing Aid System

Zhuoyi Sun, Yingdan Li, Hanjun Jiang, Zhihua Wang

Abstract: This paper presents a recurrent neural network (RNN)-based speech enhancement method for a binaural hearing aid system. We design a binaural RNN architecture to train gains of subbands. The proposed method trains the binaural recurrent neural network from binaural signals separately before concatenating to a weighting fully connected layer. The method preserves more cues from binaural signals using different training strategies and weighting variations. The results show the proposed method achieves a balance between speech intelligence and noise suppression in different acoustics scene. We demonstrate that the proposed method can implement speech enhancement for hearing aids with a low complexity neural network. This makes it applicable on smartphone or embedded devices.

Physically-Derived 3-Box Power Amplifier Model

Elias Soleiman, Dang-Kièn Germain Pham, Chadi Jabbour, Patricia Desgreys, Mahmoud Kamarei

Abstract: In this work, a novel approach to reduce the complexity of memory polynomial model is presented. The proposed technique, named the coefficient decomposition (CD) technique, is based on reducing the search space for the memory polynomial coefficients based on memory effects generation mechanism. In this paper, the technique is demonstrated for power amplifier of classes A and AB. In this case, the physical analysis shows that the conventional two-dimensional coefficient architecture of the memory polynomial could be simplified into a one dimensional architecture while keeping almost the same accuracy. The performance of the proposed approach is demonstrated and compared with other models using a 30 dBm commercial power amplifier with 20 MHz and 60 MHz LTE signals. The measurements and simulations showed that, the presented model achieves –34:2 dB of NMSE while needing only 13 coefficients compared with 25 needed for a memory polynomial model. Also, the DPD performance of the proposed model is the same as memory polynomial model and comparable with high complexity models like the PLUME and GMP.

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OCEAN12 (ECSEL JU) Project

Francois Brunier, Soitec

Abstract: OCEAN12 is a major "Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node" and leverage Europe leadership on Automotive and aeronautics applications. For the last years, electronic components become more and more widespread in the automotive industry. Today they create a superior value for the final customer and represent an important vector of differentiation in the industry. The sharing economy model, which drives innovation strategies in Smart mobility, will further increase the need for safe, cost efficient, secure, reliable and unhackable operations. This will enlarge costs of electronics and software in the total cost of a vehicle. OCEAN12 will bring very concrete technological solutions and corresponding demonstrators for this problem. Based on the innovative Fully Depleted Silicon On Insulator (FD-SOI) technology, the project aims to develop new processors and applications design, which will leverage FD-SOI to offer the industry's lowest power consuming processor and components, mainly for automotive and aeronautic applications. The project highlights Europe's unique leading position on FDSOI technology, integrating the entire manufacturing chain - from substrate suppliers and foundries to TIER-1 and OEM, involving academia and RTO's. By doing so, it aims to secure a unique FDSOI roadmap beyond the 22FDX.

REFERENCE (ECSEL JU) Project, Aeronautic WAIC hotspot: wireless video transmission using an SOI RF front-end

Leonardo Govoni, T. Perekhodko (AED Engineering), P. Kumar, L. Maurer (University of Bundeswehr Munich), D. Schupke, T. Meyerhoff (Airbus), E. Böhme (Fraunhofer EMFT), M. Kreissig, F. Protze, S. Damjancevic (TU Dresden)

Abstract: In the framework of the Horizon 2020 ECSEL JU funded project REFERENCE, a demonstrator is implemented that aims the development of a WAIC (Wireless Avionic Intra-Communications) hotspot based on an SDR (Software Defined Radio) hardware employing new RF SOI components. The Wireless Transmission System (WTS) is composed of an FPGA based board and a RF analogue front-end, based on RF SOI technology. The processing unit performs the ADC/DAC conversion and analog signal conditioning, I/Q modulation and amplification to drive the antenna. In the current demonstrator the RF front-end is substituted by COTS product.

SERENE-IoT (PENTA) Project, MRSA Detector

Christian Hochreiter, Fraunhofer EMFT

Abstract: Antibiotics are one of the most important therapeutic inventions in all medical history, so far saving millions of lives per year, reducing mortality and morbidity. Misuse of antibiotics reduces its efficiency and therefore combating resistance to last-line antibiotics in the EU is a priority (source: European Centre for Disease Prevention and Control - ECDC). Multiple drug resistance (MDR) or multi-resistance is antimicrobial resistance present in various microorganisms against drugs. The most dangerous bacteria are those that resist antibiotics.

Methicillin-resistant Staphylococcus aureus is one of the most frequent causes of antibiotic-resistant healthcare-associated infections worldwide. It is a dangerous bacteria type inducing infections which are difficult to treat in humans. MRSA is especially critical in hospitals, prisons, nursing and care homes where patients with open wounds or weak immune systems are at risk of infections. Typically MRSA progresses substantially within 24 to 48 hours of initial symptoms. After 72 hours MRSA takes hold in human body and become difficult to treat. The population at risk comes from various groups: elderly, diabetics, intravenous drug users, patients in hospitals, hospital personnel and people with weak immune system (e.g. cancer, AIDS, etc.). In the current state of the art, dedicated laboratories are the main diagnosis tool for identifying MRSA infections or outbreaks (usually in the range of 24 hours up to several days due to logistics to ship the samples to dedicated labs).

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In the scope of the European SERENE-IoT Project Fraunhofer EMFT, together with SGS TÜV, KUM, XFAB, Flavia-IT, STMicroelectronics, have developed an MRSA detector, whose form factor will be showcased to the attendees with a complementary poster to inform about the project and the contributions.

REFERENCE (ECSEL JU) Project, LMV-based WakeUp-Receiver Frontend in 22FDX

Thomas Thönes, Frank Oehler, Heinrich Milosiu, Gralf Popken, Markus Eppel, Dieter Frühsorger, Johan Tsayem, Fraunhofer IIS

Abstract: Modern fully-depleted SOI silicon technologies (FD-SOI) show important properties such as inherent low-leakage currents, high transit frequencies and a wide range of possible operating voltages, making them attractive for battery-operated applications in the emerging Internet-of-Things (IoT). In the REFERENCE EU research project, Fraunhofer IIS developed the main RF components necessary for an ultra-low-power WakeUp receiver in 22-FDX technology from GLOBALFOUNDRIES. Targeting an average power consumption of below 1 µW at very low latencies in the range of milliseconds, the goal is to push the lower boundaries of energy-efficient receiver design.

B2L-A / Analog-to-Digital & Digital-to-Analog Converters Session

Tuesday, June 25th
1:30 pm - 3:00 pm

Room A

Chair: Harald Pretl

A 0.8 V Low-Power 3rd Order Sigma-Delta Modulator in 22 nm FDSOI CMOS Process for Sensor Interfaces

Pragoti Pran Bora, David Borggreve, Frank Vanselow, Erkan Isa, Linus Maurer

Abstract: We present the design of a low-power 3rd order sigma-delta (∑Δ) modulator targeted for sensor applications. The circuit is implemented in the 22 nm Fully Depleted Silicon on Insulator (FDSOI) CMOS process technology from GlobalFoundries. The modulator features a single-loop feed-forward architecture. Low-voltage operation of the fully-differential switched-capacitor based modulator is achieved with enhanced bootstrapped switches for highly linear sampling, and operational transconductance amplifiers (OTAs) operating in weak inversion. The on-chip area of the modulator is 0.193 mm2. The measurement results show that operating over a signal bandwidth of 500 Hz at a nominal supply voltage of 0.8 V and a sampling rate of 512 kHz, the modulator achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 89 dB and a dynamic range of 94 dB. The total average power consumption of the designed modulator, including that of the auxiliary circuits, is 170 µW.

FIR Feedback in Continuous-Time Incremental Sigma-Delta ADCs

Ayman Mohamed, Ayman Sakr, Jens Anders

Abstract: In this paper, we present a new method to include finite-impulse-response (FIR) feedback digital-to-analog

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converters (DACs) in continuous-time (CT) Incremental Sigma-Delta (I-SD) analog-to-digital converters (ADC), which minimizes transient overshoots and thereby maximizes the modulator's stability. More specifically, it can be shown that increasing the number of FIR taps in I-SD feedback DACs could lead to instability or a reduced maximum stable amplitude (MSA), even when using a proper compensation path. However, by presetting the FIR feedback to a voltage close to the input signal, a larger number of FIR taps can be used, increasing the jitter robustness of the CT I-SD. This presetting is achieved using a low resolution Nyquist rate ADC to preset the FIR taps. Moreover, presetting the FIR feedback slightly increases the modulator's MSA and signal-to noise ratio compared to a non-return-to-zero (NRZ) feedback. To validate the proposed presetting approach, a third-order I-SD ADC employing a 12-tap FIR DAC with presetting using a 4-bit flash ADC is compared against a conventional NRZ DAC and a conventional FIR DAC without presetting in MATLAB/Simulink.

A Novel Offset and 1/F Noise Compensated Single-Slope ADC with Reduced Hardware Effort

Lukas Straczek, Furkan Ercan, Jürgen Oehm

Abstract: Process, voltage, temperature variations (PVT), and noise typically influence the conversion accuracy of an ADC. This work presents a new modular concept for reducing offset, 1/f-noise, and slope errors in single slope analog-to-digital converters (ADCs), advantageously applicable in array structures. The proposed concept combines some analog methods known from chopper amplifier techniques with numerical arithmetics at minimal hardware effort. To increase the conversion speed, an extended concept is proposed, where the converted data are automatically corrected in time after each conversion cycle. Since the ramp generator is also susceptible to PVT fluctuations, the proposed ADC concept can be extended by some calibration options using a bandgap voltage reference. For this work the data of a 180 nm CMOS technology was base and the functionality was verified by nominal and statistical simulations. Index Terms—CMOS, microelectrode array, MEA, single slope ADC, PVT, offset calibration, 1/f-noise cancelation, chopper techniques, numerical fast in-time correction.

A Tri-Level Current-Steering DAC Design with Improved Output-Impedance Related Dynamic Performance

Shantanu Mehta, Anthony G. Scanlan, Brendan Mullane, Daniel O'Hare

Abstract: This paper presents a design of a low-latency 12-bit linear tri-level current-steering digital-to-analogue-converter for use in continuous-time ADCs. The DAC design achieves 12-bit static linearity, while the combination of DAC slice impedance matching with a proposed compensation technique reduces output-impedance related distortion. The technique demonstrates ~10 dB improvement in DAC dynamic performance at high frequencies over the Nyquist-band at 100MS/s. The DAC has been verified by simulation results in TSMC 1.2 V 65 nm CMOS technology.

Self-Calibrating Digital-to-Time Converter in CMOS for Advanced Control in Smart Gate Drivers

Eva Schulte Bocholt, Leo Rolff, Ralf Wunderlich, Stefan Heinen

Abstract: The proposed self-calibrating digital-to-time converter achieves a time resolution of less than 250 ps, consuming less than 0.2 mW of power when constantly activated. Thereby, the necessary timing resolution and range is achieved, that enables soft switching of power MOSFETs and SiC devices and can further increases the switching performance of IGBT.

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B2L-B / Neural Networks Session

Tuesday, June 24th
1:30 pm - 3:00 pm

Room B
Chair: Nima TaheriNejad

MoNA: Mobile Neural Architecture with Reconfigurable Parallel Dimensions

Weiwei Wu, Shouyi Yin, Fengbin Tu, Leibo Liu, Shaojun Wei

Abstract: We propose an architecture called MoNA (mobile neural architecture) for mobile DNNs acceleration. The dataflow of MoNA, with reconfigurable parallel processing dimensions, can help to avoid reduction of PE utilization when processing DW and PW layers.The computing core supports three different kinds of parallel processing dimensions, with reduced bandwidth requirement. The experimental results exhibit the high performance of MoNA when processing mobile DNNs.

Synthesis of Approximate Logic on Memristive Crossbars

Salman Khokhar, Amad Hassen

Abstract: The realization of extremely low power compact devices is critical for ubiquitous computing. In that context, approximate computing is one approach towards improving computing efficiency in error-tolerant applications that may endure a small loss in accuracy in exchange for better efficiency. In this paper, we present a framework for automated synthesis of crossbar designs that implement approximate versions of compute kernels using flow-based computing. We propose Approximate Free Binary Decision Diagrams (AFBDDs) using a relaxed function equality criterion in node merging. We create AFBDD representations of kernels which are then mapped onto crossbars. These crossbars can compute an approximation of the original compute kernel. Our framework allows us to easily tune the accuracy-efficiency trade-off for an approximate design. We generate designs for RevLib and MCNC benchmarks, and basic image processing kernels. Our designs are up to 80% more compact than exact designs while retaining ~90% accuracy.

Efficient Hardware Implementation of Incremental Learning and Inference on Chip

Ghouthi Boukli Hacene, Vincent Gripon, Nicolas Farrugia, Matthieu Arzel, Michel Jezequel

Abstract: In this paper, we tackle the problem of incrementally learning a classifier, one example at a time, directly on chip. To this end we propose an efficient hardware implementation of a recently introduced incremental learning procedure that achieves state-of-the-art performance by combining transfer learning with majority votes and quantization techniques. The proposed design is able to accommodate for both new examples and new classes directly on the chip. We detail the hardware implementation of the method (implemented on FPGA target) and show it requires limited resources while providing a significant acceleration compared to using a CPU.

Exploring the Training and Execution Acceleration of a Neural Network in a Reconfigurable General-Purpose Processor for Embedded Systems

Grégory C. Marchesan, Everton Carara, Marcelo S. Zanetti, Leonardo Oliveira

Abstract: Neural networks are getting more and more present in our daily lives. Whether to classify, optimize, or predict results, the use of neural networks proves to be a great and powerful choice to solve these situations. However, the time spent in the training process can be an issue. Although it can be accelerated by GPUs (Graphics Processing Units), coprocessors or even FPGAs (Field Programmable Gate Array), these approaches may not be the best choices to improve training performance in embedded systems due to the large area and power consumption. In

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this paper, we present a customized instruction set architecture with fixed-point math considering a lightweight general purpose processor in order to accelerate the training and execution of neural networks. Cadence LX7 Processor and Xtensa software are used to identify hotspots and optimize specific pieces of hardware. Experimental results show that our proposed architecture achieves about 25X runtime reduction with regard to a floating-point implementation. The obtained results are also comparable to an Intel Core i7 execution.

Cryptography by Synchronization of Hopfield Neural Networks That Simulate Chaotic Signals Generated by the Human Body

Elias de Almeida Ramos, João Carlos Britto Filho, Ricardo Reis

Abstract: In this work, an asymmetric cryptography method for information security was developed inspired by the fact that the human body generates chaotic signals, where these signals can be used to create sequences of random numbers. Encryption was implemented in a Reconfigurable Hardware (FPGA). To encode and decode the image, the chaotic synchronisation between two dynamic systems, such as Hopfield neural networks (HNNs), was used to simulate the chaotic signals. The notion of Homotopy, an argument of topological nature, was used for the synchronisation. The experiment showed efficiency compared to state of the art in terms of image correlation, histogram analysis and hardware implementation.

B3L-A / Power Amplifiers: Design, Modeling & Optimization Session

Tuesday, June 25th
3:30 pm - 5:00 pm

Room A

Chair: Thierry Taris

New Analytical Boundary Condition for Optimized Outphasing PA Design

Joe Bachi, Ayssar Serhan, Dang-Kièn Germain Pham, Patricia Desgreys, Alexandre Giry

Abstract: A novel analytical approach is used to determine a new boundary condition for optimal operation of a class B Chireix outphasing PA. In the proposed method, a threshold outphasing angle is defined as a new design parameter and used to optimize the power stage in an outphasing system.

An Ultra-Broad-Band Low-Distortion High-Efficiency Class-D Power Amplifier in 130 nm CMOS Technology

Ahmed Mamdouh, Mohamed Aboudina, Faisal Hussien, Ahmed N. Mohieldin

Abstract: This paper presents a novel design of an ultra-broadband class-D power amplifier (PA). The proposed architecture is based on the concept of the ripple buck converter after employing some modifications to facilitate supporting bandwidths up to tens of MHz. The input frequency range covered using the proposed class-D PA is from 0.5 MHz up to 30 MHz. A wide-band transformer has been used to convert the differential outputs of the class-D PA to single-ended load. The design has been implemented and fabricated using a CMOS 0.13 µm technology. It occupies an active area of 0.836 mm^2 and operates from a single 1.2 V supply. The measurement results validates the func-

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tionality of the proposed class-D PA with good linearity and peak efficiency of 58% at 140mW of output power. This has been achieved using few offchip passive components.

Optimization of a Pruned 2-D Digital Predistortion Model Structure for Power Amplifiers Linearization

Siqi Wang, Morgan Roger, Caroline Lelandais-Perrault

Abstract: Two-dimensional digital predistortion (2-D DPD) is one of the most commonly used approach to linearize the concurrent dual-band radio frequency (RF) power amplifiers (PA). This paper explores the use of a hill-climbing optimization heuristic to determine the optimal structure for 2-D DPD. To improve convergence and reduce computation time, we propose a new parameterization for the 2-D DPD model. The proposed search criterion is based on the generalized information criterion, which represents the trade-off between the DPD linearization accuracy in both bands and the model complexity. A comparison against a compressed-sensing-based method is also made. The effectiveness of the proposed method is validated with two 20~MHz long-term-evolution (LTE) signals on two carriers with 100~MHz frequency separation.

Nonlinearity Modeling of Chireix Outphasing Power Combiner Under Amplitude Imbalance

Pavel Afanasyev, Prasidh Ramabadran, Ronan Farrell, John Dooley

Abstract: This work proposes a concise standalone model for Chireix power combiner. The model is based on the analysis of the nonlinear behaviour of a Chireix power combiner under amplitude imbalance. The generalised equations for input impedance of Chireix combiner branches excited by signals with different amplitudes have been derived. The results predicted by the model were validated using both commercial high frequency circuit simulations and experimentally measured results. As a result the proposed model serves two purposes. For one it can be used directly in a larger circuit simulation to predict the performance of an outphasing power amplifier. It can also be used as the basis for a linearization strategy for outphasing power amplifiers.

CMOS Amplifier Design Based on Extended gm/ID Methodology

Amin Aghighi, Jacob Atkinson, Nickolas Bybee, Stuart Anderson, Mitchel Crane, Anthony Bailey, Reuben Morell, Ahmed Hassanin, Armin Tajalli

Abstract: A methodology to optimally design CMOS amplifier stages is described. Unlike conventional methods, which are based on an iterative approach, a closed form solution is proposed. The optimal device operating conditions are directly calculated from design constraints (e.g. voltage gain, and bandwidth). The proposed analytical approach enables implementing accurate and fast optimization algorithms to speed up the design procedure. Design examples are provided illustrating the results of the proposed analysis and optimization methodology.

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B3L-B / SPECIAL SESSION: Rapid Design Tools and Methodologies Session

Tuesday, June 25th
3:30 pm - 5:00 pm

Room B
Chair: Yves Leduc

Virtuoso CurvyCore Infrastructure for Curvilinear Layout Design

presentation only

Janez Jaklic, Cadence

Abstract: Tools for the physical design of microelectronic devices are generally based on the polygonal representation of the layout. This is becoming increasingly inadequate in design applications requiring curvilinear layout, such as photonics, MEMS, microfluidics and conformal routing. The new CurvyCore infrastructure integrated in Virtuoso overcomes this limitation by using the representation or the layout by parametric curves in symbolic mathematical form. This allows operations on the layout to be performed with maximum numerical precision or even analytically, requiring discretization to polygons in the OA database only for display and manufacturing output. This presentation will give an overview of the CurvyCore architecture and the application of the methods it provides for discretization, Boolean operations, offsetting, smoothing and physical verification of curvilinear layouts.

Power-Gating Models for Rapid Design Exploration

Dustin Peterson, Oliver Bringmann

Abstract: Power gating (PG) is an effective method to reduce leakage currents in an SoC design during run-time. It dynamically shuts down components using a network of sleep transistors, but requires a detailed analysis to scale this network appropriately with respect to area, wake-up time, in-rush currents, voltage drops and transition energies. In this paper, we present a method to efficiently determine these key parameters for any SoC design and sleep transistor network at gate-level to enable the rapid exploration of power design alternatives while providing sufficient accuracy for high-level design exploration. Compared to SPICE our approach achieves a speed-up of up to 11457x for two ISCAS circuits, a 32-bit multiplier and a RISC-V core, each build for a 90 nm PDK. The average error compared to SPICE is 2.6% for peak current and 10% for wake-up energy and delay.

Designing Mixed-Signal PLLs Regarding Multiple Requirements Taking Non-Ideal Effects Into Account

Christian Hangmann, Christian Hedayat, Ulrich Hilleringmann

Abstract: This work deals with the efficient characterization and reliable design of mixed-signal (MS) systems like the phaselocked loop (PLL) for frequency synthesis considering non-ideal effects. For the simulation of the PLL and its non-ideal effects an efficient fully event-driven (ED) model is used preceding to a fast and precise system insight. The developed characterization clearly shows that non-ideal effects influence the PLL's dynamic behavior like pull-out range, gain crossover frequency and phase noise behavior. Based on the introduced results a more robust system design is presented, considering multiple requirements. The identified feasible parameter range is also applicable to assess process, voltage and temperature variations.

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Challenges in Statistical Analysis: Yesterday, Today, and Tomorrow

Michael Pronath

Abstract: Verification of custom circuit designs for parametric variation defects has become a must-have procedure for today's nanometer designs. Statistical analysis of circuits poses a challenge because the simulation effort is often high, and the accuracy of some statistical analysis methods is difficult to assess. This paper gives an overview on various approaches to address statistical parametric analysis with respect to their efficiency and reliability.

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B4L-A / Circuits for Wireline Communications Session

Tuesday, June 25th
5:00 pm - 6:30 pm

Room A

Chair: Francois Rivet

ISI Sensitivity of PAM Signaling for Very High-Speed Short-Reach Copper Links

Firat Celik, Ayca Akkaya, Armin Tajalli, Yusuf Leblebici

Abstract: This paper presents a comparative study, analyzing the potentials of pulse amplitude modulation (PAM) for implementing next generation high-speed copper wireline links. This comparative study analyzes the sensitivities of PAM2, PAM4 and PAM8 to inter-symbol interference (ISI), using four different channels (with their loss gradually increased) running at 28 Gb/s, 56 Gb/s, 112 Gb/s and 224 Gb/s. Each case is examined with and without equalization to properly assess the inherent limitations of the modulation schemes in the presence of ISI. This study shows that although higher order PAM offer a better spectral efficiency, this does not translate into the best performance in terms of signal integrity. Depending on the severity of ISI and the data rate, a lower order PAM can outperform a higher order PAM, especially for the low-loss cases.

A 2.8 pJ/Bit 10 Gb/s Delayed-Phase-Select 2-Bit Pulsewidth Modulator in 45-nm SOI CMOS

Sami Ur Rehman, Ali Ferchichi, Mohammad Mahdi Khafaji, Corrado Carta, Frank Ellinger

Abstract: This paper presents the design and characterization of a low output jitter and high resolution pulsewidth modulator in 45-nm SOI CMOS. The modulator uses a current mode logic (CML) delay line to generate delayed phases of a reference signal. A digital input vector selects a particular delayed phase inside a CML phase selector. The delayed

and undelayed phases of the reference are then combined inside a CML OR gate to generate different pulsewidths. The designed 2-bit 10 Gb/s CML pulsewidth modulator offers the highest time resolution of 10 ps, least output jitter of 0.6 ps, and among the best energy figures of 2.8 pJ/bit in comparison to the reported pulsewidth modulators.

A 0.93 pJ/Bit Controlled Capacitor-Charge 2-Bit Pulsewidth Demodulator in 45-nm RFSOI CMOS

Sami Ur Rehman, Mohammad Mahdi Khafaji, Ali Ferchichi, Corrado Carta, Frank Ellinger

Abstract: This paper presents the design and characterization of a unique low-power pulsewidth demodulator (PWDM) which works by controlling the total amount

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of charge stored on a capacitor. The proposed PWDM consists of a time-to-voltage converter (TVC) and a flash architecture based 2-bit analog-todigital converter (ADC). The TVC operates in two phases: the charge phase and the discharge phase. During the charge phase an input pulsewidth-modulated (PWM) signal charges a capacitor to a certain value. The larger the width of the PWM signal, the higher the voltage developed across the charged capacitor. This capacitor voltage, which is unique to each pulsewidth, is then digitized inside a 2-bit ADC. During the discharge phase, the capacitor is allowed to completely discharge to ground. Designed in the 45-nm RFSOI CMOS, the PWDM occupies an active area of 70×80 μm^2, achieves data rates upto 8 Gb/s, and dissipates only 7.25 mW of power. To the best of the authors' knowledge, the proposed PWDM offers the best energy figure compared to the existing pulsewidth demodulator designs.

A 34-fJ/Bit 20-Gb/s 1/8-Rate Charge-Steering DFE for IoT Applications

Marco Saif, Khaled Hassan, Ahmed Abdelati, Sameh Ibrahim

Abstract: The need for equalization in the receivers of wireline communication systems has increased with the large increase in data rates. There are two main categories for equalizers; Continuous Time Linear Equalizer (CTLE) and non-linear equalizer implemented as Decision Feedback Equalizer (DFE). Most DFEs use half-rate or quarter-rate architectures meanwhile, this paper uses 1/8-rate architecture to relax the timing constraint and reduce power consumption. This paper presents the design of a 1-tap 20-Gb/s charge-steering 1/8-rate DFE in a 65-nm CMOS technology. The proposed DFE consumes 0.68-mW from a 1-V supply and compensates for 7-dB channel loss when processing 20-Gb/s data.

Data-Transition Decision Feedback Equalizer with Edge-Emphasis Taps and Raised References

Yue Li, Fei Yuan

Abstract: This paper presents an adaptive data-transition decision feedback equalizer (DT-DFE) with edge-emphasis (EE) taps and raised reference voltages. The distinct characteristics of data-state (DS) DFE and DT-DFE are examined first. It is followed with an introduction of DT-DFE with EE-taps. We show that the proposed DFE is capable of improving the edges and vertical eye-opening of equalized data. We further show that the proposed DFE is capable of raising reference voltages to desired values so as to improve vertical eye-opening. The details of the design of the DFE are provided. The effectiveness of the proposed DFE is validated using a 10 Gbps backplane link. Simulation results show that the DFE is capable of sharpening data edges by 3.28 times, lowering data jitter by 3.36 times, and improving vertical eye-opening by 3.7 times.

B4L-B / SPECIAL SESSION: Security of Systems and Cryptographic Circuits Session

Tuesday, June 25th
5:00 pm - 6:50 pm

Room B
Chair: Oliver Bringmann

Random Number Generator Based on Micro-Scale Bio-Electrochemical Cell System

Celal Erbay, Salih Ergün

Abstract: Random number generators (RNG) are essential components for security system. RNGs are used in sensitive applications such as key generation and challenge-response based authentication. Therefore, ensuring the unpredictability of the generated bits is very important to keep the all system in safe. This paper presents RNG based on micro-scale bio-electrochemical cell system that provides alternative way of producing random bit streams. The system here is fabricated by using photolithography process and the main purpose of the micro device is analyzing the activity of micro-organism that produces electrons to generate power. We use the randomly produced voltage value over time to generate strong random numbers which are successfully passed the NIST 800-22 statistical randomness tests after SHA-224 hash algorithm post-processing method. This alternative method ensures secure data transfer where bio-electrochemical cell system needs to be used such as environmental protection sensor networks, vehicles power by bio-electrochemical cell system, and portable electronic devices.

On the Confidence in Bit-Alias Measurement of Physical Unclonable Functions

Florian Wilde, Michael Pehl

Abstract: Physical Unclonable Functions (PUFs) are modern solutions for cheap and secure key storage. The security level strongly depends on a PUF's unpredictability, which is impaired if certain bits of the PUF response tend towards the same value on all devices. The expectation for the probability of 1 at some position in the response, the Bit-Alias, is a state-of-the-art metric in this regard. However, the confidence interval of the Bit-Alias is never considered, which can lead to an overestimation of a PUF's unpredictability. Moreover, no tool is available to verify if the Bit-Alias is within given limits. This work adapts a method for the calculation of confidence intervals to Bit-Alias. It further proposes a statistical hypothesis test to verify if a PUF design meets given specifications on Bit-Alias or bit-wise entropy. Application to several published PUF designs demonstrates the methods' capabilities. The results prove the need for a high number of samples when the unpredictability of PUFs is tested. The proposed methods are publicly available and should improve the design and evaluation of PUFs in the future.

Fault Attacks on Cryptographic Circuits

Ilia Polian

Abstract: Fault-injection attacks on cryptographic circuits are physical manipulations applied by an adversary during the circuit's operation with the purpose of extracting sensitive information, such as secret key bits. Fault attacks gain in relevance for cyberphysical applications and autonomous systems, where the system's hardware is naturally exposed to a potential attacker. This paper will provide an introduction into fault attacks, give an overview of fault-injection techniques and known countermeasures, and point out new research directions in this area.

Estimating the Unknown Parameters of a Random Number Generator Based on a Chaotic Jerk System

Salih Ergün

Abstract: A novel estimating system is proposed to find out the security weaknesses of a random number generator

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(RNG) based on a chaotic jerk system. Convergence of the estimating system is proved using auto-synchronization. Unknown parameter of the target RNG is revealed where the public information are the design of the RNG and a scalar time series observed from the target chaotic jerk system. Simulation and numerical results verifying the feasibility of the estimating system are given such that, next bit can be predicted while the same output bit sequence of the RNG can be regenerated.

Analysis of Random Number Generators Based on Fibonacci-Galois Ring Oscillators

Kaya Demir, Salih Ergün

Abstract: This paper presents the analysis of random number generators(RNGs) based on regular sampling of irregular waveform method where the irregular signal is obtained from the oscillations of combined Fibonacci and Galois ring oscillators. As the proposed random number generator is made up of logic gates only, it is implemented on a FPGA (field-programmable gate array). The regular waveform generated by the digital clock manager of the FPGA is used for sampling the irregular signal and the resulting bit stream is uploaded to a computer where it is subjected to standard statistical test. The polynomials defining the Fibonacci and Galois ring oscillators are varied to assess the relationship between the polynomial and the randomness of the output bit stream. It is demonstrated that for both polynomial functions, by combining enough number of oscillator structures, the output bit streams from each RNG satisfy standard statistical tests without post processing. To the best of our knowledge, this paper presents the first comparative study on the impact of polynomials on random number generators based on Fibonacci and Galois ring oscillators.

Idols with Feet of Clay: on the Security of Bootloaders and Firmware Updaters for the IoT

Lionel Morel, Damien Couroussé

Abstract: IoT devices are generally implemented with low- cost embedded solutions, and connectivity and communication capabilities are the raison d'être of such devices. But this is a double-edged sword, since connectivity also implies (1) to open the door to more attack possibilities, and (2) the targeted system, once breached, can be the support for attacks at a larger scale, possibly involving many connected systems. In this paper, we provide an overview of the threats targeting Bootloaders and Firmware Upgrades, and existing protections. We argue that vulnerabilities to physical attacks, in particular to fault injection attacks, are mostly left un-attended.

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C1L-A / Analog to Digital Converters Session

Wednesday, June 26th
10:30 am - 12:00 noon

Room A
Chair: Elena Blokhina

Multi-Step Capacitor Switching Scheme for Low-Power SAR ADC

Aleksandr Gusev, Dmitry Osipov, Steffen Paul

Abstract: A new multi-step monotonic switching SAR ADC architecture was proposed. The paper describes a method to improve energy savings of conventional monotonic switching SAR ADC architecture by adding 2^n voltage-steps per capacitor switching. Modified step-down switched capacitor DC-DC converter for generation of voltage steps between reference and ground was also described. Multi-step monotonic switching provides increased power efficiency of capacitive DAC in 10-bit SAR ADC of up to 66% compared to 1-step monotonic switching architecture without consideration of DC/DC conversion influence. Energy savings with considered influence of proposed switched-capacitor DC/DC converter are approximately 50%.

A 300MS/s 10bit SAR with Loop-Embedded Input Buffer for a Photonic System

Leonhard Klein, Antonios Nikas, Bijoy Kundu, Matthias Voelker

Abstract: This work presents a 300 MS/s 10bit successive approximation analog to digital converter (SAR-ADC). It is designed in a 180nm technology suitable for co-integration with a photonic system. The ADC employs a loop embedded input buffer to reduce its input capacitance. A current steering DAC is implemented to eliminate kickback to the reference voltage. The proposed topology is independent of the input common mode voltage and thus enables the use

of the current steering DAC. The implementation provides a low input capacitance of 386fF and suppresses nonlinearities from the buffer due to input common mode variations.

First Order Fully Passive Noise-Shaping SAR ADC Architecture with NTF Zero Close to One

Dmitry Osipov, Aleksandr Gusev, Steffen Paul

Abstract: A new noise-shaping architecture for successive approximation register (SAR) analog-to-digital converters (ADCs) was proposed. It does not require comparator modification, so the standard comparator can be used. A first-order noise transfer function with zero located nearly at one can be achieved. This allows the use of higher over sampling ratios (OSR) and increased effective number of bits (ENOB). The architecture is fully passive. The architecture was applied to the design of a 9.9-bit ENOB SAR ADC in a 65 nm complementary metal-oxide semiconductor (CMOS) of United Microelectronics Corporation (UMC) with OSR equal to 10. A 6-bit DAC was used. The proposed architecture provides 3.9 additional bits in ENOB. Signal-to-noise and distortion ratio (SINAD) of 61.4 dBFS was achieved according to simulation results for a signal bandwith of 200 kHz with sampling rate of 4 MS/s.

A 0.0053-mm² 6-Bit Fully-Standard-Cell-Based Synthesizable SAR ADC in 65 nm CMOS

Naoki Ojima, Zule Xu, Tetsuya Iizuka

Abstract: This paper proposes an all-standard-cell synthesizable successive approximation register analog to digital converter (SAR ADC) that consists of only standard cells. In this SAR ADC, analog components such as resistive digital to analog converters (RDAC), a four-input clocked comparator, and track and hold (T/H) circuits are fully implemented with standard cells. The layout of analog components is implemented with automatic place and route, which drastically relaxes the design burden and time. The 6-bit resolution prototype is fabricated in a 65 nm standard CMOS technology with 0:0053 mm² area occupation. The measurement

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results show that SNDR and SFDR is 28:1 dB and 32:5 dB respectively, at a 10 MS/s and 4:99 MHz sinusoidal input.

An UWB 18.5 GS/s Sampling Front-End for a 74 GS/s 5-Bit ADC in 22 nm FDSOI

Nima Lotfi, Friedel Gerfers

Abstract: This paper presents the design of a single channel front-end sampler operating at 18.5 GS/s. The sampler, which is designed for a 5-bit 4X time-interleaved (TI) flash ADC (fs=74 GS/s), is designed in 22 nm FDSOI. It comprises a low jitter limiting amplifier and clock buffer in the clock path, PMOS source follower and PMOS only sampling switches and a pair of NMOS source followers to buffer the track and hold from the flash comparator array and enhance the effective sampling bandwidth. The sampling channel has a differential input range of 600 mVp-p and uses a 0.9 V supply for the clock domain and 1.2 V supply for the source followers. The Simulation results over different process corners showed a total sampling bandwidth of 40 GHz at the worst corner(SS, T=120), while it achieves a SFDR and SNDR of better than 41 dBc and 38dB respectively at the fourth Nyquist zone (fin=37 GHz). The total power consumption including the clock buffers (10 mW) is 75 mW.

C1L-B / Biomedical Circuits & Systems Session

Wednesday, June 26th
10:30 am - 12:00 noon

Room B

Chairs: Franck Badets, Mohamad Sawan

Pseudo-Continuous Flow System for Dopamine and Ascorbic Acid Detection Based on FTIR-Spectrometery

Hamza Landari, Mourad Roudjane, Younès Messaddeq, Amine Miled

Abstract: In this work a new protocol based on FTIR-microspectrometry and solvent evaporation for neurotransmitter detection is presented. In addition, a new automated sample handle support is developed and coupled to the microscope-FTIR in order to perform Dopamine and Ascorbic Acid sensing in aqueous solutions. Results show that these molecules can be detected in homogeneous and mixture samples with different ratios of concentrations (Dopamine/Ascorbic Acid) varying from 4 to 0.25. Achieved limits of detection was 3 µM and 5 µM for Dopamine and Ascorbic Acid respectively with this system configuration.

Using Meta-Heuristic Optimization to Extract Bio-Impedance Parameters from an Oscillator Circuit

Menna Mohsen, Lobna Said, Ahmed Madian, Ahmed Elwakil, Ahmed G. Radwan

Abstract: This paper introduces a method for extracting the Cole-impedance model parameters using a meta-heuristic optimization technique. The method is based on a proposed single resistor controlled oscillator (SRCO) where the unknown bioimpedance is embedded. At two different oscillation frequencies, the start-up oscillation condition is recorded and then the corresponding nonlinear equations are solved using the flower pollination optimization (FPA) technique to

Abstracts

find the optimum impedance parameters that minimize an objective error function. Experimental results are provided and comparisons with model parameters extracted using standard Impedance Spectroscopy are shown.

Design and Validation of a Six-Antenna WPT System with Tracking Capabilites for Biomedical Devices

Hugo Dinis, Ivo Colmiais, Paulo Mendes

Abstract: This paper presents a 2 GHz RF WPT system capable of tracking an implantable device and maximizing the amount of power transferred to it along its path. Measurements and simulations were performed to validate the system, and the use of tracking increased the amount of available power for the implant along its path in all the studied points comparatively to the scenario where no tracking was used. This technology presents itself as a promising stepping stone towards battery-less implantable medical devices.

High-Efficiency LED Driver for Short Fluorophores Lifetime Biosensing Applications

Isam Gharib, Mohamad Sawan

Abstract: We present in this work a high speed light emitting diode (LED) driver for nanosecond fluorescence lifetime measurements. Fluorescence-based sensing is widely used in both chemical and biological microscopies due to its high sensitivity, selectivity and reliability. The challenge of this technique is that most fluorophores have lifetimes in the order of nanoseconds, which requires very-fast excitation and detection systems. To achieve needed speed, a novel LED driver is proposed to deliver short pulse excitation by reducing significantly the optical fall time. The simulated results provide fall time of light pulses as short as 1.6 ns.

C2L-A / Frequency Synthesis Circuits & Building Blocks Session

Wednesday, June 26th
1:30 pm - 3:00 pm

Room A

Chairs: Elena Blokhina, Wessam Ajib

A 22-29 GHz Voltage-Biased LC-VCO with Suppressed Flicker Noise Over Tuning Range in 22 nm FD-SOI

Zhiwei Zong, Giovanni Mangraviti, Piet Wambacq

Abstract: A 22-29 GHz voltage biased LC-VCO with low 1/f3 corner is proposed in 22nm FD-SOI. Thanks to the use of common centroid layout technique for SCB implementation, a significant flicker noise suppression is achieved throughout the frequency tuning range. In addition, a 2-turn coupled inductor is used for saving area and simplifying the design of decoupling capacitor CD. The post layout simulation shows that the proposed oscillator achieves a 1/f3 corner lower than the state-of-the-art above 20 GHz with a competitive FOMT of 197.2 dBc/Hz at 1MHz offset.

28 GHz Quadrature Frequency Generation Exploiting Injection-Locked Harmonic Extractors for 5G Communications

Zhong Gao, Yizhe Hu, Teerachot Siriburanon, Robert Bogdan Staszewski

Abstract: This paper proposes a mm-wave quadrature frequency generator using injection-locked harmonic extractors (HEs) incorporated with quadrature class-F oscillators. While maintaining high output levels at 28GHz, the utilization of injection locking technique improves the effective quality (Q)-factor and helps to achieve a fundamental harmonic suppression of 60 dB. This results in an FoM of the whole frequency generation system reaching -184 dB.

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The consideration of quadrature phase mismatch induced by electromagnetic coupling between quadrature buffers is also discussed.

A Comparison of Frequency Synthesizers Up to 25 GHz for 130 nm CMOS Implementation

Zakaria El Alaoui Ismaili, Wessam Ajib, François Gagnon, Mounir Boukadoum

Abstract: This paper provides a critical comparison of three frequency synthesizer schemes implemented in 0.13 µm CMOS technology, with the aim to select the best architecture to use given the application specs. The presented architectures can generate carrier frequency bands from a maximum frequency down to any lower frequency. All systems are designed based on 0.13 µm CMOS technology and can reach frequencies up to 25 GHz. We show that the single switched capacitors voltage controlled oscillator (S-VCO) architecture is the best choice for frequencies below 6 GHz, and multiple core VCOs (Multi-VCO) synthesizers show the best performances for frequencies above 16 GHz. On the other hand, the synthesizer equipped with a single side band mixer (SSB-m) is the choice for applications requiring frequencies between 6 GHz and 16 GHz.

A Cell-Based Wide-Frequency-Range DLL Supporting Fast Frequency Scaling

Wei Chu, Shi-Yu Huang

Abstract: In this paper, we present a cell-based wide-frequency- range DLL supporting clock frequencies from 10 MHz to 1 GHz in 90 nm. To support fast locking (during frequency scaling), we present novel architecture with a socalled "fast-locking mode" – in which the control code for the Long-Range Delay Block (LRDB) can be quickly determined in a way that the overall delay across the underlying DLL can be roughly one or multiple clock cycle times of the input clock signal. One can use this LRDB as a common building block and integrate it with any arbitrary narrow-range DLL for DVFS (Dynamic Voltage and Frequency Scaling) applications while achieving fast frequency scaling. The functionality is validated by post-layout simulation using a 90nm CMOS process. With the proposed scheme, the long-range locking time can be reduced significantly from 24% to 98%, respectively, for different input clock frequencies.

All-Digital Phase-Locked Loop Arrays: Investigation of Synchronisation and Jitter Performance Through FPGA Prototyping

Eugene Koskin, Pierre Bisiaux, Dimitri Galayko, Elena Blokhina

Abstract: In this paper, we study the propagation of timing error in a synchronous All-Digital Phase-Locked Loop network. The architecture of the network represents a linear array of oscillators, where the first oscillator is considered as the reference oscillator, and the others are implemented as digitally controlled oscillators. The synchronisation of the network is achieved through interactions between a controlled oscillator and its closest neighbours. Using FPGA prototyping, we have shown that the jitter of a controlled oscillator saturates with the distance from the reference oscillators and that the bidirectional topology has better performance than the unidirectional topology. A comparison of measurements with a theoretical model is carried out to verify our FPGA prototyping framework.

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C2L-B / Analog & Mixed-Signal Circuits Session

Wednesday, June 26th
1:30 pm - 3:00 pm

Room B
Chair: Sylvain Bourdel

An Ultra Low-Power Low-Offset Double-Tail Comparator

Ata Khorami, Roghayeh Saeidi, Mohammad Sharifkhani, Nima Taherinejad

Abstract: In double tail comparators, the pre-amplifier amplifies the input differential voltage and when the output Vcm of the pre-amplifier becomes larger than Vth of the latch input transistors, the latch is activated and finalizes the comparison. As a result, the pre-amplification delay is fixed to a value and cannot be set at the minimum required delay, to save power and improve offset. In fact, when the latch is activated the pre-amplifier output differential voltage is still growing but the latch finishes the comparison before the maximum differential gain is formed and applied to the latch. In this paper, a comparator is proposed in which the pre-amplifier is turned off when the maximum gain is achieved so that always the maximum possible gain is applied to the latch. Therefore, not only the input referred offset is improved but also the power consumption of the pre-amplifier is saved. Simulations in 0.18µm technology show that if an appropriate pre-amplification delay is set, the average power is saved by up to 75% while the offset voltage is reduced by about 30%.

Two-Fold Noise-Cancelling Low-Noise Amplifier in 28-nm CMOS

Amir Bozorg, Robert Bogdan Staszewski

Abstract: In this paper, a low-noise amplifier (LNA) employing across-coupled common-gate stage for wide-band input matching is presented. By applying a two-fold noise cancellation technique, the channel thermal noise of the first stage is removed which improves its noise performance and linearity. We perform a detailed analysis of the transfer function, noise and linearity, which are then verified in simulations in TSMC 28-nm LP CMOS technology. The presented LNA achieves a power gain of 18.9–16 dB within 100 MHz up to 3.7 GHz and the input and output return loss of better than 11 dB. The IIP3 is +2.8 dBm and the noise figure (NF) ranges 1.58–2.4 dB over the band of interest with 24 mW DC power consumption.

Low Complexity Architecture of N-Path Mixers for Low Power Application

Ali Al Shakoush, Estelle Lauga-Larroze, Serge Subias, Thierry Taris, Florence Podevin, Sylvain Bourdel

Abstract: The principle of harmonic rejection in N-Path receiver is first detailed and a generic architecture based representation is given to better analyze the complexity of these structures. Then a proposed structure based on differential effective local signal generation is presented and compared to other ones. The proposed structure can reject up to the 8th harmonic with a comparable complexity of a classical 6 order harmonic rejcetion N-path receiver.

Fractional-Order Asymptotical Phase Shifter with Flat Magnitude Response

Roman Sotner, Lukas Langhammer, Jan Jerabek, Tomas Dostal

Abstract: This work deals with design of fractional-order asymptotical phase shifter having constant magnitude response within almost three decades (100 Hz – 100 kHz) and frequency dependent phase difference going from 0 to -45 degrees. PSpice simulations employing macromodels of off-the-shelf active parts brought the results suitable for brief analysis of the complete solution of our phase shifter in both frequency and time domain. Magnitude flatness with only ±0.3 dB variation and maximal phase error in the

Abstracts

middle of operational bandwidth 3.7 degrees prove very good performance of designed circuit.

A Robust Random Number Generator Based on Chaotic Ring Oscillators

Ibrahim Taştan, Salih Ergün

Abstract: A robust chaos-based random number genertor (RNG) system is newly proposed. Output bitstreams generated from this new RNG system is tested on NIST-800-22 test suite. Proposed RNG circuit fulfill all fifteen randomness tests of NIST- 800-22 without undergoing any post-processing implementations except for the XOR operation. While classical ring oscillator based RNG systems needs at least 25 rings, each of them containing 13 inverters, and 25 D flip-flops to pass all the tests, newly designed RNG system pass all the tests succesfully with 10 chaotic new subcells containig 20 ring oscillators with 13 inverters and each subcell includes two resistors, a capacitor and two diodes. These are enough for the new system to generate sufficient randomness without any D flip-flops.

C3L-A / Wireless Communications Session

Wednesday, June 26th
3:30 pm - 5:00 pm

Room A

Chair: Dominique Morche

A 1.9-µW 7-GHz IR-UWB Transmitter with RF-Energy-Harvester in 180-nm CMOS for Battery-Less Bio-Sensors

Stefan Schmickl, Thomas Faseth, Harald Pretl

Abstract: A fully integrated 802.15.4a-LRP-UWB-PHY- and ETSI-compliant impulse-radio ultra-wide-band (IR-UWB) transmitter (TX) front-end, powered by an RF-energy-harvester in 180nm CMOS technology, is presented. The TX is working in the 7 GHz band transmitting with -42 dBm at 5.12 kbps data rate, consuming 1.89 µW. The RF-energy-harvester is capable of generating 5 µW dc-power at -13.3 dBm RF input power at a frequency of 868 MHz. The harvested energy is sufficient for the IR-UWB-TX front-end, an ADC with pre-amplifier and the digital core logic for a wireless bio-sensing chip.

Enhanced Symbol Synchronization for Multi-User High Reliable Dynamic Industrial Wireless Communication

Mingjie Hao, Ludwig Karsthof, Jochen Rust, Steffen Paul

Abstract: Recently, the wireless communication system development driven by the ongoing Industry 4.0 (I40) and Industrial Internet of Thing (IIoT) has been growing enormously. In industrial automation and manufacturing, closed-loop control applications are commonly used, which require completely new solutions to achieve ultra high reliability and have stringent requirements on message timing and repetitive packet losses. A novel hardware-based enhanced preamble-aided OFDM frame detection and frequency offset

estimation aiming at the high reliability and low packet loss rate is introduced in this work. With the introduced carrier frequency offset estimation, key highlights of our work are a) multi-user support, b) low hardware overhead, and c) lower packet loss rate.

Ultra Low Latency Implementation of Robust Channel Estimation and Equalization for Industrial Wireless Communication Systems

Ludwig Karsthof, Mingjie Hao, Jochen Rust, Steffen Paul

Abstract: In this paper, we propose a robust low latency, low complexity hardware implementation of a channel estimation algorithm. The hardware is designed and validated in an industrial wireless communication system and optimized in terms of area and latency. The algorithm was tested using a standard FPGA-platform and operated at 100 MHz.

CDM-Based 4-Channel Digital Beamforming Transmitter Using a Single DAC

Amit Sangwan, Rui Ma, Bingnan Wang, Kyeong Kim, Kieran Parsons, Toshiaki Koike-Akino, Pu Wang, Phil Orlik, Koon Teo, Kuriyama Tasuku, Kihira Kazunari, Toru Fukasawa

Abstract: In recent years, digital beamforming (DBF) is gain- ing more attention for next generation directional communication systems such as 5G, thanks to its flexibility for beamstearing in both analog- and hybrid-beamforming systems. However,conventional digital beamforming requires the use of independent Digital to Analog converter (DAC) and RF chain for each antenna element, which poses significant challenges in cost, power and heat dissipation. In this work, we present for the first time a novel low-cost solution with reduced hardware complexity in DBF. Digital beamformed multiple baseband signal are to be fed for different antenna elements through a single DAC. We implemented coding schemes in digital baseband domain and successfully decoded and recovered in the analog RF domain. The recovered signals are measured before connected with antenna for proof-of-concept. The demonstrated technique provides cost and size reduction of the array system while keeping the integrity of the signals.

A 15 - 34 GHz Robust GaN Based Low-Noise Amplifier with 0.8dB Minimum Noise Figure

Shiyong Zhang, Penghui Zheng, Jianxing Xu, Rong Wang, Yang Huang, Xiaodong Tong

Abstract: In this report, a broad band (15 GHz to 34 GHz) low noise amplifier (LNA) using 100 nm GaN on silicon technology is designed and fabricated. The LNA shows an extremely low noise figure of 1.2 dB across the bandwidth. The small signal gain is 18.5±1.5 dB. The robustness of the LNA is also tested by applying a 30 dBm continuous-wave (CW) input power at 27 GHz to the working LNA, and no significant degradation is observed.

Abstracts

C3L-B / Circuits for Sensing Applications Session

Wednesday, June 26th
3:30 pm - 5:00 pm

Room B
Chair: Luc Hebrard

Integrated Multipurpose Analog Front-End for Electrochemical ISFET Sensors

Markus Hefele, Ernst Müllner, Ralf Brederlow, Andreas Lösel, Sebastian Meier, Christian Pfeffer, Franz Kreupl, Bernhard Wolf

Abstract: We propose a new circuit for Ion-Sensitive-Field-Effect-Transistors (ISFETs) for pH sensing based on a standard mixed-signal-processor with minimal required external components. The ISFET is controlled by a servo loop in software. The internal ADC is used for feedback. We compare this method with an analog ISFET readout circuit and show their equivalence. The new circuit provides some additional features, such as run time configurable operating point and channel type settings. The integrated MCU can perform calibration and sensor diagnosis functionality and eases the integration in other systems and parallel operation of many units with its digital interfaces.

Wirelessly-Powered Printed Temperature Sensor with an Ultra-Low-Power and High-Sensitivity CMOS Readout IC

Shao-Yung Lu, I-Feng Wu, Ying-Chih Liao, Yu-Te Liao

Abstract: This paper presents a wireless-powering high-sensitivity printed temperature sensor (TS). The proposed system consists of a -17 dBm sensitivity RF-DC conversion circuit, a 2.2 µW readout interface, and a printed NiO thermistor sensor. The 1 mm^2 printed NiO film has a good sensitivity of ~4000 K but has high resistance (~MΩ). Conventional readout system has difficulties to detect the small resistance changes in the large thermal resistance range while only consuming a few µW that is a need for enabling the RF-powering sensors. A low-noise readout IC was designed to convert the resistance changes to digital codes. The proposed TS achieves a resolution of 0.04 oC/code in a temperature range of -20~90 oC and measurement deviation within ±1.1% while only consuming 2.2 nJ per conversion.

A 0.5-V 180-nm CMOS Switched-Capacitor Temperature Sensor with 319 nJ/Measurement

Markus Stadelmayer, Thomas Faseth, Harald Pretl

Abstract: In this paper, an ultra-low-power switched-capacitor temperature sensor realized in a 180 nm CMOS process is introduced and the measurement results are presented. The sensor is operational at supply voltages down to 0.5 V. While bipolar transistors are utilized for reference and temperature dependent voltage generation in a switched-capacitor band-gap core, the overall temperature sensor is formed by a combination of the band-gap and a time-discrete pseudo-differential single-slope analog-to-digital converter. This allows systematic compensation of the temperature dependent common-mode error while utilizing the high accuracy of single-slope architectures and simultaneously improving traditional single slope ADC designs. The temperature sensor has a power consumption of 2.62 uW (4.56 uW) including all biasing at supply voltages of 0.5 V (0.8 V), and achieves an estimated 3 sigma accuracy of 2.42 °C (1.36 °C) using a two-point trim for the wide temperature range of 10 °C to 100 °C (-20 °C to 100 °C). Besides the temperature sensing functionality, the presented circuitry additionally provides a stable clock signal and a reference voltage for other circuit blocks.

Abstracts

A Low-Complex Compressive Sensing Based Thermal Sensor Placement for Multicore Systems

Kun-Chih Chen, Hsueh-Wen Tang

Abstract: In this paper, we propose a low-complex CS-based thermal sensor placement for the multicore system. Firstly, we divide the chip into several equally sized grid blocks and randomly place the number-limited thermal sensors on the grid blocks. Afterward, we adopt the MIB property to propose a MIB-based OMP to estimate the full-chip temperature distribution with low computational complexity. The experimental results show that we can reduce 52% average full-system temperature reconst-ruction error compared with the previous non-CS-based approaches. Besides, we can reduce 22% - 27% calculation time compared with the current CS-based temperature reconstruction algorithm.

Inductive Locating Method to Locate Miniatu-rized Wireless Sensors Within Inhomogeneous Dielectrics

Sven Lange, Dominik Schröder, Christian Hedayat, Thomas Otto, Ulrich Hilleringmann

Abstract: For the measurement of process data in bioreactors, very small wireless sensors are currently under development to replace the conventional rod probes. The so-called Sens-o-Spheres measure the temperature and in future the oxygen content and the pH of fluids. In order to evaluate the distribution of the measured values within the process, it is necessary to locate the wireless sensors. Because of the small size of the sphere (diameter 8 mm), inhomogeneous ambient media and the size of the reactor (less than 2 m), an inductive locating by magnetic fields with a frequency of f=13.56 MHz is necessary.

Silver Sponsor

Sunday, June 23rd

Fraunhofer EMFT, Hansastrasse 27d, 80686 Munich

	T1	T2	T3
8:00			
8:30	Registration		
9:00	**Systematic design of low-power Analog/RF CMOS circuits using the Inversion Coefficient** Prof. Christian Enz, EPFL, Switzerland Prof. Willy Sansen, KU Leuven, The Netherlands	**Spread-spectrum techniques for mitigation of inband jammers in RF transceivers** Prof. Ramesh Harjani, University of Minnesota, USA	**An Efficient Solution to Simulate Mixed-Signal Circuits in C** Dr. Yves Leduc, Associate Member Polytech Lab, University of Nice Sophia-Anipolis, France
9:30			
10:00			
10:30			
11:00			
11:30			
12:00			
12:30	Lunch break		
13:00			
13:30			
14:00	**T4** **Amplifier Efficiency vs. Linearity: What physics does and does not allow?** Prof. Dr. Earl McCune, TU Delft, Netherlands Prof. Thierry Taris, University of Bordeaux, France	**T5** **Things you always wanted to know about the bioelectricity of living cells and their marriage with electronics – but never dared to study** Prof. Joachim Wegener, Fraunhofer EMFT, Prof. Sven Ingebrandt, RWTH Aachen, Germany	**T6** **Design and Mitigation methodologies of COTS FPGAs for Aerospace Missions** Assoc. Prof. Luca Sterpone, Politecnico die Torino, Italy
14:30			
15:00			
15:30			
16:00			
16:30			
17:00			
17:30	Individual Transfer to the Conference Venue Hilton Munich Park, Am Tucherpark 7, 80538 Munich		
18:00			
18:30			
19:00			

Monday, June 24th

Hilton Munich Park

8:00	Registration	
8:30	Opening Ceremony	
9:00	**Keynote** **Quantum Computing: From Curiosity to First Useful Applications** Dr. Alessandro Curioni Vice President Europe & Director IBM Research, Switzerland	
9:30		
10:00	Coffee break	
10:30	**A1L-A** **Neuromorphic Circuits & Neural Networks** **(5 papers)**	**A1L-B** **Robust & Reliable Circuit Design** **(5 papers)**
11:00		
11:30		
12:00	Lunch break	
12:30		
13:00		
13:30	SPECIAL SESSION SOI Ecosystem for 5G	
14:00		
14:30		
15:00	Coffee break	
15:30	**A2L-A** **SPECIAL SESSION: SOI based RF and mm-wave Design** **(3 papers + 2 presentations)**	**A2L-B** **Efficient Image & Video Processing** **(5 papers)**
16:00		
16:30		
17:00	**A3L-A** **SPECIAL SESSION: 5G and beyond: from Material to Systems** **(4 papers + 1 presentation)**	**A3L-B** **Digital Circuits & Designs for Digital Systems** **(5 papers)**
17:30		
18:00		
18:30	Welcome Event IEEE NEWCAS 2019 Hofbräuhaus Munich	
19:00		

by 22:00

Tuesday, June 25th

Hilton Munich Park

8:00		
8:30	**Registration**	
9:00	**Keynote**	
9:30	**Mixed-Signal Techniques for Embedded Machine Learning Systems** Professor Boris Murmann Stanford University, USA	
10:00	**Keynote**	
10:30	**Tiny AI – how sensors become truly smart** Wolfgang Furtner Infineon AG, Munich, Germany	
11:00	**B1P-C**	
11:30	**Posters (13 papers), Project Demos & Coffee**	
12:00	**Lunch break**	
12:30		
13:00		
13:30	**B2L-A**	**B2L-B**
14:00	**Analog-to-Digital & Digital-to-Analog Converters** **(5 papers)**	**Neural Networks** **(5 papers)**
14:30		
15:00	**Coffee break**	
15:30	**B3L-A**	**B3L-B**
16:00	**Power Amplifiers: Design, Modeling & Optimization** **(5 papers)**	**SPECIAL SESSION: Rapid Design Tools and Methodologies** **(3 papers + 1 presentation)**
16:30		
17:00	**B4L-A**	**B4L-B**
17:30	**Circuits for Wireline Communications** **(5 papers)**	**SPECIAL SESSION: Security of Systems and Cryptographic Circuits** **(6 papers)**
18:00		
18:30	**Networking Reception IEEE NEWCAS 2019**	
19:00	**Hilton Munich Park**	

by 21:30

Wednesday, June 26th

Hilton Munich Park

8:00		
8:30	**Registration**	
9:00	**Keynote**	
9:30	**Kalray's MPPA® Manycore Processor: At the Heart of Intelligent Systems** Dr. Benoît Dupont de Dinechin, CTO, Kalray , France	
10:00	**Coffee break**	
10:30	**C1L-A**	**C1L-B**
11:00	**Analog to Digital Converters** **(5 papers)**	**Biomedical Circuits & Systems** **(4 papers)**
11:30		
12:00	**Lunch break**	
12:30		
13:00		
13:30	**C2L-A**	**C2L-B**
14:00	**Frequency Synthesis Circuits & Building Blocks** **(5 papers)**	**Analog & Mixed-Signal Circuits** **(5 papers)**
14:30		
15:00	**Coffee break**	
15:30	**C3L-A**	**C3L-B**
16:00	**Wireless Communications** **(5 papers)**	**Circuits for Sensing Applications** **(5 papers)**
16:30		
17:00	**Best Students' Paper & Poster Awards** **Closing Ceremony & See you at NEWCAS 2020**	
17:30