Fast Macromodel-based Signal Integrity Assessment for RF and Mixed-Signal Modules

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S. Grivet-Talocia*, P. Brenner§, and F. G. Canavero*
*Politecnico di Torino, Dip. Elettronica, Torino, Italy. E-mail: stefano.grivet@polito.it
§Infineon Technologies AG, Germany. E-mail: pietro.brenner@infineon.com

***Abstract*—This paper presents a macromodel-based approach for fast Signal Integrity assessment for highly integrated Radio Frequency (RF) and Mixed-Signal System on Chip (SoC) applications. In particular, we introduce a complexity reduction process that enables the Signal Integrity verification via analog circuit simulations, and we apply the methodology to complex radio transceiver chips in order to characterize the influence of parasitic elements on the signal processing performance of the system. Some preliminary tests show that the proposed methodology leads to significant simulation speedup factors with respect to standard approaches for the specific application herewith considered.**

I. Introduction

Modern Radio-Frequency (RF) transceivers and RF Systems on Chip (SoC) in nanoscaled CMOS or BiCMOS technologies consist of multiple analog and mixed-signal circuit blocks that must coexist within the same structure with large digital circuit blocks. It is well known that the digital parts often generate significant amount of noise at clock harmonics, which may couple via capacitive, inductive, and substrate mechanisms to the very sensitive analog parts, leading to signal degradation and possibly compromising the functional performance of the system. Such Signal Integrity (SI) problems typically occur in full system context, possibly arising only in special workload transmit/receive scenarios. This means that SI issues will not be detected until system hardware is under test. Therefore, a suitable signal verification process must be devised for the investigation of all scenarios defined in the communication standard specification. Of course, this verification must be performed in early stages of the design using suitable circuit simulation tools.

Due to the mixed-signal nature of the application, the signal verification is usually performed by transient circuit simulations using base-band modeling approaches [2]. However, the RF carrier frequency dictates the maximum time step to be allowed. It is clear that the simulation of a full transmission burst using the detailed transistor-level description of all digital and analog blocks is unfeasible due to its overwhelming complexity. The purpose of this work is to propose a technique to reduce the computational burden of such simulations, still retaining the analog accuracy level that is required for a sound system verification.

One main factor enables a complexity reduction in this signal integrity analysis. Looking at the signal processing chain, e.g., in a RF transceiver, it is possible to identify several large analog blocks that operate nearly linearly under a suitable bias. Linearity is indeed one of the requirements for proper system performance. When signals are within the linearity region of such blocks, linear transfer function models can be employed to represent their behavior at the interface ports, regardless of the very complex internal structure. A typical example is a Baseband Filter block (BBF), often located in the receiver chain of a GSM/EDGE and UMTS transceiver chip, which is the test case considered in this paper. Once the scattering matrix of the entire block is known, e.g., via simulation of a device-level circuit model including parasitics from physical implementation (layout, substrate), a linear macromodel can be extracted via standard techniques, usually with excellent accuracy levels. The macromodel can then be used as a reduced-complexity replacement for the circuit block in all subsequent simulations, with significant savings in simulation time and at no loss of accuracy.

This paper is organized as follows. Section II presents the main example that is considered in this work to illustrate the feasibility of the approach. Section III presents the macromodeling technique for complexity reduction. Section IV provides numerical results showing the excellent accuracy and performance of the proposed behavioral macromodels. This section provides also preliminary results on a parameterization scheme for macromodels, aimed at fast sensitivity studies with respect to external parameters. Conclusions are drawn in Section V.

II. Problem description

We illustrate all steps of the proposed macromodeling strategy using a specific example. However, since the the methodology is general in principle, an additional example will be presented in Section IV-C. We consider a GSM/EDGE multi-band transceiver [10] targeted for all four worldwide frequency standards at 850, 900, 1800, and 1950 MHz. Among the various functional circuit blocks on the chip, including oscillators, buffers, and the digital core, we select the Baseband Filter block, a big analog building block located in the receiver path between the Demodulator unit and the Analog/Digital Converter (ADC) unit. This block is responsible for amplifying with programmable gain steps and accurately filtering the downconverted in-phase and quadrature signals after the demodulator. The integrated BBF provides sufficient suppression of blocking signals and adjacent channel interferers as to match optimally the integrated ADC, providing 90 dB dynamic range at a full scale of 2 Vpp. The BBF also provides

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TABLE I
BASEBAND FILTER PORT DESCRIPTION.

Port #	Description
1–12, 26, 27	Digital control pins
13–20	Signal inputs
21	Bias current
22-25	Signal outputs
28	Bandgap voltage
29	Feedback voltage (to Demodulator)
30–33	Switchable Measurement/Calibration Outputs
34, 35	V_{SS}, V_{DD} power supply

suppression to fulfill the anti-aliasing requirements of the ADC.

The BBF block has several interface ports, some of them represent digital inputs used to program and configure the filter for a dedicated receive scenario, e.g., for the selection of which carrier frequency is to be processed. The design is fully differential, with 35 pins including two power supply pins. A short pin description is outlined in Table I. Our aim is the derivation of a reduced-complexity model that is capable of representing not only the ideal schematic behavior, but also the crosstalk through the block due to parasitic small signals always present at V_{DD}, V_{SS}, analog bias pins and especially from digital inputs into the analog domain, the latter often causing the most critical signal degradation effects. This parasitic crosstalk is mainly due to capacitive and possibly inductive couplings in the realized block layout.

As mentioned above, the behavior of the 35-port block is highly linear in its input/output response, so a linear transfer function model can be used to characterize all couplings. Therefore, a full 35-port S-parameter simulation is performed to generate the complete scattering parameter set for this circuit block, using nominal operation bias. This simulation is performed using a fully-detailed circuit netlist that includes all parasitics as well as all device-level models. Device-level models are available from the design library, whereas parasitics extraction is performed using a commercial tool [9] (with all its known limiting constraints). If this strategy were applied on full chip scale (SoC level), the result would be a huge circuit netlist having a complexity which is orders of magnitude away from current analog simulation capabilities. Even at the single-block level, the extracted netlist including all couplings is too complex and not manageable.

In order to be able to provide a frequency-domain characterization, an ad hoc reduction was applied to the extracted netlist, leading to a subset of "effective" RC circuit elements on and between the internal wiring. The (still large) netlist could now be run, and the scattering parameters

$$\mathbf{S}(j\omega)\,, \quad \omega = \omega_1, \ldots \omega_{\max} \tag{1}$$

could be computed using a standard circuit analysis tool [1]. Details of the circuit complexity involved in this characterization are presented in Section IV. The bandwidth of this characterization ranges from 1 kHz to 100 GHz, with a dynamic range in the scattering parameters between +32 dB down to -200 dB. We remark that a wide dynamic range down to -150 dB is required for GSM/EDGE applications, since very high isolation levels must be guaranteed for a successful isolation and signal integrity verification. The frequency range has been extended up to 100 GHz mainly for demonstration of the capabilities of proposed macromodeling approach. In real applications, frequencies up to 10 or 20 GHz are sufficient, depending on the specific structure. We remark that no investigations on the accuracy of the automated parasitic extraction tools [9] over such frequency range have been performed, although the validity of such parasitics must be carefully assessed in order to perform a meaningful system verification.

III. METHODOLOGY

The scattering data in (1) are the starting point of our complexity reduction process. This reduction is performed by fitting a rational model to the scattering data

$$\mathbf{S}(j\omega) \simeq \widehat{\mathbf{S}}(j\omega) = \mathbf{S}_\infty + \sum_{n=1}^{N} \frac{\mathbf{R}_n}{j\omega - p_n} \quad \text{for} \quad \omega = \omega_k\,, \tag{2}$$

where p_n and $\mathbf{R}_n$ denote the poles and the residues of the rational approximation, whereas $\mathbf{S}_\infty$ is the high-frequency direct coupling matrix. We adopt a rational function of frequency since this functional form is natural for lumped circuits. Also, the rational model (2) is readily synthesized into an equivalent circuit or state-space matrix stamp in order to be included as an external model in system-level simulations.

For the computation of the poles and residues we use a variation of the well-known Vector Fitting (VF) algorithm [3], using the particular implementation available in [4] and documented in [7]. Some of the details of this computation that are relevant for this application are now addressed.

The first difficulty that must be addressed is the very high dynamic range of the scattering data. At low frequencies some functional responses provide an analog gain of about +32 dB, whereas some other responses must provide an isolation of at least 120 dB, thus implying some 150 dB of dynamic range to be fitted accurately. It is clear that an absolute error control in the fit would require at least 8 significant digits to guarantee such accuracy level, and this is obviously unfeasible. Therefore, we adopt a relative error control by using an inverse magnitude weighting scheme. In particular, we minimize the error

$$\mathcal{E}_{lm} = \sum_k \beta_{lm}(j\omega_k)|\widehat{S}_{lm}(j\omega_k) - S_{lm}(j\omega_k)|\,, \tag{3}$$

for each matrix elements, where the individual weights $\beta_{lm}(j\omega_k)$ are defined as

$$\beta_{lm}(j\omega_k) = \begin{cases} |S_{lm}(j\omega_k)|^{-\alpha} & \text{if} \quad |S_{lm}(j\omega_k)| < \varepsilon\Pi \\ (\varepsilon\Pi)^{-\alpha} & \text{otherwise} \end{cases} \tag{4}$$

and

$$\Pi = \max_{klm} |S_{lm}(j\omega_k)|\,. \tag{5}$$

The parameter α can be used to fine-tune the performance of the weighting scheme. In particular, standard absolute error

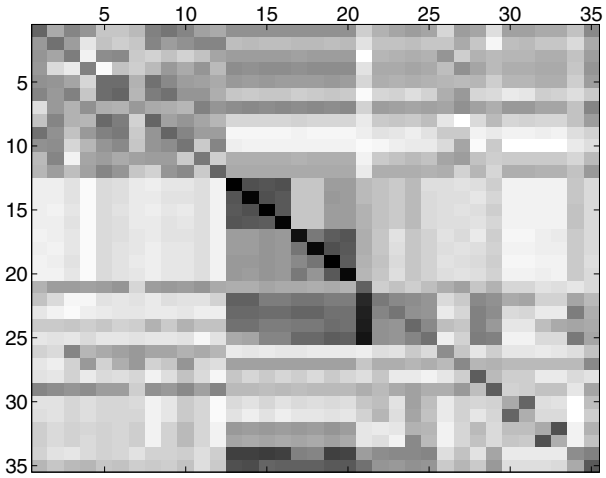

Fig. 1. Weighted error between model and data for each of the scattering matrix elements. Darker elements correspond to larger errors, plotted using a logarithmic scale. The maximum observed error was 0.22%.

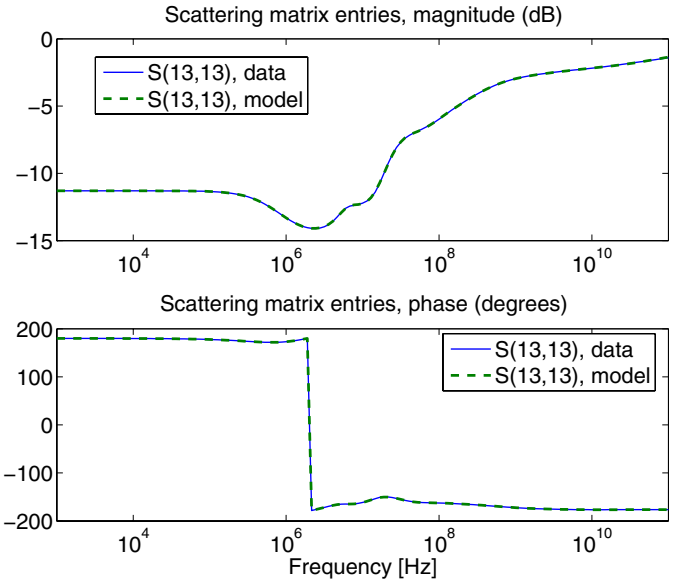

Fig. 2. Comparison between raw scattering data and fitted model for the matrix element characterized by the worst-case error.

control is obtained when $\alpha = 0$, whereas pure relative error control is obtained with $\alpha = 1$. Usually, a good performance is achieved with intermediate values. The second parameter ε allows to control the dynamic range that is fitted accurately, by avoiding excessively large weights occurring when the magnitude of the corresponding scattering elements is very small. In this work, we use the combination $\alpha = 0.4$ and $\varepsilon = 10^{-6}$, which is observed to guarantee excellent performance without requiring many poles in the rational fit.

A second difficulty that is typical for this type of application is the large port count of the structure under modeling. The complete set of scattering parameter samples cannot be processed at once in the same least squares fit. Therefore, some complexity reduction is in order. We adopt here a response

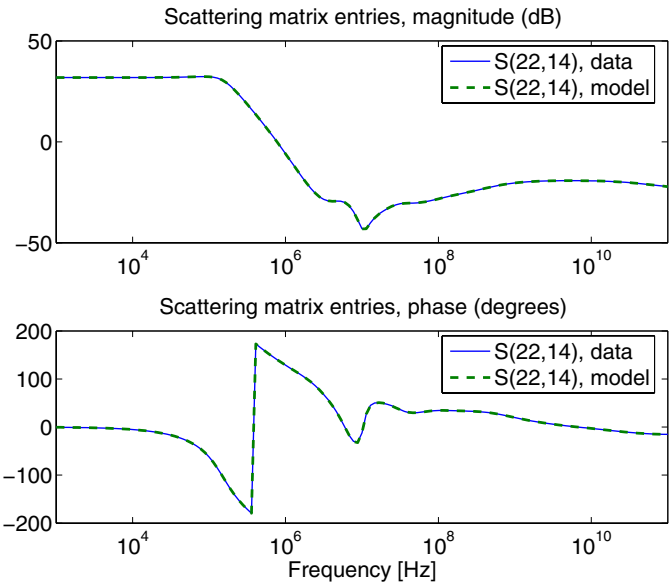

Fig. 3. Comparison between raw scattering data and fitted model for input-output transfer function (Lower Band, In-phase signal).

splitting process [5], [6], based on fitting separately subsets of the scattering responses with common poles. In a second stage, the individual submodels are combined by suitably connecting their minimal state-space realizations. This procedure is known to maximize the accuracy of the model since the number of constraints in a single least squares fit is reduced. Also, the complexity of the overall model (in terms of circuit elements) is comparable to the complexity that would be obtained by using common poles for all scattering responses, since a circuit synthesis in the latter case would require the replication of each pole by a number of times given by the numerical rank of its associated residue matrix.

A third difficulty is the estimation of the correct model order to be employed for the rational fit. Due to the complexity of the modeled circuit block and to the very different nature of the various input ports, any *a priori* estimate for the number of required poles, which is valid for all scattering matrix elements, is rather difficult to provide. Therefore, we adopt the algorithm of *Adding* and *Skimming* introduced in [7] in order to provide a reasonable estimate based on the stagnation of the fitting error $\mathcal{E}$ for each individual subset under processing. As a final remark, we note that no passivity enforcement, as usually needed for passive macromodeling applications, is required here, since the circuit block under modeling does not represent a passive structure.

IV. Numerical Results

A. BaseBand Filter macromodeling

We present now a few results that are representative for the entire modeling task. Figure 1 reports a global view of the entire 35×35 scattering matrix. Each box in this plot reports the deviation between model and data for the corresponding matrix element S_{lm}. Darker colors correspond to elements

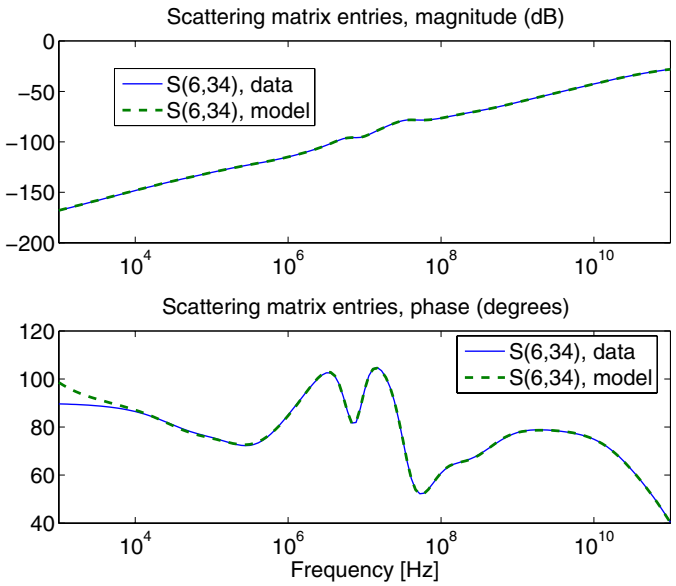

Fig. 4. Comparison between raw scattering data and fitted model for coupling between noisy digital control pin #6 and analog V_{SS}.

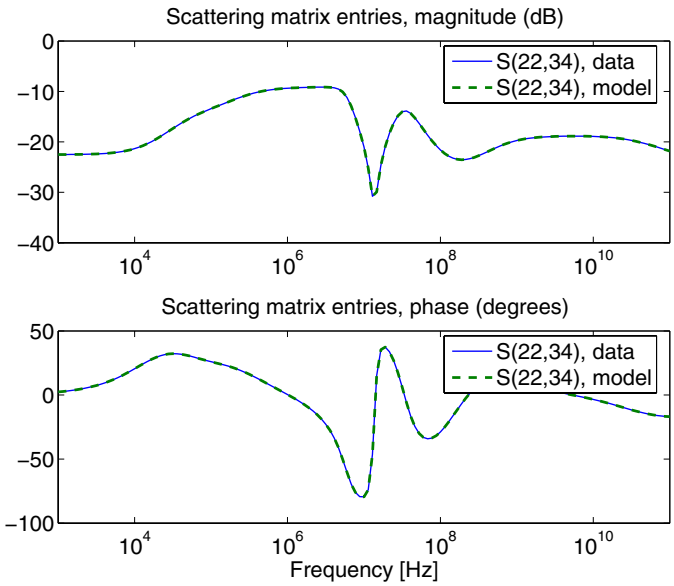

Fig. 5. Comparison between raw scattering data and fitted model for coupling between V_{SS} and one of the analog output signals.

with worse fit accuracy. Figure 2 reports a comparison between model and data for the worst-case matrix element resulting for the fit. The picture shows that even for this worst-case element the accuracy is excellent. Figures 3–6 demonstrate the accuracy of the rational fit for four transfer functions that are important for present application. In particular, Fig. 3 shows one of the input-output transfer functions (linear signal gain for in-phase/quadrature signals). Significant signal amplification is evident as well as a sharp lowpass filter behavior. Figure 4 reports the coupling between a noisy digital control pin and V_{SS}, for which good isolation should occur. Finally, Figs. 5 and 6 report the coupling into one of the analog outputs from V_{SS} noise and analog bias current, respectively. The model accuracy is excellent for all scattering matrix elements, as expected from the synoptic view of Fig. 1. The only visible differences between model and data are in the phase plot of Fig. 4, but only for those frequencies corresponding to a very small magnitude, below -150 dB.

One may ask why is it possible to retain this level of accuracy with such a drastic simplification in the circuit. This is not true in general, indeed. For present application, however, the original circuit has a very small electrical size. Its circuit complexity arises from a complicated geometry configuration, leading to a very large number of layout-driven parasitic components. Transfer functions remain very smooth throughout the investigated frequency range, allowing for rational approximations with very few poles.

The modeling task that we have described in this paper was essentially aimed at reducing the complexity that would be required to run system-level Signal Integrity analyses including parasitic elements. We compare now the complexity and the performance of the two available circuit representations for the Baseband Filter Block under investigation in Tables II and III. Table II compares the two circuits by showing the element count of the corresponding netlists. The column labeled "full" denotes the starting device-level circuit model including parasitics from physical layout. The column labeled "model" denotes the rational fitted model. The complexity reduction is evident from the table.

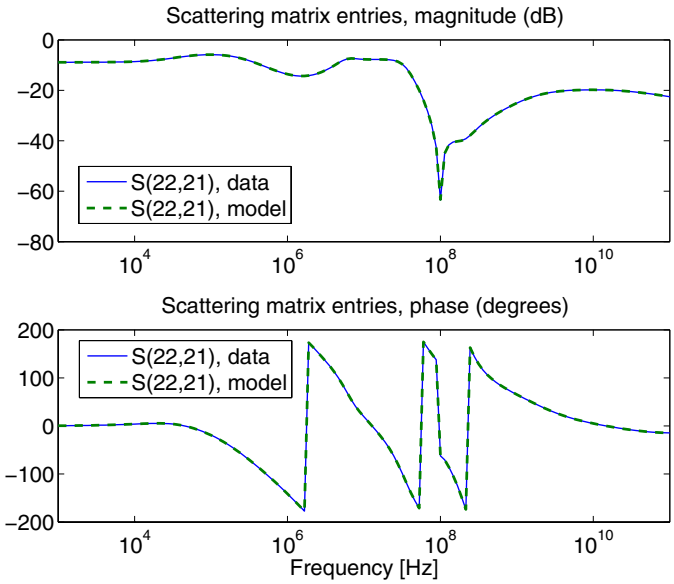

Fig. 6. Comparison between raw scattering data and fitted model for coupling between bias current noise and one of the analog output signals.

Table III summarizes the results of a few different simulation runs performed with the two models. The table reports the CPU cost for three different types of analysis that are relevant for this application, namely the evaluation of the DC operation point, the AC analysis for the evaluation of the scattering

TABLE II
CIRCUIT COMPLEXITY FOR FULL AND REDUCED-ORDER MODELS OF THE BBF CIRCUIT BLOCK.

	Full	Model
nodes	31718	539
equations	31840	644
iprobe	35	35
bsim4	6873	—
diode	3638	—
capacitor	27552	469
inductor	52	—
resistor	61730	539

TABLE III
CPU TIME REQUIRED FOR DIFFERENT TYPES OF ANALYSIS FOR FULL AND REDUCED-ORDER MODELS OF THE BBF CIRCUIT BLOCK.

	Full	Model	Speedup
DC	37 m 38.4 s	0.18 s	1255 X
AC	8 m 0.6 s	4.14 s	116 X
TRAN	29 m 18.7 s	2.52 s	698 X

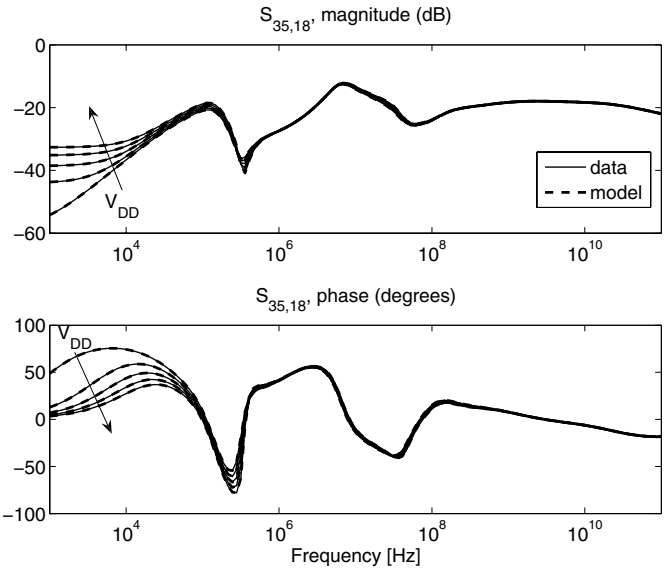

Fig. 7. Comparison between raw scattering data and fitted model on the reference identification grid $V_{DD} = \{2.4, 2.6, 2.8, 3.0, 3.2\}\ V$.

parameters, and transient analysis for a $50\,\mu$s signal sequence. The speedup factor that is achieved using the proposed model is quite significant, with practically no loss of accuracy within the validity of the linearization. An asymptotic estimation of this speedup factors is easily justified by the number N of equations in the netlists, see Table II. The CPU time scales as a power of N, typically between 2 and 3 depending on the circuit solution method embedded in the adopted solver (e.g., Modified Nodal Analysis for SPICE).

B. Parameterization for sensitivity analysis

In this section, we present preliminary results on the generation of parameterized macromodels aimed at fast sensitivity studies under the variation of external variables, e.g., geometry, material, biasing conditions, etc. The basic idea is to apply a similar interpolation process as already applied in [8] to transmission line macromodels. Given some external parameter $\lambda \in [\lambda_{\min}, \lambda_{\max}]$, we want to derive a rational macromodel $\widehat{\mathbf{S}}(j\omega;\lambda)$ providing an accurate fit to the parameter-dependent scattering responses

$$\mathbf{S}(j\omega;\lambda) \simeq \widehat{\mathbf{S}}(j\omega;\lambda) \quad \forall\omega, \quad \forall\lambda \in [\lambda_{\min}, \lambda_{\max}]\,. \tag{6}$$

The above relation is first enforced on a discrete grid in the parameter space, i.e., for

$$\lambda \in \{\lambda_1, \lambda_2, \ldots, \lambda_q\} \tag{7}$$

using common poles in a single VF run. Then, smooth interpolation schemes (spline-based) are applied to the residue matrices in order to recover a continuous dependence on λ

$$\widehat{\mathbf{S}}(j\omega;\lambda) = \mathbf{S}_\infty(\lambda) + \sum_{n=1}^{N} \frac{\mathbf{R}_n(\lambda)}{j\omega - p_n}\,, \tag{8}$$

starting from the discrete set of residue matrices available as a result from the VF run.

Figures 7-8 show the results for the Baseband Filter block under investigation. In this experiment, nine independent sets of 35×35 scattering responses were generated, with different values of V_{DD} in the range $[2.4, 3.2]$ V, with equal spacing of 0.1 V, the nominal value being $V_{DD} = 2.8$ V. Then, only $q = 5$ sets of responses with $V_{DD} = \{2.4, 2.6, 2.8, 3.0, 3.2\}$ V were used for the model identification. Models are compared to these raw responses in Fig. 7 for one scattering matrix element, showing excellent accuracy. Interpolation was then applied as in (8) to compute the model responses for $V_{DD} = \{2.5, 2.7, 2.9, 3.1\}$ V. These interpolated model responses are compared to the reference raw responses in Fig. 8. These plots confirm that the dependence of the responses on V_{DD} is very smooth, and that the proposed interpolation scheme is very well suited to match the accuracy constraints needed for system verification. We remark that the circuit complexity is identical for each parameterized model, with the same element counts reported in Table II. Availability of such parameterized macromodel allows for very fast sensitivity analyses and what-if analyses at the system level, using standard circuit solvers.

C. Another test case

We report in this Section the macromodeling results for a full integrated CMOS Low Noise Amplifier (LNA) for an actual EDGE/GSM transceiver. The circuit block has 14 pins and is internally much less complex than the Baseband Filter analyzed in the foregoing sections. It provides however an additional feasibility analysis example for the proposed technique aimed at complexity reduction.

The modeling procedure is the same as for the BBF block. Parasitic extraction tools are applied to the layout in order to provide a broadband characterization of the multiport behavior, including relevant spurious coupling paths. Then, VF is applied to compute a linear reduced-complexity macromodel. Figure 9 provides the comparison between model and data for a few selected responses. As for the BBF block, accuracy is excellent. Table IV reports the CPU cost for various simula-

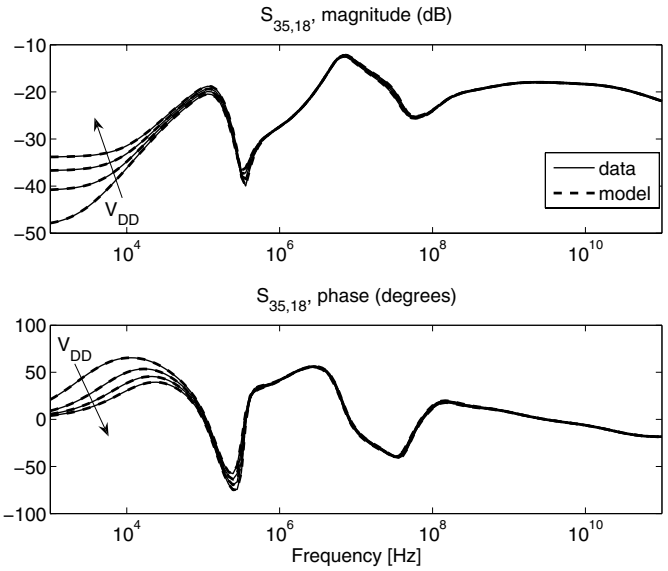

Fig. 8. Comparison between raw scattering data and parameterized model on the validation grid $V_{DD} = \{2.5, 2.7, 2.9, 3.1\}\ V$.

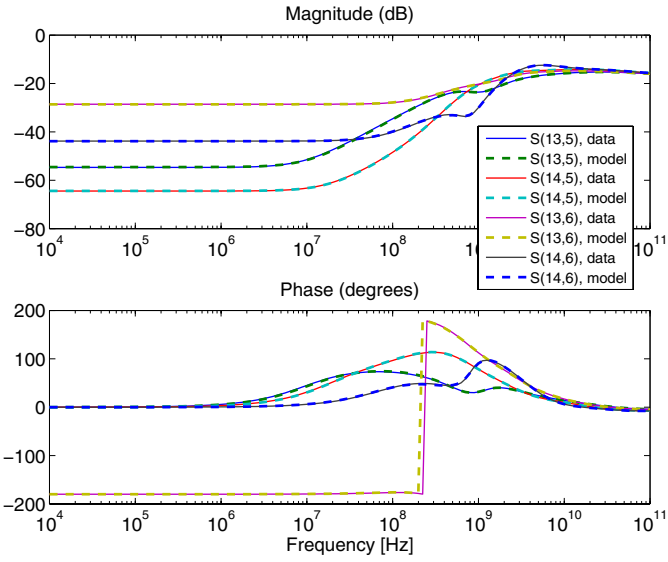

Fig. 9. Comparison between raw scattering data and fitted model for the LNA structure. Couplings between non-inverting inputs at 1800 MHz (port 5) and 1900 MHz (port 6) to power supply ports V_{DD} (port 13) and V_{SS} (port 14) are shown.

tion tasks employing original circuit and macromodel. Good speedup factors are observed for this case as well.

V. Discussion and Conclusions

In this paper, we have presented a general methodology for the frequency-domain characterization of complex linear circuit blocks for RF and Mixed-Signal integrated applications. The basic idea is the characterization of such blocks via rational macromodels, which can be identified using standard fitting algorithms such as VF. However, special care must be taken in handling large dynamic ranges in the macromodel responses and large port counts. These two aspects can be dealt with via suitable weighting schemes combined with response-splitting strategies.

TABLE IV
CPU time required for different types of analysis for full and reduced-order models of the LNA circuit block.

	Full	Model	Speedup
DC	1.07 s	10 ms	107 X
AC	11.85 s	220 ms	54 X
TRAN	138.93 s	9.52 s	14.6 X

The main technique was applied in this work to a Baseband filter block located in the receiver chain of a GSM/EDGE chip. The results that we obtained show that excellent accuracy was obtained for the corresponding 35-port macromodel, with the advantage of a very effective complexity reduction. Such performance boost when using the macromodels is easily justified by the element count (see Table II) in the circuits to be solved. The original schematic includes many more linear elements than the macromodel. In addition, the presence of nonlinear active devices is the main reason for the very slow computation of the DC operation point in the original circuit. These devices are not present in the macromodel, since the latter only represents a linear transfer function around the nominal bias. Nonetheless, it has been shown that inclusion of bias variation in the macromodel can be performed using a suitable parameterization scheme. Overall, these results show that the reduced-order macromodel enables fast simulation runs, which are not feasible with the full device-level circuit of the filter including the parasitic elements from the layout. Therefore, the proposed technique is enabling system-level Signal Integrity characterization and analysis, including sensitivity and what-if investigations.

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