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Modeling method of sequence admittance for three-phase voltage source converter under unbalanced grid condition

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Abstract The admittance is a strong tool for stability analysis and assessment of the three-phase voltage source converters (VSCs) especially in grid-connected mode. However, the sequence admittance is hard to calculate when the VSC is operating under unbalanced grid voltage conditions. In this paper, a simple and direct modeling method is proposed for a three-phase VSC taking the unbalanced grid voltage as a new variable for the system. Then coupling in the three-phase system can be calculated by applying the harmonic linearization method. The calculated admittance of three-phase VSCs is verified by detailed circuit simulations.

Keywords Unbalanced grid voltage, Three-phase voltage source converter, Harmonic linearization, Positive and negative sequence admittance, Stability

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1 Introduction

In recent years, renewable energy is widely used in the power system to solve the increasing energy crisis and environmental problems. In a modern power system, the penetration of renewable energy is much higher than ever before. The three-phase voltage source converter (VSC) is one of the key pieces of equipment to make full use of renewable energy because it can provide a sinusoidal current to the grid and flexible power control [1, 2]. However, the stability of the grid-connected VSC will affect the safety and stability of the power system in such a situation [3].

There are two main ways to perform the stability analysis of grid-connected converter systems [4]. One is the time domain method based on the state space model [5] and the other one is the frequency domain method which is based on the impedance model [6]. The time domain method is mainly suitable when the root locus analysis determines that the frequency is not changing, given a unified model of the grid-connected system [7, 8]. Thus, the stability analysis will be very complex when considering the influence of the phase-locked loop (PLL) and the grid impedance [9].

The frequency domain method is based on the impedance model which includes the impedance of the grid and the power converter and uses them to represent their external characteristics. Then, the stability of the system can be judged by stability criteria like the Nyquist criterion [10]. The impedance of the grid can be easily obtained by measuring through experiments or from a given X/R ratio [11]. However, the impedance of the converter is hard to obtain because of the various and complex control strategies and circuit parameters.

Much research effort has been devoted to impedance modeling of three-phase voltage source converters. In [12], several small-signal analysis methods used for modeling electric ship power systems are discussed. The conventional small-signal linearization techniques cannot be directly used because of the lack of a constant operating point during the periodic steady-state operation trajectory. Belkhayat linearized the system in the *dq*-coordinate reference frame by transforming the fundamental component into DC quantities in [13]. Then the nonlinearity can be eliminated to develop a small-signal model which can be used for control design and system stability analysis at a given operation point. But it is not suited for unbalanced conditions and provides no clear physical meaning for the *d*-axis and *q*-axis impedances. In [14], an impedance model of a three-phase VSC is proposed in the *dq*-frame considering the effect of PLL's and the control strategy's parameters. But the impedance in the *dq*-frame is hard to measure directly, and the stability criterion in the *dq*-frame is too complicated to be used in practice [4]. In [15], a small-signal model of a PV inverter containing the PLL and DC-side voltage and inner loops was proposed. It illustrates the PLL impacts on the output *q*-channel impedance of the inverter which can lead to instability. However, the coupling between the *d*-*q* channels has not been considered. In [16], a *d*-*q* impedance matrix of the inverter was proposed to analyze the stability of the system. In [17], the same model was used for analyzing stability of three-phase paralleled converters. The *q*-*q* channel impedance interaction leads to instability of the system. However, it is hard to obtain such impedances without some special equipment and instruments. The research above mainly focusses on situations of balanced grid voltage. However, there is still a gap because there is no mature method for impedance modeling of the VSC under practical three-phase unbalanced condition.

Harmonic linearization [18] is a method to transform a nonlinear periodically time varying system into a small-signal linear model, and has been successfully realized to get the impedance of uncontrolled diode rectifiers [6, 19] and single-phase PFC converters [20] as well as grid-connected inverters [21, 22]. Particularly, in [21, 22], the positive and negative sequence impedance model is proposed in a static frame and then can be applied in stability analysis. In [22], an impedance-based stability analysis method is studied initially for a grid-connected inverter working under unbalanced grid voltage. However, the method in this paper neglects the coupling effects between the positive and negative sequence impedances. Knowing the sequence admittance of a VSC under sustained grid faults is helpful for judging the stability of the grid-connected converter system [23, 24]. It is also helpful for the design of the control system and for admittance shaping to manage power quality of the converter [25–27]. Therefore, the harmonic linearization method should be improved for unbalanced situations.

In this paper, a simple and direct modeling method of a three-phase VSC under unbalanced grid voltage is proposed. Based on harmonic linearization, the coupling of the positive and negative sequence admittances is considered and the admittance matrix is given. This method can be used with some kinds of sustained grid faults such as unbalanced grid voltage. This would be caused by unbalanced sources or loads in the grid. These faults can be sustained, so the operation of the VSC will be highly affected by them. In our opinion, the impedance of the VSC would be changed by an unbalanced grid fault. However, some fault conditions may occur very quickly, in milliseconds, and the fault can be eliminated. These are transient faults. Actually, in responding to these transient faults, the VSC would be quite slow. For instance, the PLL is usually used with a bandwidth of 10–100 Hz, like a general used synchronous reference frame PLL (SRF-PLL). Therefore, during these kinds of transient fault, the output of PLL would be only slightly affected and in many cases the converter will keep operating. The rest of this paper is organized as follows: Section 2 proposes the improved sequence admittance of the three-phase VSC under unbalanced grid conditions by harmonic linearization. The unbalanced grid voltage can be introduced as a new variable of the original model. Section 3 shows the calculation method of the sequence admittance of the VSC based on this model. Section 4 verifies the admittance of the VSC by detailed circuit simulations and analyzes the influence of the admittance on the system stability. Section 5 concludes this paper.

2 Sequence admittance modeling

2.1 Topology and control strategy of VSC

Figure 1 illustrates the topology of a three-phase voltage source pulse-width modulation (PWM) converter. According to Kirchhoff's law, the model of the converter working as an inverter referred to the three-phase stationary frame is:

$$L\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{a}} \\ i_{\mathrm{b}} \\ i_{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} V_{\mathrm{a}} - V_{\mathrm{PCC,a}} \\ V_{\mathrm{b}} - V_{\mathrm{PCC,b}} \\ V_{\mathrm{c}} - V_{\mathrm{PCC,c}} \end{bmatrix} \tag{1}$$

where i_{a}, i_{b} and i_{c} are the output currents of the converter. The direction of the currents is towards the grid as shown in Fig. 1. $V_{\mathrm{PCC,a}}$, $V_{\mathrm{PCC,b}}$ and $V_{\mathrm{PCC,c}}$ are the voltages at the point of common coupling (PCC). V_{a}, V_{b} and V_{c} are the

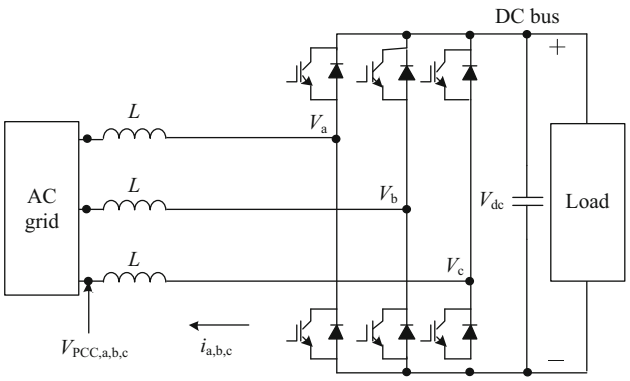
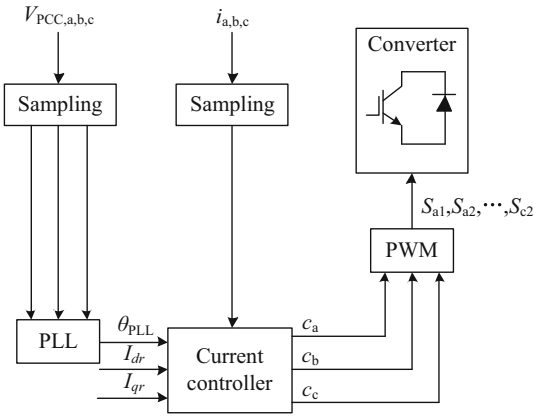


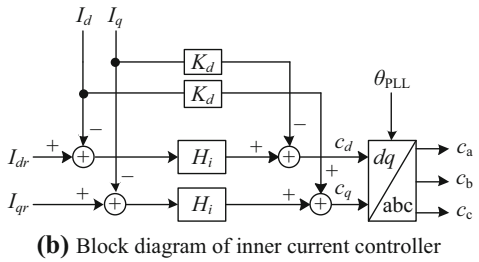
Fig. 1 Topology of three-phase voltage source PWM converter

output phase voltages of the converter. L is the output filter inductance. V_{dc} is the voltage of DC side.

The control structure of the three-phase voltage source PWM converter is shown in Fig. 2a. The voltage at the PCC is sampled as the input of PLL. θ_{PLL} is the output angle of the PLL. I_{dr} and I_{qr} denote the reference current components on the d-axis and the q-axis. V_{dc} is assumed constant because of the large capacitance on the DC side and the low bandwidth of the voltage loop, and consequently I_{dr} and I_{qr} are also assumed constant. The current control signals c_a, c_b and c_c are obtained by sampling the grid side currents i_a, i_b and i_c as the input of the inner current controller. Then the switching function of the converter (S_{a1}, S_{a2}, S_{b1},…,S_{c2}) can be obtained by inputting the current control signals into the PWM signal generator.



(a) Controller of VSC



(b) Block diagram of inner current controller

Fig. 2 Control strategy of three-phase voltage source PWM converter

Based on the average of the converter model and the topology and the control strategy, (1) can be rewritten as:

$$L\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\bar{i}_a\\ \bar{i}_b\\ \bar{i}_c\end{bmatrix} = K_m V_{dc}\begin{bmatrix}\bar{c}_a\\ \bar{c}_b\\ \bar{c}_c\end{bmatrix} - \begin{bmatrix}V_{PCC,a}\\ V_{PCC,b}\\ V_{PCC,c}\end{bmatrix} \tag{2}$$

where K_m is the modulator gain.

The inner current controller is shown as Fig. 2b. The I_d and I_q are the current component on the d-axis and the q-axis obtained by transforming the grid side current using the Park Transformation. H_i is the compensation factor for the inner current controller, which is usually a PI or a PR controller, and K_d is its decoupling factor. c_d and c_q are the d-axis and q-axis current control signals after decoupling. The current control signals are obtained by the inverse Park Transformation.

As indicated in Fig. 2b, the d-axis and q-axis current control signals are obtained as follows:

$$\begin{cases} c_d = H_i(I_{dr} - I_d) - K_d I_q \\ c_q = H_i(I_{qr} - I_q) + K_d I_d \end{cases} \tag{3}$$

Thus, c_a, the current control signal of phase A can be obtained as:

$$c_a = c_d \cos\ \theta_{PLL} - c_q \sin\ \theta_{PLL} \tag{4}$$

2.2 Sequence admittance modeling for balanced grid

This analysis generally follows [21]. Firstly, if the output of the PLL is not affected by the harmonic voltage of the PCC, θ_{PLL} increases linearly, and is an ideal sawtooth wave modulo 2π, given by $\theta_{PLL}=\theta_1=2\pi f_1 t$. Then, assuming the voltage of phase A at the PCC has a small perturbation in the time domain, the voltage can be written as:

$$\begin{aligned} V_{PCC,a} = {} & V_1\cos(2\pi f_1 t) + V_p\cos(2\pi f_p t + \varphi_p) \\ & + V_n\cos(2\pi f_n t + \varphi_n) \end{aligned} \tag{5}$$

where the V_1, V_p and V_n are the magnitudes of the fundamental positive sequence voltage, positive sequence harmonic voltage and negative sequence harmonic voltage, respectively, and f_1, f_p and f_n are the corresponding frequencies. φ_p and φ_n are the phases of the positive sequence and negative sequence harmonic voltage. Based on Euler's law, the first term of (5) $V_1\cos(2\pi f_1 t)$ can be changed to $(V_1/2)(e^{j2\pi f_1 t} + e^{-j2\pi f_1 t})$. Thus, the equation for $V_{PCC,a}$ in the frequency domain is as follows:

$$V_a[f] = \begin{cases} V_1 & f = \pm f_1 \\ V_p & f = \pm f_p \\ V_n & f = \pm f_n \end{cases} \tag{6}$$

where V_1 corresponds to the fundamental positive sequence voltage of phase A in frequency domain, $V_p = (V_p/2)e^{\pm j\varphi_p}$ to the positive sequence harmonic voltage, and $V_n = (V_n/2)e^{\pm j\varphi_n}$ to the negative sequence harmonic voltage.

Assume that the current of phase A responds to the voltage in the time domain as:

$$\begin{aligned} i_a = {} & I_1 \cos(2\pi f_1 t + \varphi_{i1}) + I_p \cos(2\pi f_p t + \varphi_{ip}) \\ & + I_n \cos(2\pi f_n t + \varphi_{in}) \end{aligned} \tag{7}$$

where I_1, I_p and I_n are the magnitudes of the fundamental positive sequence current, positive sequence harmonic current and negative sequence harmonic current, respectively, and φ_{i1}, φ_{ip} and φ_{in} are their phases. Then, the equation of i_a in the frequency domain is as follows:

$$I_a[f] = \begin{cases} I_1 & f = \pm f_1 \\ I_p & f = \pm f_p \\ I_n & f = \pm f_n \end{cases} \tag{8}$$

where $I_1 = (I_1/2)e^{\pm j\varphi_{i1}}$ corresponds to the fundamental positive sequence current of phase A in frequency domain, $I_p = (I_p/2)e^{\pm j\varphi_{ip}}$ corresponds to the positive sequence harmonic current, and $I_n = (I_n/2)e^{\pm j\varphi_{in}}$ corresponds to the negative sequence harmonic current. The equation of $I_a[f]$ after sampling is

$$I_a[f] = \begin{cases} G_i(\pm j2\pi f_1)I_1 & f = \pm f_1 \\ G_i(\pm j2\pi f_p)I_p & f = \pm f_p \\ G_i(\pm j2\pi f_n)I_n & f = \pm f_n \end{cases} \tag{9}$$

Applying the Park Transformation to (8) gives:

$$\begin{cases} \begin{aligned} i_d(t) = {} & I_1 \cos\ \varphi_{i1} + I_p \cos(2\pi(f_p - f_1)t + \varphi_{ip}) \\ & + I_n \cos(2\pi(f_n - f_1)t + \varphi_{in}) \end{aligned} \\ \begin{aligned} i_q(t) = {} & I_1 \sin\ \varphi_{i1} + I_p \sin(2\pi(f_p - f_1)t + \varphi_{ip}) \\ & + I_n \sin(2\pi(f_n - f_1)t + \varphi_{in}) \end{aligned} \end{cases} \tag{10}$$

According to [21], sampling at the fundamental frequency is neglected since $G_i(\pm j2\pi f_1) \approx 1$. Based on Euler's law, $\sin(2\pi f_1 t)$ can be transformed to $(e^{j2\pi f_1 t} - e^{-j2\pi f_1 t})/(2j)$, so the equations for I_d and I_q in the frequency domain are as follows:

$$I_d[f] = \begin{cases} I_1 \cos\ \varphi_{i1} & \text{dc} \\ G_i(s \pm j2\pi f_1)I_p & f = \pm(f_p - f_1) \\ G_i(s \mp j2\pi f_1)I_n & f = \pm(f_n + f_1) \end{cases} \tag{11}$$

$$I_q[f] = \begin{cases} I_1 \sin\ \varphi_{i1} & \text{dc} \\ \mp jG_i(s \pm j2\pi f_1)I_p & f = \pm(f_p - f_1) \\ \pm jG_i(s \mp j2\pi f_1)I_n & f = \pm(f_n + f_1) \end{cases} \tag{12}$$

where $I_d[f]$ denotes I_d in the frequency domain and $I_q[f]$ denotes I_q in the frequency domain; dc represents that the frequency is 0 Hz. G_i denotes the delay of the current sampling as follows:

$$G_i(s) = e^{-sT_i} \frac{1 - e^{-sT_i}}{sT_i} \frac{1}{1 + s/\omega_i} \tag{13}$$

where T_i is the period of current sampling and ω_i is the cut-off frequency of the analog-digital converter.

Figure 3 illustrates the assumption that the positive sequence harmonics of voltage only produce positive sequence harmonics of current at the same frequency. Similarly, the negative sequence harmonics of voltage only produce negative sequence harmonics of current at the same frequency. The positive and negative sequence components are decoupled from each other.

Based on harmonic linearization, if

$$X(t) = Y(t)Z(t) \tag{14}$$

then a Fourier coefficient $X[i]$ of the function $X(t)$ can be calculated by the convolution of the Fourier coefficients of $Y(t)$ and $Z(t)$ as follows:

$$X[i] = \sum_{k=-\infty}^{\infty} (Y[k]Z[i-k]) \tag{15}$$

The equation of the inner current controller signal of phase A at the frequency f_p can therefore be derived from (4) and (15) as follows:

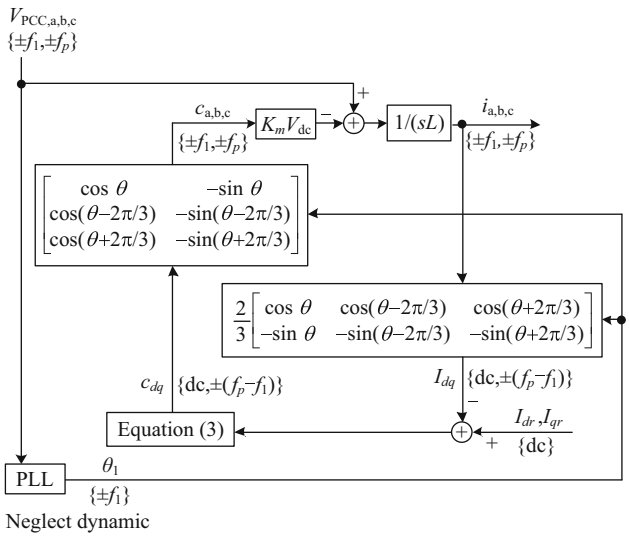


Fig. 3 Signal flow diagram of positive sequence harmonic voltage

$$C_a[\pm f_p] = C_d[\pm(f_p - f_1)]\cos\ \theta_{PLL}[\pm f_1] - C_q[\pm(f_p - f_1)]\sin\ \theta_{PLL}[\pm f_1] \quad (16)$$

where $C_a[\pm f_p]$ corresponds to c_a at $\pm f_p$ in the frequency domain, $C_d[\pm(f_p - f_1)]$ corresponds to c_d at $\pm(f_p - f_1)$ in the frequency domain, and $C_q[\pm(f_p - f_1)]$ corresponds to c_q at $\pm(f_p - f_1)$ in the frequency domain. θ_{PLL} corresponds to θ_{PLL}in the frequency domain.

Thus, the positive sequence admittance of the converter, neglecting the effect of the PLL, can be obtained by (2)–(4), (6), (8)–(12) and (16) as follows:

$$Y_p(s) = \frac{V_a[f_p]}{-I_a[f_p]} = \frac{1}{K_m V_{dc}[H_i(s - j2\pi f_1) - jK_d]G_i(s) + sL} \quad (17)$$

Similarly, the negative sequence admittance is as follows:

$$Y_n(s) = \frac{1}{K_m V_{dc}[H_i(s + j2\pi f_1) + jK_d]G_i(s) + sL} \quad (18)$$

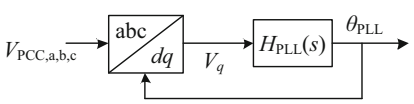
However, a disturbance will be introduced at the output of the PLL due to the grid voltage, and this leads to nonlinearity in the Park Transform. So, the effect of PLL should be taken into consideration when modeling the admittance of the VSCs.

Figure 4(a) illustrates the principle of the PLL. H_{PLL} is the forward loop gain. The harmonic voltage at the PCC will disturb the output of the PLL, and in order to get an accurate admittance of the converter, the disturbance must be modeled precisely. Assume that the disturbance of the output phase, $\Delta\theta$, is a small disturbance around the rated operating point of the VSC system. The output phase of the PLL in the time domain is

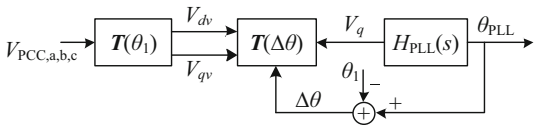
$$\theta_{PLL}(t) = \theta_1(t) + \Delta\theta(t) \quad (19)$$

Therefore, the output phase of the PLL in the frequency domain is:

$$\theta_{PLL}[f] = \begin{cases} \theta_1 & f = \pm f_1 \\ \Delta\theta & \text{At other frequency} \end{cases} \quad (20)$$



(a) Working principle of PLL



(b) Equivalent signal flow diagram of PLL

Fig. 4 PLL working principle and its equivalent diagram

Define $\boldsymbol{T}(\theta)$ to be the matrix of the Park Transformation using the angle θ. The relationship between $\boldsymbol{T}(\theta_{PLL})$ and $\boldsymbol{T}(\theta_1)$ is:

$$\boldsymbol{T}(\theta_{PLL}) = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) & 0 \\ -\sin(\Delta\theta) & \cos(\Delta\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \boldsymbol{T}(\theta_1) \quad (21)$$

and the equivalent signal flow diagram of the PLL can be drawn as shown in Fig. 4b.

The V_{dv} and V_{qv} are the d-axis and q-axis components of the PCC voltage through the ideal Park Transformation. So the real q-axis component is:

$$V_q = V_{qv}\cos\ \Delta\theta - V_{dv}\sin\ \Delta\theta \quad (22)$$

Linearizing (22) gives

$$V_q \approx V_{qv} - V_{dv}\Delta\theta \quad (23)$$

The equations of V_{dv} and V_{qv} in the frequency domain are obtained by Park Transformation and (6) as follows:

$$V_{dv}[f] = \begin{cases} V_1 & \text{dc} \\ G_v(s \pm j2\pi f_1)V_p & f = \pm(f_p - f_1) \\ G_v(s \mp j2\pi f_1)V_n & f = \pm(f_n + f_1) \end{cases} \quad (24)$$

$$V_{qv}[f] = \begin{cases} \mp jG_v(s \pm j2\pi f_1)V_p & f = \pm(f_p - f_1) \\ \pm jG_v(s \mp j2\pi f_1)V_n & f = \pm(f_n + f_1) \end{cases} \quad (25)$$

where G_v is the delay of voltage sampling as follows:

$$G_v(s) = e^{-sT_v}\frac{1 - e^{-sT_v}}{sT_v}\frac{1}{1 + s/\omega_v}\frac{1}{1 + s/\omega_{tv}} \quad (26)$$

where T_v is the period of voltage sampling; ω_v is the cut-off frequency of the analog-digital converter; ω_{tv} represents the delay of transducer.

Thus, the equation of $\Delta\theta$ in the frequency domain is

$$\Delta\theta[f] = \begin{cases} G_p(s)G_v(s \pm j2\pi f_1)V_p & f = \pm(f_p - f_1) \\ G_n(s)G_v(s \mp j2\pi f_1)V_n & f = \pm(f_n + f_1) \end{cases} \quad (27)$$

where $G_p(s)$ is the transfer function of the disturbance which is caused by the positive sequence harmonic voltage V_p at the frequency $\pm(f_p - f_1)$, and $G_n(s)$ is the transfer function of the disturbance which is caused by the negative sequence harmonic voltage V_n at the frequency $\pm(f_n + f_1)$. The equation for V_q in the frequency domain is obtained from (23–27) is as follows:

$$V_q[f] = \begin{cases} [\mp \mathrm{j} - V_1 G_p(s)] G_v(s \pm \mathrm{j}2\pi f_1) V_p & f = \pm(f_p - f_1) \\ [\pm \mathrm{j} - V_1 G_n(s)] G_v(s \mp \mathrm{j}2\pi f_1) V_n & f = \pm(f_n + f_1) \end{cases} \tag{28}$$

Thus, in Fig.4b, the phase angle is

$$\theta_{\mathrm{PLL}}(s) = H_{\mathrm{PLL}}(s) V_q \tag{29}$$

and so

$$\Delta\theta = H_{\mathrm{PLL}}(s) V_q \qquad f \neq \pm f_1 \tag{30}$$

Thus, the equations of $G_p(s)$ and $G_n(s)$ are obtained from (27–30) as follows:

$$G_p(s) = \frac{\mp \mathrm{j} H_{\mathrm{PLL}}(\mathrm{s})}{1 + V_1 H_{\mathrm{PLL}}(s)} \tag{31}$$

$$G_n(s) = \frac{\pm \mathrm{j} H_{\mathrm{PLL}}(\mathrm{s})}{1 + V_1 H_{\mathrm{PLL}}(s)} \tag{32}$$

Because

$$\begin{cases} \cos\theta_{\mathrm{PLL}} = \cos\theta_1 - \sin\theta_1 \cdot \Delta\theta \\ \sin\theta_{\mathrm{PLL}} = \sin\theta_1 + \cos\theta_1 \cdot \Delta\theta \end{cases} \tag{33}$$

the equations of $\cos\ \theta_{\mathrm{PLL}}$ and $\sin\theta_{\mathrm{PLL}}$ in the frequency domain are as follows:

$$\cos\ \theta_{\mathrm{PLL}}[f] = \begin{cases} \frac{1}{2} \frac{H_{\mathrm{PLL}}(s \mp \mathrm{j}2\pi f_1) G_v(s)}{1 + V_1 H_{\mathrm{PLL}}(s \mp \mathrm{j}2\pi f_1)} V_p & f = \pm f_p \\ \frac{1}{2} \frac{H_{\mathrm{PLL}}(s \pm \mathrm{j}2\pi f_1) G_v(s)}{1 + V_1 H_{\mathrm{PLL}}(s \pm \mathrm{j}2\pi f_1)} V_n & f = \pm f_n \end{cases} \tag{34}$$

$$\sin\ \theta_{\mathrm{PLL}}[f] = \begin{cases} \frac{1}{2} \frac{\mp \mathrm{j} H_{\mathrm{PLL}}(s \mp \mathrm{j}2\pi f_1) G_v(s)}{1 + V_1 H_{\mathrm{PLL}}(s \mp \mathrm{j}2\pi f_1)} V_p & f = \pm f_p \\ \frac{1}{2} \frac{\pm \mathrm{j} H_{\mathrm{PLL}}(s \pm \mathrm{j}2\pi f_1) G_v(s)}{1 + V_1 H_{\mathrm{PLL}}(s \pm \mathrm{j}2\pi f_1)} V_n & f = \pm f_n \end{cases} \tag{35}$$

I_{dv} and $I_{qv}$are the d-axis and q-axis components of $i_{\mathrm{a}}(t)$ in the time domain after applying the ideal Park Transformation $\boldsymbol{T}(\theta_1)$. According to (21),

$$\begin{cases} I_d = I_{dv} + \Delta\theta I_{qv} \\ I_q = -\Delta\theta I_{dv} + I_{qv} \end{cases} \tag{36}$$

Thus, the realistic d-axis and q-axis current components I_d and I_q at the frequency $\pm(f_p - f_1)$ and $\pm(f_n + f_1)$ may be obtained, and are given by (A1) in Appendix A.

Table 1 Relationship of frequency components

$C_d[f]$, $C_q[f]$	$\boldsymbol{T}^{-1}(\theta_{\mathrm{PLL}})$	$C_{\mathrm{a}}[f]$, $C_{\mathrm{b}}[f]$, $C_{\mathrm{c}}[f]$
dc	$\pm f_p$	$\pm f_p$
$\pm (f_p - f_1)$	$\pm f_1$	$\pm f_p$

The convolution of the frequency components of the inner current controller signals c_{a}, c_{b} and c_{c} at the frequency $\pm f_p$ is shown in Table 1. Given these, the equation of the inner current control signal of phase A at the frequency $\pm f_p$ can be derived from (4) as follows:

$$\begin{aligned} C_{\mathrm{a}}[\pm f_p] &= \sum C_{dq}[f] \boldsymbol{T}^{-1}(\theta_{\mathrm{PLL}})[\pm f_p - f] \\ &= C_{dq}[\mathrm{dc}] \boldsymbol{T}^{-1}(\theta_{\mathrm{PLL}})[\pm f_p] + C_{dq}[\pm(f_p - f_1)] \boldsymbol{T}^{-1}(\theta_{\mathrm{PLL}})[\pm f_1] \\ &= C_d[\mathrm{dc}] \cos\theta_{\mathrm{PLL}}[\pm f_p] - C_q[\mathrm{dc}] \sin\theta_{\mathrm{PLL}}[\pm f_p] \\ &\quad + C_d[\pm(f_p - f_1)] \cos\theta_{\mathrm{PLL}}[\pm f_1] - C_q[\pm(f_p - f_1)] \sin\theta_{\mathrm{PLL}}[\pm f_1] \end{aligned} \tag{37}$$

where $\boldsymbol{T}^{-1}$ denotes the inverse Park Transformation.

The positive sequence admittance of the converter can be obtained from (2–4), (31), (32), (34), (35), (A1) and (37) as follows:

$$\begin{aligned} Y_p(s) = \Big\{ & 1 - K_m V_{\mathrm{dc}} G_v(s) H_{\mathrm{PLL}}(s - \mathrm{j}2\pi f_1)[1 + V_1 H_{\mathrm{PLL}}(s - \mathrm{j}2\pi f_1)]^{-1} \\ & \cdot \left[(C_1/2) \mathrm{e}^{\mathrm{j}\varphi_{c1}} + (I_1/2) \mathrm{e}^{\mathrm{j}\varphi_{i1}} (H_i(s - \mathrm{j}2\pi f_1) - jK_d) \right] \Big\} \\ & \cdot [K_m V_{\mathrm{dc}} [H_i(s - \mathrm{j}2\pi f_1) - \mathrm{j}K_d] G_i(s) + sL]^{-1} \end{aligned} \tag{38}$$

Similarly, the negative sequence admittance is as follows:

$$\begin{aligned} Y_n(s) = \Big\{ & 1 - K_m V_{\mathrm{dc}} G_v(s) H_{\mathrm{PLL}}(s + \mathrm{j}2\pi f_1)[1 + V_1 H_{\mathrm{PLL}}(s + \mathrm{j}2\pi f_1)]^{-1} \\ & \cdot \left[(C_1/2) \mathrm{e}^{-\mathrm{j}\varphi_{c1}} + (I_1/2) \mathrm{e}^{-\mathrm{j}\varphi_{i1}} (H_i(s + \mathrm{j}2\pi f_1) + \mathrm{j}K_d) \right] \Big\} \\ & \cdot \{K_m V_{\mathrm{dc}} [H_i(s + \mathrm{j}2\pi f_1) + \mathrm{j}K_d] G_i(s) + sL\}^{-1} \end{aligned} \tag{39}$$

where $(C_1/2)\mathrm{e}^{\pm \mathrm{j}\varphi_{c1}} = (C_d[\mathrm{dc}] \pm \mathrm{j}C_q[\mathrm{dc}])/2 = C_1$ and $C_1 = (V_1 + \mathrm{j}2\pi f_1 I_1)/K_m V_{\mathrm{dc}}$.

2.3 Proposed sequence admittance modeling for unbalanced grid conditions

Reference [21] proposes a modeling method for the sequence impedance of VSCs under balanced grid conditions using harmonic linearization. All variables of the system are transformed into the frequency domain firstly, such that V_1 represents $V_{\mathrm{PCC,a}}$ at $\pm f_1$ and V_p represents $V_{\mathrm{PCC,a}}$ at $\pm f_p$, and so on. Then, the output disturbance of the PLL due to the harmonic voltage can be modeled as shown in (27–35). This establishes the use of the Park Transformation considering the effect of $\Delta\theta$, which is applied below under unbalanced grid conditions. Then, the realistic d-axis and q-axis current I_d and I_q are obtained in (A1). These allow the output signal of the inner current controller in dq-frame to be easily calculated using (3). Finally, the output signal of the inner current controller c_{a} at the relevant harmonic frequency ($\pm f_p$ or $\pm f_n$) can be calculated as shown in (37), which is derived using the convolution relationships in Table 1 and the inverse Park Transform. The sequence admittance can be obtained by

putting the calculated C_a into the circuit equation of the system as shown in (2).

The modeling process for the sequence admittance of VSCs under unbalanced grid conditions is nearly the same as the process above. The unbalanced grid voltage can be introduced as a new variable in the original model. The unbalanced grid voltage V_2 will lead to new frequency components of $\Delta\theta$ such as $\Delta\theta[\pm 2f_1]$. It will also introduce a new frequency component in the Park Transformation at the fundamental negative frequency as shown in Fig. 5. The unbalanced grid voltage V_2 generates an unbalanced output current I_2 from the VSC at the fundamental negative frequency. Then, $I_{dq}[\pm 2f_1]$ will be generated by the Park Transformation. Due to the existence of $\Delta\theta[\pm 2f_1]$, some new frequency components such as $I_{dq}[\pm(f_p+f_1)]$, $I_{dq}[\pm(f_n-f_1)]$, and so on, will be introduced when calculating I_d and I_q.

Then, the output signals of the inner current controller in the dq-frame can be easily obtained. In order to compare with the balanced condition, some new frequency components such as $C_{dq}[\pm(f_p+f_1)]$, $C_{dq}[\pm(f_n-f_1)]$ and $C_{dq}[\pm 2f_1]$ will be introduced. C_a can be calculated at the relevant frequencies such as $\pm f_p$ and $\pm f_n$ by considering all the possible convolution relationships of the frequency components.

Therefore, there are some new elements in C_a due to the unbalanced grid voltage V_2. By putting the positive and negative components of C_a into each sequence circuit equations of the system, and solving them, the sequence admittance of VSCs can be obtained. The detailed step-by-step calculation is shown in Section 3.

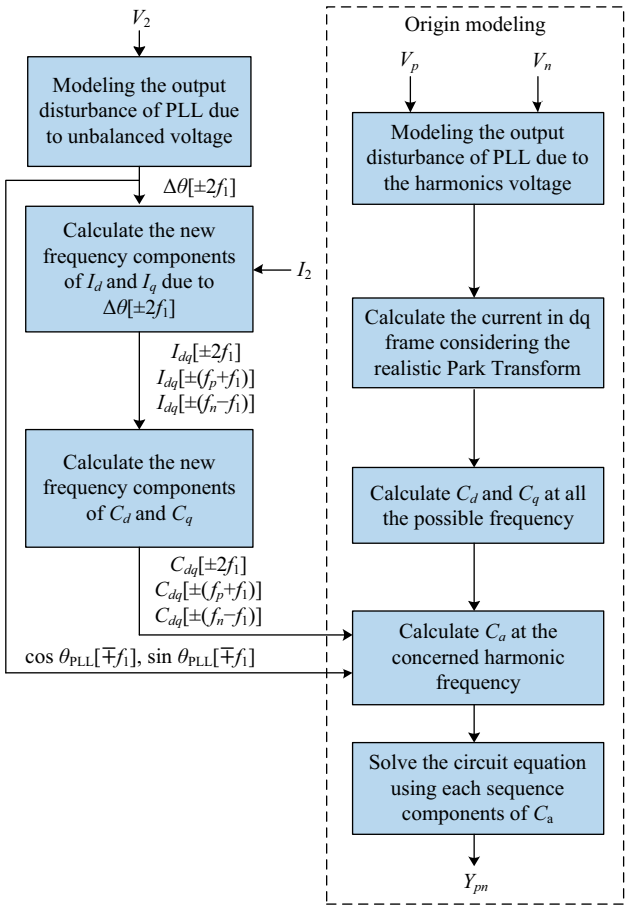


Fig. 5 The proposed method to obtain the admittance model by harmonic linearization

3 Step-by-step admittance calculation of VSCs under unbalanced grid conditions

The converter is often running with unbalanced grid voltage on the grid side. There is not only the rated positive sequence voltage at the fundamental frequency, but also the negative sequence voltage at the fundamental frequency exists in the voltage at PCC. Assume that the equation of the voltage of phase A is:

$$\begin{aligned} V_{\mathrm{PCC,a}} = {} & V_1\cos(2\pi f_1 t)+V_2\cos(2\pi f_1 t+\varphi_2) \\ & + V_p\cos(2\pi f_p t+\varphi_p)+V_n\cos(2\pi f_n t+\varphi_n) \end{aligned} \tag{40}$$

where the V_2 and φ_2 correspond to the magnitude and the initial phase of the negative sequence voltage at the fundamental frequency. Similarly, the equation of the current of phase A in the time domain is as follows:

$$\begin{aligned} i_{\mathrm{a}} = {} & I_1\cos(2\pi f_1 t+\varphi_{i1})+I_2\cos(2\pi f_1 t+\varphi_{i2}) \\ & + I_p\cos(2\pi f_p t+\varphi_{ip})+I_n\cos(2\pi f_n t+\varphi_{in}) \end{aligned} \tag{41}$$

where I_1 and φ_{i2} correspond to the magnitude and initial phase of the negative sequence current at the fundamental frequency.

The detailed steps to obtain the admittance model by harmonic linearization considering the effect of the negative sequence voltage at the fundamental frequency are shown in Fig. 6.

Thus, we can find $C_a[f]$ which is the phase A output control signal of the inner current controller in the frequency domain.

The sequence components and their convolution relationships are shown in Table 2. Clearly, the positive sequence harmonic voltage at the frequency $\pm f_p$ produces not only the positive sequence harmonic component, but also the negative sequence harmonic voltage at the same frequency. Similarly, the negative sequence harmonic voltage at the frequency $\pm f_n$ produces not only the negative sequence harmonic component, but also the positive sequence harmonic voltage at the same frequency. The positive and negative sequence harmonic components couple with each other because of the negative sequence

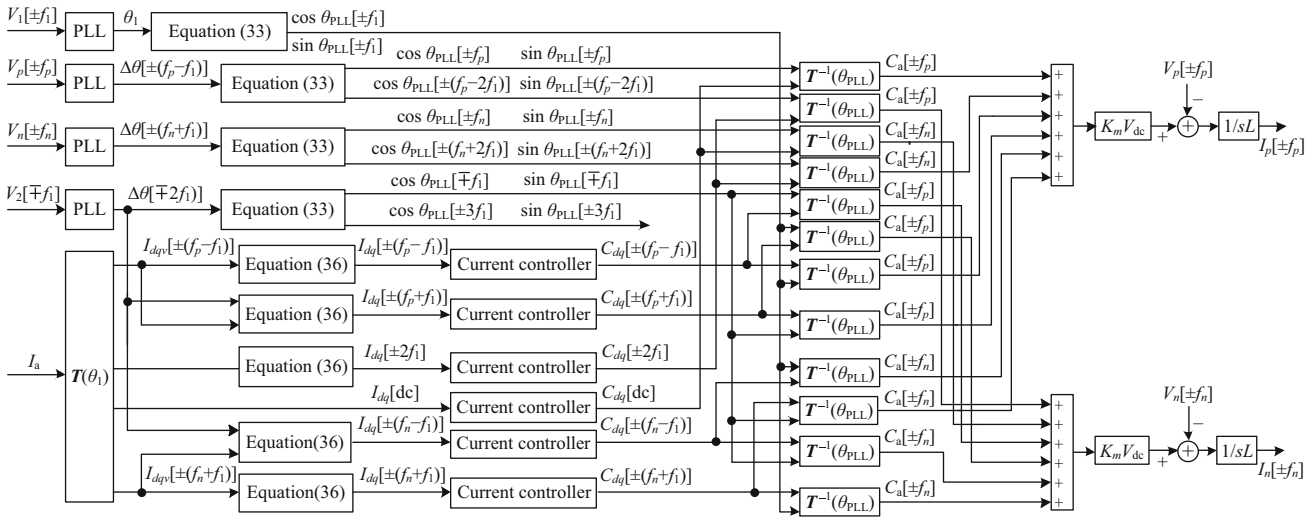


Fig. 6 Step-by-step detailed process to obtain impedance model with unbalanced grid voltage by harmonic linearization

Table 2 Convolution relationship of frequency components

$C_d[f]$, $C_q[f]$	$T^{-1}(\theta_{PLL})$	$C_a[f]$, $C_b[f]$, $C_c[f]$	Sequence
dc	$\pm f_p$	$\pm f_p$	Positive
dc	$\pm f_n$	$\pm f_n$	Negative
$\pm(f_p-f_1)$	$\pm f_1$	$\pm f_p$	Positive
$\pm(f_p-f_1)$	$\mp f_1$	$\pm f_p$	Negative
$\pm(f_n+f_1)$	$\pm f_1$	$\pm f_n$	Negative
$\pm(f_n+f_1)$	$\mp f_1$	$\pm f_n$	Positive
$\pm(f_p+f_1)$	$\pm f_1$	$\pm f_p$	Negative
$\pm(f_p+f_1)$	$\mp f_1$	$\pm f_p$	Positive
$\pm(f_n-f_1)$	$\pm f_1$	$\pm f_n$	Positive
$\pm(f_n-f_1)$	$\mp f_1$	$\pm f_n$	Negative
$\pm 2f_1$	$\pm(f_p-2f_1)$	$\pm f_p$	Negative
$\pm 2f_1$	$\pm(f_n+2f_1)$	$\pm f_n$	Positive

voltage at the fundamental frequency. The positive and negative sequence equation of the system is obtained from (2) as follows:

$$sL\begin{bmatrix} I_p \\ I_n \end{bmatrix} = K_m V_{dc}\begin{bmatrix} C_{a,p} \\ C_{a,n} \end{bmatrix} - \begin{bmatrix} V_p \\ V_n \end{bmatrix} \tag{42}$$

where $C_{a,p}$ and $C_{a,n}$ are the positive and negative sequence components of $\boldsymbol{C}_a$ respectively.

This can be expressed as follows:

$$\begin{bmatrix} A_{pp} & A_{pn} \\ A_{np} & A_{nn} \end{bmatrix}\begin{bmatrix} I_p \\ I_n \end{bmatrix} = \begin{bmatrix} B_{pp} & B_{pn} \\ B_{np} & B_{nn} \end{bmatrix}\begin{bmatrix} V_p \\ V_n \end{bmatrix} \tag{43}$$

where the equations of A_{pp}, A_{pn}, A_{np}, A_{nn}, B_{pp}, B_{pn}, B_{np} and B_{nn} are obtained by solving (43).

Equation (43) can be written in matrix form as: $\boldsymbol{A}_{pn}\boldsymbol{I}_{pn} = \boldsymbol{B}_{pn}\boldsymbol{V}_{pn}$. Thus,

$$\begin{cases} \boldsymbol{I}_{pn} = -\boldsymbol{Y}_{pn}\boldsymbol{V}_{pn} = \boldsymbol{A}_{pn}^{-1}\boldsymbol{B}_{pn}\boldsymbol{V}_{pn} \\ \boldsymbol{V}_{pn} = -\boldsymbol{Z}_{pn}\boldsymbol{I}_{pn} = \boldsymbol{B}_{pn}^{-1}\boldsymbol{A}_{pn}\boldsymbol{I}_{pn} \end{cases} \tag{44}$$

where $\boldsymbol{Z}_{pn}$ corresponds to the positive and negative output impedance matrix of the converter under the unbalanced condition, and $\boldsymbol{Y}_{pn}$ is the admittance matrix corresponding to $\boldsymbol{Z}_{pn}$.

Assume that:

$$\boldsymbol{Y}_{pn} = \begin{bmatrix} Y_{pp} & Y_{pn} \\ Y_{np} & Y_{nn} \end{bmatrix} \tag{45}$$

and then according to (44) the admittance matrix $\boldsymbol{Y}_{pn}$ can be obtained as follows:

$$\begin{cases} Y_{pp} = -\dfrac{A_{nn}B_{pp} - A_{pn}B_{np}}{A_{pp}A_{nn} - A_{pn}A_{np}} = -\dfrac{B_{pp}}{A_{pp}} \\ Y_{pn} = -\dfrac{A_{nn}B_{pn} - A_{pn}B_{nn}}{A_{pp}A_{nn} - A_{pn}A_{np}} = -\dfrac{B_{pn}}{A_{pp}} \\ Y_{np} = -\dfrac{-A_{np}B_{pp} + A_{pp}B_{np}}{A_{pp}A_{nn} - A_{pn}A_{np}} = -\dfrac{B_{np}}{A_{nn}} \\ Y_{nn} = -\dfrac{-A_{np}B_{pn} + A_{pp}B_{nn}}{A_{pp}A_{nn} - A_{pn}A_{np}} = -\dfrac{B_{nn}}{A_{nn}} \end{cases} \tag{46}$$

4 Simulations and verifications

4.1 Detailed circuit simulations

In order to prove the validity of the calculated admittance, cycle-by-cycle simulations have been carried out in Matlab Simulink. The circuit used in the simulations is shown in Fig. 7. The part shown as the "Converter" in Fig. 7 contains the whole control system.

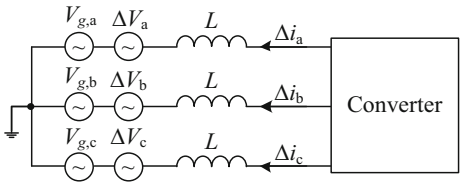


Fig. 7 Simulation circuit

ΔV in Fig. 7 is a small perturbance of voltage on the grid side, and Δi is the variation of the current. The simulation parameters are shown in Table 3. The magnitude of the unbalanced voltage at the fundamental frequency is 0.1 p.u. The delay of the whole control loop can be considered as a sum of time delays. Then the time delay representing the whole control loop of the system can be set to model different practical applications.

Figures 8, 9, 10 and 11 compare simulated with calculated result to verify the correctness of the equation of $\boldsymbol{Y}_{pn}$. The root-mean-square (RMS) difference in magnitude is 1.07 dB and the RMS phase difference is 2.56°, suggesting that we may have high confidence in the equation.

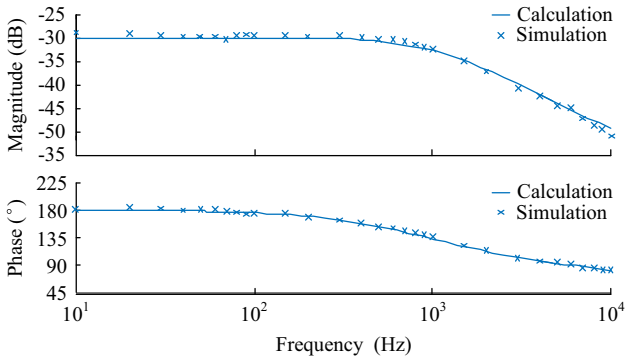


Fig. 8 Simulation and calculation results of Y_{pp}

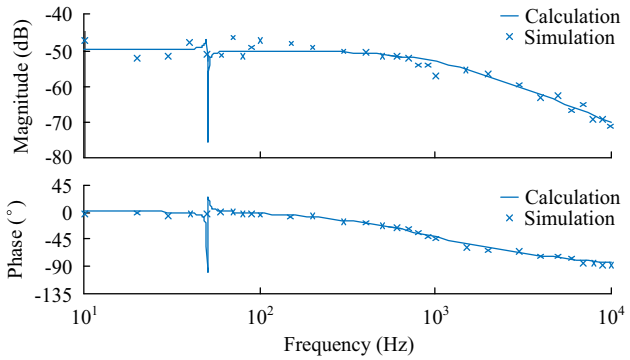


Fig. 9 Simulation and calculation results of Y_{pn}

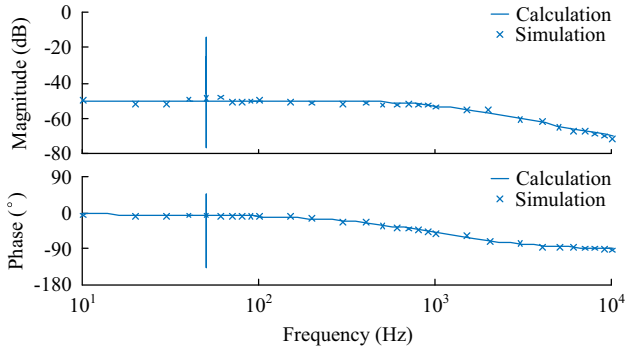


Fig. 10 Simulation and calculation results of Y_{np}

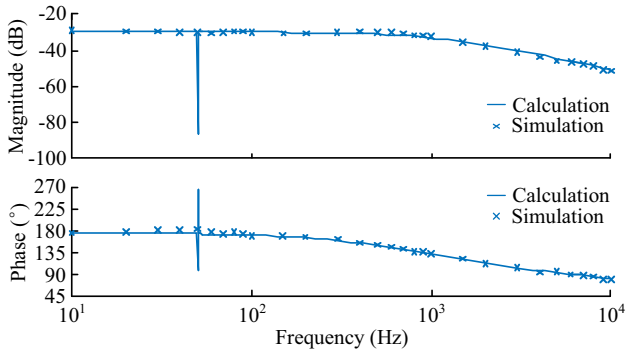


Fig. 11 Simulation and calculation results of Y_{nn}

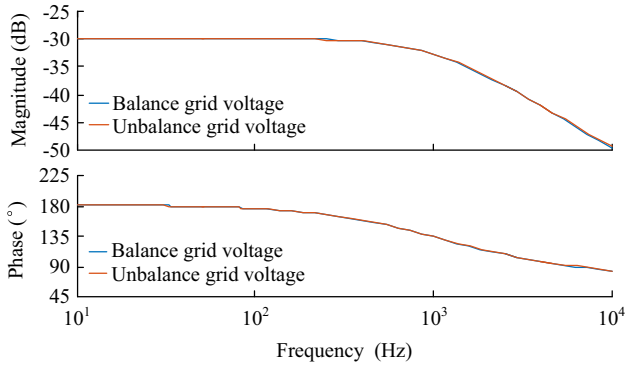


Fig. 12 Comparison of Y_{pp} under normal conditions and with unbalanced grid voltage

4.2 Sensitivity analysis

Figures 12 and 13 compare the positive and negative admittances under normal conditions and with unbalanced grid voltage. It can be seen that the admittances in these two situations are nearly the same. The unbalanced voltage has little effect on the positive and negative admittances, but it will produce coupled admittances.

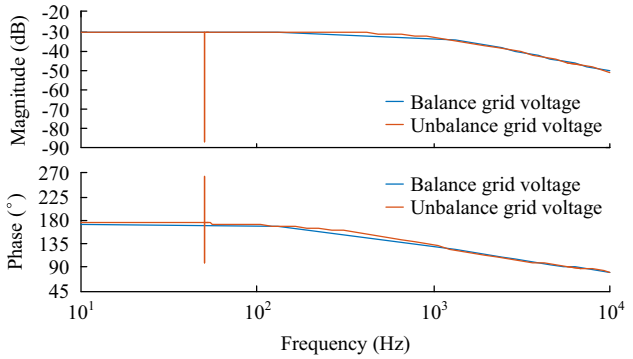


Fig. 13 Comparison of Y_{nn} under normal conditions and with unbalanced grid voltage

According to Fig. 5, the unbalanced grid voltage V_2 will lead to a new frequency component of $\Delta\theta$ such as $\Delta\theta[\pm 2f_1]$. Due to the existence of $\Delta\theta[\pm 2f_1]$, the coupled admittance will be introduced. The relationship between $\Delta\theta[\pm 2f_1]$ and V_2 is:

$$\Delta\theta[\pm 2f_1] = \pm \mathrm{j}\frac{H_{\mathrm{PLL}}(\pm 2f_1)}{1 + V_1 H_{\mathrm{PLL}}(\pm 2f_1)} G_v(\pm f_1) V_2 \tag{47}$$

This indicates that the magnitude of V_2 and the transfer function of the PLL will have big impacts on the coupled admittances. The transfer function of the PLL determines its bandwidth.

Figure 14 shows the variation of the magnitude of the coupled admittance Y_{np} of the simulated VSC with different magnitudes of V_2. All other parameters are as shown in Table 3. It can be seen that the increased magnitude of the negative sequence voltage at the fundamental frequency will lead to an increased coupled admittance of the VSC.

Figure 15 illustrates the coupled admittance Y_{np} of the VSC with a lower PLL bandwidth. All the parameters are as shown in Table 3 except for the smaller proportionality

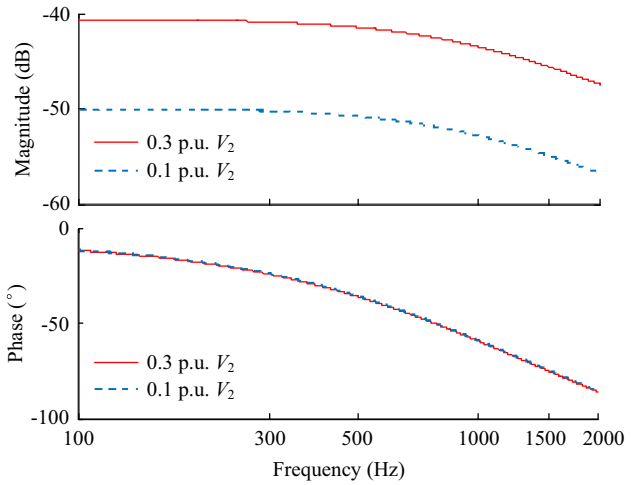


Fig. 14 Coupled admittance Y_{np} of VSC with different magnitude of V_2

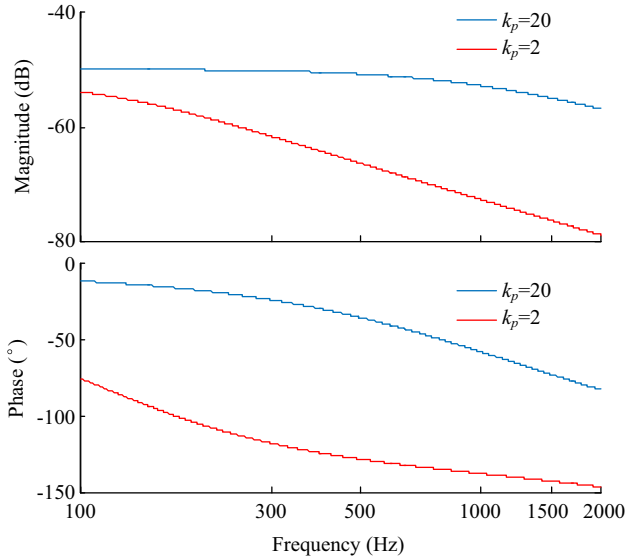


Fig. 15 Coupled admittance Y_{np} of VSC with different bandwidth of PLL

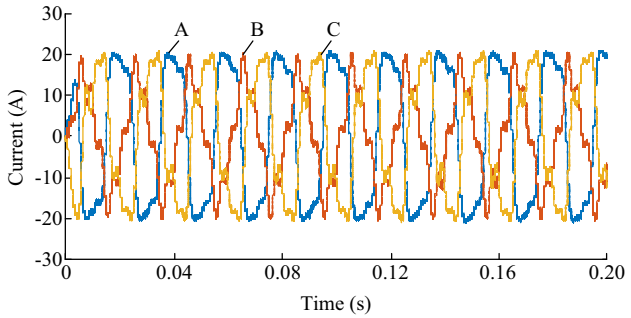


Fig. 16 Distorted output currents of VSC with a lower PLL bandwidth

coefficient k_p of the PLL. When it is set as 2, representing a lower bandwidth of PLL, Fig. 15 illustrates that the phase and magnitude of Y_{np} decrease significantly. This suggests that a lower bandwidth of the PLL will lead to a decrease of the phase and magnitude of Y_{np}.

In [23], the sufficient criterion for stability of the converter according to its admittance is that the real part of the admittance of the VSC is above zero. Figure 16 shows that the output currents of the VSC with lower PLL bandwidth distort severely, which can be attributed to negative real parts of the coupled admittances for the central frequency. This means that a lower bandwidth of the PLL will decrease the phase and magnitude of Y_{np} and lead to the distortion of the output currents.

Table 3 Parameters of system

Symbol	Description	Value
V_{dc}	Magnitude of DC side voltage	800 V
V_1	Magnitude of fundamental positive sequence voltage at frequency f_1	311 V
V_2	Magnitude of fundamental negative sequence voltage at frequency f_1	31.1 V
I_1	Magnitude of fundamental positive sequence current at frequency f_1	20 A
φ_{i1}	Initial phase of I_1	0°
L	Inductance of output filter	3 mH
T_m	Period of voltage and current sampling	50 μs
ω_m	Cut-off frequency of analog-digital converter	10 kHz
K_m	Modulator gain	0.5
H_i	Proportionality coefficient of compensation factor of inner current controller	5
	Integral coefficient of compensation factor of inner current controller	15
H_{PLL}	Proportionality coefficient of forward loop gain of PLL	20
	Integral coefficient of forward loop gain of PLL	5
K_d	Decoupling factor of inner current controller	0.9425

5 Conclusion

The sequence admittances of a three-phase VSC are independent of each other when it is operating under normal conditions. However, the positive and negative sequence harmonic components will be coupled with each other if three-phase grid-connected converter is running with unbalanced grid voltages. This is mainly caused by the negative sequence voltage at the fundamental frequency. This paper proposes a step-by-step modeling method to calculate the matrix of positive and negative sequence admittances of three-phase grid-connected converters under unbalanced grid voltage conditions, based on the method of harmonic linearization. The calculated admittances agree with simulated results within 1.07 dB of magnitude and 2.56° of phase, and can be easily applied in stability analysis.

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Appendix A

By inserting (9–12) into (36), the realistic d-axis and q-axis components of currents I_d and I_q can be obtained as follows:

$$\begin{cases} I_d[\pm(f_p-f_1)] = I_{dv}[\pm(f_p-f_1)]+\Delta\theta[\pm(f_p-f_1)]I_{qv}[\mathrm{dc}] \\ \quad = G_i(\pm j2\pi f_p)I_p + I_1\sin\ \varphi_{i1}G_v(\pm j2\pi f_p) \\ \quad G_p(\pm j2\pi(f_p-f_1))V_p \\ I_q[\pm(f_p-f_1)] = I_{qv}[\pm(f_p-f_1)] - \Delta\theta[\pm(f_p-f_1)]I_{dv}[\mathrm{dc}] \\ \quad = \mp\mathrm{j}G_i(\pm j2\pi f_p)I_p - I_1\cos\ \varphi_{i1}G_v(\pm j2\pi f_p) \\ \quad G_p(\pm j2\pi(f_p-f_1))V_p \\ I_d[\pm(f_n+f_1)] = I_{dv}[\pm(f_n+f_1)]+\Delta\theta[\pm(f_n+f_1)]I_{qv}[\mathrm{dc}] \\ \quad = G_i(\pm j2\pi f_n)I_n + I_1\sin\ \varphi_{i1}G_n(\pm j2\pi(f_n+f_1)) \\ \quad G_v(\pm j2\pi f_n)V_n \\ I_q[\pm(f_n+f_1)] = I_{qv}[\pm(f_n+f_1)] - \Delta\theta[\pm(f_n+f_1)]I_{dv}[\mathrm{dc}] \\ \quad = \pm\mathrm{j}G_i(\pm j2\pi f_n)I_n - I_1\cos\ \varphi_{i1}G_n(\pm j2\pi(f_n+f_1)) \\ \quad G_v(\pm j2\pi f_n)V_n \end{cases} \tag{A1}$$

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