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Guest Editorial: Low-Voltage Integrated Circuits and Systems

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Interest in developing new design techniques for low-voltage integrated circuits and systems has continued over several decades. It is mainly caused by system power constraints and advanced deep submicron technologies, which require lower and lower supply voltages. Since the early 90s, when the supply voltage of 3.3 V was considered as low, the required supply voltages have been constantly decreasing, in some applications dropping (much) below 1 V. Nowadays, as predicted by the *Technology Roadmap for Semiconductors*, we can expect that the supply voltages will be reduced to 0.6 V for high performance microprocessors and 0.54 V for low-power solutions in a near future. Regarding the latter, in some cases even lower V_{DD} can be required, e.g., for circuits supplied with non-conventional energy sources, and devoted to some specific applications, like biomedical implants.

The increasing demand for both the low supply voltage and the energy efficiency often have a detrimental effect, especially upon analog and mixed signal circuits, which

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must operate with reduced voltage headroom and power dissipation. Therefore, the most challenging task for today's designers is to maintain the circuit performances by developing novel circuit structures capable of operating with highly reduced supply voltages. The main goal of this special issue is to present recent advances in the field and the main challenges relating to the theory, design and applications of low-voltage integrated circuits and systems. From 43 submitted manuscripts, a total of 15 papers have been accepted for publication. The papers are arranged to cover four main topics: digital circuits, analog functional blocks, RF circuits, supply and energy harvesting blocks. Below is a summary of the accepted contributions under each of the themes.

1 Digital Circuits

In the paper "High-speed digital domino logic for ultra-low supply voltages," a high-speed differential clocked voltage switch logic inverter operating at ultra-low supply voltages is presented. Simulated data for the new gate as well as preliminary measurements are presented. The increase in speed for supply voltages below 300 mV is between 10 and 20 times compared to modified clocked voltage switch logic. In the paper "An Aging Aware Reliable FinFET-Based Low-Power 32 Word x 32-bit Register File," a reliable FinFET-based low-power 32 word x 32-bit register file in a 32 nm technology is introduced. A novel Aging aware dynamic OR gate is proposed here which is capable of maintaining a constant performance under negative bias temperature instability degradation. This proposed domino bit-line is further used to design a novel register file which is capable of maintaining a constant performance for a lifetime of more than 10 years.

2 Analog Functional Blocks

In the paper "A Low-Voltage PLL Design Using a New Calibration Technique for Low-Power Implantable Biomedical Systems," a low-voltage phase-locked loop (PLL) design using a new calibration technique for low-power implantable biomedical systems is described. The proposed PLL uses a switching technique in the charge pump and a bulk-driven technique in the voltage-controlled oscillator to reduce power consumption and operate at ultra-low voltage. In the paper "An ultra-low-energy analog comparator for A/D converters in CMOS image sensors," a new solution of an ultra-low-energy analog comparator, dedicated to slope analog-to-digital converters (ADC), particularly suited for CMOS image sensors featuring a large number of ADCs is proposed. In the paper "Ultra-low-Voltage Integrable Electronic Realization of Integer and Fractional-order Liao's Chaotic Delayed Neuron Model," an ultra-low-voltage sinh-domain implementation of the neuron model is introduced. Moreover, for the first time, the fractional-order implementation of the model is presented. In the paper "Active current mirrors for low voltage analog circuit design," active current mirrors using sensing resistors and a pass transistor in a feedback loop are examined in detail. First, several non-idealities in this family of circuits like offset, noise, output impedance or bandwidth are addressed, showing no performance degradation under certain circumstances. Then, the design and measurement results of a 10 μA (nominal)

active current mirror that can operate down to just 80 mV voltage drop are presented. In the paper "An Ultra-Low-Voltage Bulk-Driven Analog Voltage Buffer with Rail-to-Rail Input/Output Range," a low-voltage high driving capability rail-to-rail Class-AB CMOS bulk-driven operational transconductance amplifier (OTA) for analog voltage buffer with minimal current consumption is presented. The proposed OTA design consists of adaptively-biased Class-AB differential input stage to improve the effective transconductance and adaptive load relying on nonlinear current mirrors, configured in partial positive feedback mode to enhance the overall gain. In the paper "An accurate CMOS interface small capacitance variation sensing circuit for capacitive MEMS sensor applications," an accurate front-end CMOS interface circuit for sensing very small capacitance changes in capacitive sensors is presented. Finally, in the paper "Design and Analysis of an Ultra-Low-Power Second-Order Asynchronous Delta–Sigma Modulator," a second-order asynchronous delta–sigma modulator based on the active RC integrators and operating from supply voltage of 0.25 V is proposed. The OTAs used in the integrators are improved by employing a class-AB structure with bulk-driven input drivers and quasi-floating gate method in subthreshold region. These circuit approaches provide better linearity, signal-to-noise ratio and speed for the integrators, resulting in an overall improvement in the performance of the modulator.

3 RF Circuits

In the paper "Integrable CMOS-based Current-mode Sinusoidal Frequency and Peak Detector," the research proposes an integrable CMOS current-mode instantaneous frequency and peak detector (FPD) based on the trigonometric relationships and mathematic algorithm without the divider function and low-pass filter. The proposed FPD structure is straightforward, consisting of two differentiators, two multipliers and one square rooter. The FPD was experimentally utilized as the FM and AM demodulators with very satisfactory demodulation outcomes. In the paper "Multi-Objective Low Noise Amplifier Optimization Using Analytical Model and Genetic Computation," a methodology for multi-objective radio frequency (RF) low noise amplifier optimization using an analytical model of the MOS transistor in combination with genetic computation is introduced. In the paper "Analysis and Design of Single Reference Reduced Summer Loading based Switched Capacitor DFE," the design of a switched capacitor decision feedback equalizers for multi-tap post-cursor cancelation with reduced summer loading is addressed. The proposed architecture is validated by post-layout simulations.

4 Supply and Energy Harvesting Blocks

In the paper "A High-Efficiency CMOS Rectifier with Wide Harvesting Range and Wide Band Based on MPPT Technique for Low-Power IoT System Applications," a wide-harvesting-range, wide-band and high-efficiency CMOS rectifier for low-power application in Internet of Things systems is described. Through maximum power point tracking, the proposed rectifier can dynamically detect the output voltage to enable switching between various circuit modes in order to achieve higher power

conversion efficiency, even during sub-1-V operation. In the paper "Design of Fast-Locked Digitally Controlled Low-Dropout Regulator for Ultra-low Voltage Input," a new design for a fast-locked digitally controlled low-dropout regulator for an ultra-low voltage input is proposed. The proposed design involves a fast-locked control mechanism that reduces the settling time of the load transient response in the tracking mode and decreases the quiescent current in the regulating mode. In the paper "A 139 nW, 67 ppm/°C BJT-CMOS-based voltage reference circuit," a low-power voltage reference circuit is developed using the principle that a thermal compensation of the threshold voltage of a diode-connected nMOSFET is obtained by using the PTAT current.

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