Introduction to the January Special Issue on the 2015 IEEE International Solid-State Circuits Conference

I. Introduction

THE IEEE International Solid-State Circuits Conference (ISSCC) is the foremost global forum for presenting advances in solid-state circuits and systems-on-a-chip. Every year since its first issue, the IEEE JOURNAL OF SOLID-STATE CIRCUITS has highlighted some well-received papers from the most recent ISSCC in special issues. This Special Issue covers the ISSCC conference held in San Francisco, CA, USA, on February 22–26, 2015.

This January issue includes topics from energy-efficient digital and high-performance processors; imagers, MEMS, medical, and displays (IMMDs); and memory as well as technology directions' (TDs') sessions.

II. Energy-Efficient Digital

Energy efficiency is becoming the main design driver for both small embedded microcontrollers and multicore platforms. This section first presents a wide range of low-power digital-design techniques implemented in complete ultra-low-power microcontrollers for the Internet-of-Things (IoT), as well as in SoC building blocks exploiting fine-grain DVFS. Innovative on-chip voltage and frequency regulation techniques enable operation across a wide range of supply voltages and PVT variations. The second part of this section highlights recent energy-efficient SoC architectures and design techniques enabling new capabilities to be added to power-sensitive systems. Machine vision processing brings object recognition and visual analytics for human–machine interfaces. New video and communication processors demonstrate energy-efficient and cost-effective designs that implement the newest standards.

The first paper, by Bowman *et al.*, describes a 16 nm adaptive clock distribution integrating an autocalibration circuit to accurately detect supply voltage droops. The autocalibration circuit maximizes the voltage droop tolerance of the adaptive clock distribution while eliminating the overhead from tester calibration. Silicon measurements demonstrate throughput gains ranging from 13% at 0.9 V to 30% at 0.6 V for a 10% voltage droop.

The second paper, by Kim *et al.*, demonstrates a digitally controlled hybrid LDO and switched-capacitor voltage regulator enabling wide autonomous DVFS in a 22 nm graphics execution core. Compared to a shared rail, hybrid voltage regulator enables an 82% reduction in core energy at V_{out} of 0.38 V. Measured data also show a 75% core frequency improvement at 0.84 V V_{out} enabled by fast droop response.

The third paper, by Myers *et al.*, presents an 11.7 pJ/cycle subthreshold ARM cortex-M0+ wireless sensor node processing subsystem implemented in low leakage 65 nm CMOS, scalable from 850 nW active power at 250 mV to 66 MHz at 900 mV and supporting 80 nW CPU and random read access (RAM) state-retention power gating for SW transparent leakage reduction.

The fourth paper, by Hong *et al.*, demonstrates a 3-D stacked gaze image sensor and object recognition processor for a gaze-activated object recognition system in head-mounted displays (HMDs). The low-power gaze image sensor is implemented with focal-plane processing circuits and the object recognition processor is implemented including LUT cores, a neural-network processor, and a DVFS controller. The system consumes only 75 mW of power, which is $3.4\times$ smaller than the previously published state of the art.

The fifth paper, by Ju *et al.*, exhibits the first 4 k high efficiency video coding (HEVC) video codec chip supporting diverse formats implemented on a $1.49 \times 1.45\,\text{mm}^2$ die in 28 nm CMOS. Several fast algorithms are proposed leading to over 80% of complexity reduction. The proposed chip achieves 4096×2160 at 30 fps HEVC encoding/decoding and consumes 126.73 mW, 0.5 nJ/pixel of energy efficiency, under 494 MHz clock frequency, enabling 4 k video conference, and WiFi display for smartphone applications.

Finally, in the sixth paper, Ren *et al.* present an 18.5 mW sparse approximation engine for energy-efficient mobile data aggregation from compressively sampled biomedical signals, integrated in 40 nm CMOS. By using a configurable architecture and an efficient memory mapping scheme, the engine achieves a real-time throughput for reconstructing 50–200 channels of ExG (ECG, EMG, and EEG) simultaneously. For high-sparsity reconstruction, the sparse approximation engine is $44-202\times$ more energy efficient than prior hardware designs.

III. Processors

Exploding data growth and analytics requirements continue to push the performance and power efficiency of microprocessors in today's computing environment. The first three papers in this year's processor session introduce state-of-the-art high-performance microprocessors with increasing core counts, cache size, I/O bandwidth, and advanced power management techniques. These papers describe significant architectural and circuit innovations in various fields from high-end enterprise computing to low-power mobile computing. The last paper features an adaptive and resilient register file that provides increased energy efficiency and flexibility.

The first paper, by Konstadinidis *et al.*, describes the next-generation SPARC M7 processor. With 32 highly optimized S4

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cores and a 1.6 TB/s bandwidth 64 MB L3 cache, the processor delivers more than $3.0\times$ throughput performance improvement over its predecessor. Hardware database analytics accelerator units (DAXs) achieve up to $10\times$ the performance in in-memory database queries. Application data integrity (ADI) supports pointer version checking for securing application data. The chip, fabricated in 20 nm, includes an on-chip network (OCN) with 0.5 TB/s data bandwidth, 280 SerDes lanes with 18 Gb/s line rate, and 1 TB/s total bandwidth.

In the second paper, Bowhill *et al.* report the next-generation Xeon processor featuring 18 dual-threaded 64 b Haswell cores, 45 MB L3 cache, four DDR4-2133 MHz memory channels, 40 8 GT/s PCIe lanes, and 60 9.6 GT/s QuickPath Interconnect (QPI) lanes. It achieves a 33% performance boost with 5.56B transistors in a 22 nm trigate CMOS technology. "Fully integrated voltage regulator" (FIVR) technology enables per-core p-states and independent uncore frequency scaling.

The third paper, by Munger *et al.*, presents their next-generation accelerated processing unit (APU), Carrizo, which includes the latest x86 core, Excavator. Implemented in a 28 nm HKMG process, the SoC occupies 244.62 mm^2 with more than 3.1B transistors. The core occupies 23% less area and dissipates 40% less power compared to the previous design. Improvements in both architecture and power management enable more than 50% reduction in typical energy use.

Finally, in the fourth paper, Kulkarni *et al.* demonstrate an adaptive and resilient register file that uses *in situ* timing margin and error detection techniques to tolerate within-die voltage droop, temperature, and aging. The chip demonstrates 409 GOPS/W operation in 22 nm trigate CMOS to achieve 21% better throughput and 67% more energy efficiency with 6.4%–12.8% area overhead and 0.2%–0.3% power overheads.

IV. Imagers, MEMS, Medical, and Displays

This section includes six innovative papers selected from the three IMMD sessions. The first paper describes a low-power image sensor with a switchable "always-ON" mode for mobile and wearable devices. Two papers present significant milestones in fluorescence lifetime imaging with precise picosecond resolution. Display technology is represented by a 6.5 bit resolution pen pressure sensor that uses a passive resonant stylus, which can replace conventional costly electromagnetic resonance-based touch systems. An electronic stability control technique pushing dynamic range and drift of inertial sensors is followed by a paper on an innovative energy-efficient readout circuit for resonant sensors.

The first paper, by Choi *et al.*, describes a low-power always-ON image sensor for mobile and wearable devices, which enables smart sensing in addition to photograph shooting. The sensor employs switchable always-ON and photo-shooting modes, dynamic voltage scaling, and reconfigurable ADCs. The fabricated 640×480 sensor operates at 45.5 μW at 15 fps, which has a potential of battery lifetime extension in always-ON sensing.

The second paper, by Seo *et al.*, presents a CMOS lock-in pixel image sensor with embedded storage diodes and a lateral electric field charge modulation method for time-resolved imaging. Fluorescence lifetime imaging for cells using the time-resolved image sensor is demonstrated. The fabricated image sensor achieves an extremely precise time resolution of 10 ps, a quick intrinsic response of 180 ps at a wavelength of 374 nm, and a low temporal noise of 1.75e-rms with true correlated double sampling (CDS) operation.

The third paper, by Perenzoni *et al.*, presents an analog counting time-gated single-photon image sensor suitable for fluorescence lifetime imaging applications. The fabricated image sensor with a resolution of 160×120 pixels has been demonstrated in a fluorescence lifetime microscopy setup with a capability to detect single photons with down-to-750 ps time-gating window, featuring programmable width and delay. Stable timing is guaranteed by an internal delay-line loop, while both analog and digital readout modes are available. The digital readout mode has been implemented by a self-referenced column-parallel converter.

For display technology, a pen-pressure-sensing capacitive touch system, presented by Park *et al.,* proposes a resonant frequency sensing scheme for a passive resonant stylus. The system detects the position of stylus and finger based on mutual-capacitance sensing, and also senses the pen pressure. A multiple driving and sensing scheme is proposed with a modified Hadamard matrix for position sensing with improving dynamic range and SNR. The pen pressure sensor detects how much the resonant frequency deviates from a reference frequency to sense small variations of resonant frequency. The measured SNR for stylus location is 49 dB with 1 mm φ and 6.5 bit resolution is achieved for pen pressure sensing.

The fifth paper, by Balachandran *et al.*, describes a three-axis automotive gyroscope ASIC with noise density less than 0.004°/s/Hz in a 80 Hz bandwidth and offset drift less than $\pm 0.1°/s$ over the temperature range of -40 °C to 140 °C The sensor employs a low-overhead approach for implementing accurate continuous safety monitoring to monitor defects, which can develop in the field and can give rise to a false output. Two test signals are injected into the quadrature cancellation loop to traverse the entire signal path with a known gain.

The final paper, by Jiang *et al.*, presents a readout circuit for MEMS resonant sensors in 0.35 μm CMOS process. It employs a dynamically switching level-crossing detector to determine the resonance frequency and quality factor from a single ring-down transient. Results obtained with three different resonators are in good agreement with the conventional impedance analysis. The prototype achieves a frequency resolution better than 30 ppm while consuming less than 80 nJ per measurement in a supply voltage of 1.8 V.

V. Memory

Five papers were selected from this year's sessions on non-volatile and embedded memories. These papers describe significant innovations in the field, including 64 Gb MLC NAND Flash, 128 Gb 3b/cell V-NAND Flash, 28 nm SG-MONOS

Flash macro, 0.6 V 84 Mb SRAM in 14 nm FinFET, and 14 nm 1.1 Mb Embedded DRAM macro.

The first paper, by Sako *et al.*, presents a low-power 64 Gb MLC NAND flash memory capable of 30 MB/s program throughput and 533 MB/s data transfer rate at a 1.8 V supply voltage. The memory is fabricated in 15 nm CMOS technology and occupies 75 mm^2. Power dissipation is reduced by 36% by lowering VCC down to 1.8 V and implementing smart pumping power control. New low current peak features reduce a multidie concurrent programming peak by 65% for the four-die case, and an erase verifying peak by 40%, respectively. High performance of 30 MB/s is achieved with newly added nanoscale transistors that reduce bit-line discharge time by 70%.

The second paper, by Jeong *et al.*, describes a 128 Gb 3b/cell vertical-NAND flash memory that incorporates 1 Gb/s I/O. It is implemented with a 3-D stacking technology and uses 32 stack wordline (WL) layers. The actual die size is 68.9 mm^2, which is the smallest ever reported, and the programming time is 700 μs.

The third paper, by Taito *et al.*, details a 28 nm embedded split-gate MONOS Flash macro for automotive applications implemented in 28 nm process. RAM frequency is increased by 15% by the use of a temperature-adjusted overdrive WL voltage control scheme. High write throughput of 2.0 MB/s is demonstrated by source-side injection (SSI) programming with negative back bias achieving 63% reduction of program pulse time.

The fourth paper, by Karl *et al.*, describes a 0.6–1.1 V, 84 Mb pipelined SRAM array design implemented in 14 nm FinFET CMOS technology. Two array architectures featuring a high density of 0.05 $\mu\mathrm{m}^2$ 6T SRAM bitcell and a 0.0588 $\mu\mathrm{m}^2$ 6T SRAM bitcell targeting low-voltage operation are detailed. The high-density array design reaches 2.7 GHz at 1.1 V with 14.5 $\mathrm{Mb/mm}^2$ bit density, while the low-voltage optimized array can operate at 0.6 V, 1.5 GHz under typical process conditions. Technology and assist co-optimization enable a 50 mV reduction in VMIN and a 1.81 $\times$ increase in density over a 22 nm design.

The final paper, by Fredeman *et al.*, presents a 1.1 Mb embedded DRAM macro for next-generation IBM SOI processors, which employs 14 nm FinFET logic technology with 0.0174 $\mu\mathrm{m}^2$ deep-trench capacitor cell. The 1.1 Mb macro is organized with a center interface block architecture, allowing 1 ns access latency and 1 ns bank interleaving operation using two banks, each having 2 ns random access cycle. 5 GHz operation has been demonstrated in a system prototype, which includes six instances of 1.1 Mb eDRAM macros, integrated with an array-built-in-self-test engine, phase-locked loop (PLL), and WL high and WL low voltage generators.

VI. Technology Directions

From the TDs' sessions at ISSCC 2015, we have selected eight papers for this special issue. The first group of papers focuses on data acquisition from various sensing systems. In the second group of TD papers, steps toward data reduction and classification are taken, whereas the last paper focuses on the body as a communication channel.

The first paper, by Harpe *et al.*, describes a compact ($0.2\,\mathrm{mm}^2$) signal acquisition system for implantable devices or unobtrusive IoT sensors, with only 3 nW power consumption. The ADC only consumes 1.5 fJ/conversion step. At this rate, 10 years of continuous in-body operation can be guaranteed with a thin-film battery of only $1\,\mathrm{mm}^3$.

The second paper, by Delorme *et al.*, focuses on the analysis of molecules in complex gas phases at subattogram resolution. This attogram gravimetric sensing resolution is obtained by an NEMS-array control IC, fabricated in a 28 nm CMOS process. This CMOS circuit addresses the sequential and parallel driving and readout of NEMS arrays with resonances in the range of 10 MHz–1 GHz. It integrates an ADC, two DACs and four-tone DSP (lock-in amplifier and direct digital synthesizer) for increased throughput. Its area is $0.9\,\mathrm{mm}^2$ and it draws a power of 68 mW.

The third paper, by Tzeng *et al.*, also describes a portable gas chromatography system. This system has been built for noninvasive lung cancer diagnosis and can obtain a sensitivity of 15 ppb. Experimental results show that the system is able to detect seven types of lung cancer associated VOCs (acetone, 2-butanone, benzene, heptane, toluene, m-xylene, and 1,3,5-trimethylbenzene).

The fourth paper, by Mahsereci *et al.*, shows a flexible stress sensor integrated in ultra-thin ($20\,\mu\mathrm{m}$) flexible silicon. The operation of this sensor has been demonstrated in an adaptive robotic gripper. The stress influence in the readout and digital circuits is minimized up to 350 MPa by using stress insensitive components, design measures, and layout techniques.

The fifth paper, by Rieutort-Louis *et al.*, describes a large-area image sensing and detection system. The system is implemented in amorphous silicon and comprises embedded thin-film weak classifiers. These weak classifiers enable the reduction of the number of interconnects from the large-area system to the readout electronics. The overall system employs error-adaptive classifier boosting to deal in an efficient way with the weak classifiers embedded in the large-area imaging system.

The sixth paper, by Badami *et al.*, demonstrates a 6 μW power-proportional acoustic sensing front-end for voice activity detection. By implementing hierarchical and scalable sensing combined with adaptive and context aware information extraction, the authors realized $10\times$ power saving in the classification system.

The seventh paper, by Yamaoka *et al.*, presents a power-efficient 20 k-spin Ising chip for combinational optimization. Problems that can be mapped to the Ising model can be solved quickly using the dedicated IC due to the implementation of CMOS annealing. The power efficiency of the chip is 1800 times higher than that of the conventional Von-Neumann computers.

The final paper, by Cho *et al.*, describes two different flavors of transceivers for body channel communication implemented in the same IC. The applications of the IC are both in the healthcare and in the entertainment domain. The entertainment

transceiver achieves 79 pJ/b 80 Mb/s full-duplex transfers and the healthcare transceiver exhibits a Q-factor over 1000 and a power consumption of only $42.5\ \mu$W.

EDITH BEIGNÉ, *editor*
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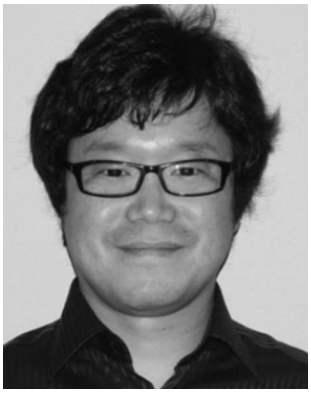
JAN GENOE, *editor*
IMEC
Leuven, Belgium

Edith Beigné received the M.S. degree in electronics engineering from Grenoble Polytechnical Institute, Grenoble, France, in 1998, and the French HDR (Research Director) degree in electronics engineering in 2014.

She joined CEA-LETI, Grenoble, France, in 1998. In 2002, she developed an asynchronous NoC dedicated to Globally Asynchronous and Locally Synchronous complex digital circuits. Since 2009, she is a Senior Scientist with the Digital and Mixed-Signal Design Laboratory. She was leading complex test-chip design dedicated to low power and variability management, exploiting asynchronous design, and advanced technology nodes like FDSOI 28 and 14 nm for many different applications from high-performance MPSoC to ultra-low power IoT devices. She has authored and coauthored more than 100 papers in international journals and presentations at international conferences, and holds several patents in the field of low power and adaptive digital and mixed-signal circuits. Her research interests include asynchronous mixed-signal circuits and systems for wireless applications.

Ms. Beigné has been served with the ISSCC Technical Program Committee since 2014 and the VLSI Symposium Committee since 2015.



Jinuk Luke Shin received the M.S. degree in electrical engineering from the University of Texas at Austin, Austin, TX, USA.

He has been with Oracle (formerly Sun Microsystems), Santa Clara, CA, USA, since 2000. He is currently a Director of Hardware Development, responsible for circuit and physical design of next-generation SPARC processors. He has led design activities in technology, power distribution/management, clocking, memories, analog components, Si validation, and chip integration for 9 SPARC processors. Prior to joining Oracle, he was with Hitachi Semiconductor America, San Jose, CA, USA, from 1997 to 2000, where he developed the level-1 cache arrays for a SuperH processor. From 1995 to 1997, he was with Motorola, Austin, TX, USA, where he was involved in the design of embedded flash memories for digital signal processors. He is an author of 37 technical papers and holds 13 issued and pending U.S. patents. His research interests include energy-efficient circuit and physical design techniques and methodologies for high-end microprocessors.

Mr. Shin is currently serving on the digital architecture and system subcommittee of ISSCC.

Yusuke Oike received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2000, 2002, and 2005, respectively.

In 2005, he joined Sony Corporation, Tokyo, Japan, where he has been engaged in research and development of architectures, circuits, and devices for CMOS image sensors. From 2010 to 2011, he was a Visiting Scholar at Stanford University, Stanford, CA, USA. Since 2011, he has returned to Sony and has been in-charge of development of CMOS image sensors as a Senior Manager. His research interests include pixel architecture and mixed-signal circuit design for image sensors and image processing algorithms.

Dr. Oike has served on the technical program committee of the IEEE ISSCC since 2011.

Chulwoo Kim received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2001.

In 1999, he worked as a Summer Intern of the Design Technology with Intel Corporation, Santa Clara, CA, USA. In May 2001, he joined IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. Since September 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor at the University of California at Los Angeles, Los Angeles, CA, USA, in 2008 and at the University of California at Santa Cruz, Santa Cruz, CA, USA, in 2012. He is a coauthor of two books: *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 4th ed., 2014) and *High-Bandwidth Memory Interface* (Springer, 2013). His research interests include wireline transceivers, memory, power management, and data converters.

Dr. Kim served as a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS and has been elected as Distinguished Lecturer of the IEEE Solid-State Circuits Society for 2015–2016. He is currently on the Editorial Board of IEEE TRANSACTIONS ON VLSI SYSTEMS and on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He was the recipient of Samsung HumanTech Thesis Contest Bronze Award (1996), the ISLPED Low-Power Design Contest Award (2001, 2014), the DAC Student Design Contest Award (2002), SRC Inventor Recognition Awards (2002), the Young Scientist Award from the Ministry of Science and Technology of Korea (2003), the Seoktop Award for excellence in teaching (2006, 2011) and ASP-DAC Best Design Award (2008) and Special Feature Award (2014), Korea Semiconductor Design Contest: Ministry of Trade, Industry and Energy Award (2013).

Jan Genoe received the M.S. and Ph.D. degrees in electrical engineering from the KULeuven, Leuven, Belgium, in 1988 and 1994, respectively.

Afterward, he joined the High Magnetic Field Laboratory, Grenoble, France, as a Human Capital and Mobility Fellow of the European Community. In 1997, he became a Lecturer with the KHLim, Diepenbeek, Belgium. Currently, he is a Professor with the KULeuven and Chief Scientist with the LAE Department, IMEC, Leuven, Belgium. He is the author and coauthor of more than 100 papers in refereed journals. His research interests include devices, design of analog circuits, design of digital circuits, organic photovoltaics, piezoelectric devices, VLSI design, and designs made using organic and oxide transistors. A crucial aspect when designing using emerging technologies is the careful assessment of parameter variations in the device characteristics. This technology insight, combined with creative design variations, has enabled to increase the level of complexity that can be obtained using designs in organic and oxide technology. Examples of design modifications to accommodate technology are the usage of the back-gate to adapt the threshold voltages and the alternative modulation scheme to obtain bidirectional communication in thin-film RFID tags. This work has resulted in seven subsequent ISSCC presentations in the technology directions session (128 bit organic RFID tags, organic microprocessor, hybrid oxide-organic RFID tags, etc.).

Dr. Genoe is a Reviewer for a broad range of journals including *Electrochemical and Solid-State Letters*, *Electron Device Letters*, *Thin Solid Films*, *Journal of Applied Physics*, *Semiconductor Science and Technology*, *Electronic Letters*, and *Organic Electronics*, and a member of the Technology Directions International Program Committee of the ISSCC.