Successfully Designing FPGA-Card for Mobile Robot Research

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ABSTRACT
This paper describes a new design of electronic board based on FPGA Cyclone III. The main objective of this idea is towards small size, fast Real Time processing, high integration and analog peripherals that are not disposal in available FPGA development kits. For the optimum performance a Microcontroller 8 Bits Flash CMS was used which is interfaced with FPGA and used as an ADC to make all the data processing on board in Real Time. This card can be used in many applications on the field of mobile robotics like autonomous navigation and intelligent parallel parking. To communicate and supervise all activities of mobile robots, an RF module was installed on the board which serves as a transmitter to a host computer that will receive all information in Real Time. The paper introduces many challenging issues which are being addressed to enhance in laboratories researchers project planning, designing and implementing capabilities. These issues are the FPGA performance, interfacing the microcontroller to the FPGA, implementing the flexible processing algorithms and high speed interconnection between the boards. The developed card was tested via the implementation of real time algorithms, and was validated experimentally on a mobile robot system.

Keywords
FPGA, Microcontroller, Mobile robot, Robotics applications.

1. INTRODUCTION
Designs of autonomous car-like robots have received a lot of increased attention of many research groups in many laboratories. Creating autonomous robots is one of the main up-to-date research activities. The parameters of the mechanical and electronic components should be optimized to perform multiple tasks.

In recent years, the scientific community and educational institutions have shown particular interest in the use of research involving autonomous mobile robots in order to stimulate researchers' interest in designing and investigation in different areas of engineering and to promote the development of new technologies. Mobile robots must be capable of accurately controlling their desired position and route.

Field Programmable Gate Arrays (FPGAs) have begun to appear as accelerators for general computation. Their potential for massive parallelism, high on chip memory bandwidth and customizable interconnection networks all contribute to demonstrate 100-1000 increases in application performance relative to current PCs. FPGA coprocessors have been available in niche markets for years, and are now appearing in mainstream supercomputers from vendors including Gray and Silicon Graphics. Available development tools do not address developers of computing application; however, traditional FPGA design tools meet the gate-level needs of logic designers, but present a computing model that vanishingly few software developers can use. Likewise, logic designers understand logic structures for high computing performance, but rarely know the intelligent autonomous systems like industrial mobile robot, intelligent vehicle or other applications that need acceleration.

Researchers in many fields have a seemingly insatiable need for high speed computation. FPGAs offer a promising approach to acceleration of a wide range of computing application, and allow the developer to create computing structures customized to the application at hand. The most popular hardware design languages (HDLs), VHDL and Verilog, still address the bit-level needs of the logic designer, at a semantic level below the barest layer of assembly programming. The fundamental hypothesis of this work is that the new designed FPGA card was developed to expand beyond the narrow domain of intelligent robots, and into board areas of computationally intensive applications. Although many application areas could benefit from this new FPGA card, this research focuses on industrial applications and intelligent systems.

Various engineering papers addressed effective design and implementation methods of FPGA based systems and signal processing card. Wei et al. [1] developed a tensor-based optical flow algorithm using FPGA technology. The new design of this algorithm can calculate optical flow at a speed of 19661 Kpps which is equivalent to 64 640x480 frames per second. The algorithm was tested on both synthetic and real image sequences.

In paper [2] studies investigated the advantages of FPGA over general purpose microcontrollers like very high data rate, flexibility, data security, parallel processing which are necessary for real time application. The paper represents a number of basic issues with implementing algorithms on FPGA platforms.

Autonomous mobile robot navigation considers the execution of three stages: (a) mapping, (b) localization, and (c) decision making. The first stage uses information from sensors for

creating a map of the environment. The second one relates the map with the sensor information, allowing the robot to self-localization in the environment. The third stage considers the path planning problems [3].

Different kinds of sensors that can be used for providing environment information to the mobile robot. Such sensors are classified in two mains groups: (a) interoceptive and (b) exteroceptive. The interoceptive sensors perform internal robot parameters measurements without environment dependence. Encoders, gyroscopes, and accelerometers are some examples of interoceptive sensors. On the other hand, exteroceptive sensors perform external measurements, for instance, ultrasound, radar and infrared positioning systems as well as cameras, GPS and magnetometers. In humans, the vision sense is the one which provides more quantity of information about the environment. Through the sensorial fusion (provided by the stereo vision system). Surrounding objects localization will be efficiently estimated.

The use of cameras jointly with image processing algorithms for implementing sensors (e.g., distance, movement, color, and presence sensors) is a suitable solution for mobile robotic applications. Additionally, cameras with embedded image processing issues are the foundations of computer vision area. Catadioptric systems are realizations of omnidirectional vision, being mainly based on specially shaped mirrors (e.g., spherical, hyperbolic, parabolic, etc) that reflect the environment to the camera from all directions, obtaining a panoramic view. Thus, these systems can provide information from a larger area than other vision sensors [4].

Common robotic platforms are based on desktop solutions executing complex algorithms for robot applications. However, desktop platforms are not tailored for embedded applications with probability and low power consumption requirements. FPGAs are a suitable solution for implementing intelligent algorithms with a high performance. FPGAs allow the involved algorithms to be mapped directly in hardware in a parallel way. In addition, FPGAs allow software RISC processors to be implemented in order to execute parts of the algorithms with low performance requirements.

FPGAs have long, successful history in digital signal processing (DSP) applications. Vendors have created FPGA design tools specifically for DSP applications. Scientists predict that robots will play an important role in the future. In this scenario, robots will be able to assist humans in many tasks. This work interest the robotic field which is one of the major challenges is providing robots with sensorial and rational capabilities, allowing them to assist, and possibly substitute, humans in some activities requiring special skills. The main purpose of this work is to show the advantages of using FPGAs to implement Robotics Platforms. Some of these advantages are parallelism, flexibility and scalability. Finally some experiments were performed to reveal these advantages.

Background: The use of an electronic card is a common solution for mobile robotics applications. Different works are related to the choice of the adapted system based on a specific processor depending on the complexity of the robotics application. Stansfield and Page proposed new FPGA architecture. This architecture includes a number of novel features not found in available FPGAs in 1995. The work described the development of the FPGA and looked at the mapping onto it of some interesting application circuit elements. The design was discussed in approximately chronological order which allows explaining other options considered and rejected during the development process [5].

In paper [6], Hanchek and Dutt proposed techniques utilizing the principle of node covering to tolerate logic or cell faults in SRAM-based FPGAs. They developed a routing discipline that allows each cell to cover-to be able to replace-its neighbour in a row. They proposed also techniques for tolerating wiring faults by means of replacement with spare options. Detection in the FPGAs is accomplished by separate testing; either at the factory or by the user. If reconfiguration around faulty cells and wiring is performed at the factory (with laser-burned fuses, for example), it is completely transparent to the user. In other words, user configuration data loaded into the SRAM remains the same, independent of whether the chip is detect-free or whether it has been reconfigured around defective cells or wiring-a major advantage for hardware vendors who design and sell FPGA-based logic (e.g., glue logic in microcontrollers, video cards, DSP cards) in production-scale quantities. Compared to other techniques for fault tolerance in FPGAs, methods proposed in paper [6] are shown to provide significantly greater yield improvement, and a 35 percent non-FT chip yield for a 16×16 FPGA is more than doubled.

A prototype version of the Front End Driver based upon the popular commercial PCI bus Mezzanine Card (PMC) form factor was proposed and described by Baird et al. The FED-PMC consists of an 8 channels, 9 bit ADC, card, providing a 1 MByte data buffer and operating at the LHC design frequency of 40 MHz. The core of the card is a re-programmable FPGA which allows the functionality of the card to be conveniently modified. The card is supplied with a comprehensive library of C routines. The PMC form factor allows the card to be plugged onto a wide variety of processor carrier boards and even directly into PCI based PCs. The flexibility of the FPGA based design permits the card to be used in a variety of ADC based applications [7].

Geralis et al. developed a global trigger processor emulator system (GTPe) for the CMS experiment data acquisition system (DAQ). The GTPe generates Level-1 triggers and exchanges information with other DAQ components. The GTPe is an FPGA-based PCI card operating in a host Linux PC. The board is programmed to function as a trigger data source, capable of generating multiple independent triggers and their associated data streams. Data are transmitted over the CMS-specific S-LINK64 protocol. The purpose of the GTPe is to decouple the Level-1 trigger system from the readout system. This is an important component of the installation, testing, and maintenance of the CMS DAQ [8].

A color card printer robot was developed by Liu.S-M [9]. The color card printer robot utilizes dye-sublimation/resin thermal transfer printing technology to achieve its direct-to-card photo-quality output. The design includes the printer robot mechanisms, control circuits system, control firmware, communication interface, and color image processing algorithms. The developed card is a standard CR-80 PVC card with a size of 54 mm × 86 mm and the printing resolution is 300 dpi. The control circuits system is based on a digital signal processor (DSP) and a FPGA, which is a programmable logic device to contain embedded arrays, offering up to 100,000 gates. The digital logic modules implemented in FPGA include DRAM access module, data and I/O control module, communication control unit, LCD display module, keypad, sensors module, thermal printing head (TPH) control module, and motors control module.

Hidvégi et al. proposed a high speed acquisition system for segmented Ge-detectors. This project introduces many challenging issues: signal integrity, ADC performance,

interfacing ADCs to the FPGA, synchronisation of ADCs across the entire system, implementing flexible processing algorithms, high speed interconnection between boards and managing the significant heat generation [10].

Recently, there has been growing interest FPGA-based system (FBS) architecture. Eugenio and Estrada have developed a Hardware/Software FPGA Robotics Architecture for applications on Mobile Robotics. A test mobile robot was built and it is based in a commercial programmable robot called Create from iRobot, also the test platform has additional components like sonar, infrared sensors and a robotic arm, these components are used to increase the robot's functionality and to show that it is feasible to build any kind of hybrid robot. The Hardware/Software Architecture is a complete Embedded System (ES). Hardware side includes a processor, buses, memory and peripherals like co-processors, sensors, robotic arm, controllers, UARTs, etc., Software side includes a Linux OS with a set of libraries that performs different functionalities and to control all components in FPGA, these functions are easy-understanding for robotic programmers [11].

Wilton proposed how to supplement the experimental methodology with a set of analytical expressions that relate architectural parameters to the area, speed, and power dissipation of an FPGA. Optimizing these analytical expressions is done using techniques such as geometric programming [12].

Zhe et al. proposed a design method of infrared image display card using FPGA and ADV7123. Its main function includes pixel gray level conversion, image zoom in and PAL standard video signal generation. The design ideals, hardware architecture, FPGA logical modules, FPGA configuration, interconnection between display card and master board, and the PAL standard video signal generation method using ADV7123 was discussed in detail. The display card is mainly applied to the hardware debugging of infrared image system and effect observation of the infrared image processing algorithm. The actual using shows that the card can well meet the display requirement of the infrared image processing system [13].

Gupta and Kumar designed a real time digital signal processing system for the mean to interface a 16-bit 1-MSPS CMOS ADC to FPGA based signal processing. As a result, the platform decode process of various kinds of digital and analog signals simultaneously for the optimum performance a 16-bit 1 MSPS ADC was interfaced with FPGA to make all the data processing on board in real time [14].

An FPGA based DAQ card using PCI express protocol was proposed by Khan et al., this DAQ card presents a cheaper solution to industrial problems of process monitoring, controlling, and fastest data logging [15].

Paper [16] presented by Carrio et al. describes the design of an optical link card developed in the frame of the R\&D activities for the phase 2 upgrade of the TileCal experiment. This board, that is part of the evaluation of different technologies for the final choice in the next years, is designed as a mezzanine that can work independently or be plugged in the optical multiplexer board of the TileCal backend electronics. It includes two SNAP 12 optical connectors able to transmit and receive up to 75 Gb/s and one SFP optical connector for lower speeds and compatibility with existing hardware as the read out driver. All processing is done in a Stratix II GX FPGA. The hardware design, included signal and power integrity analysis, needed when working with these high data rates and on firmware development to obtain the best performance of the FPGA signal transceivers and for the use of the GBT protocol.

In another study Alba-Flores et al. suggested a project-based learning approach in teaching and undergraduate level course for engineering technology students. The course is for senior students majoring in electrical or mechanical engineering technology. Topics discussed as part of the course include PID controllers, fuzzy logic control principles, robot mechanics, sensors for mobile robots, FPGA embedded systems implementation, and robot path planning techniques. The main goal of this course is to apply the above topics to the design and implementation of an autonomous navigation robot [17].

Research Objectives: The rapidly increase of personal robotic platforms and their applications represents a great challenge for researches at universities. Electric drives and motion control systems represent an engineering discipline that has rapidly developed over the last few decades.

The main objective of this work was to propose a generic electronic platform for a robotic mobile system [18], seeking to obtain a support tool for under-graduation and graduation activities. Another objective was to gather knowledge in the mobile robotic area, aiming at presenting practical solutions for industrial problems [19].

The proposed new FBS would serve as material needs of more robotic applications. The developed FBS is an integrated system for intelligent software middleware to coordinate many activities in the field of electric drives, robotics, autonomous systems and artificial intelligence. As a result of this study, this paper contributed researches to the industrial development, principally in the fields of industrial robotics and also in different application purposes such as entertainment, personal use, welfare, education, rehabilitation, etc.

The present work intends to implement applications on the newly designed FBS, which is able to solve precisely manoeuvring operations in complex situations [20-21]. The remainder of this paper is organized as follows. After reviewing the literature, section 2 outlines some computational techniques related to the Altium Designer environment. Section 3 presents the development strategy. Section 4 describes the FPGA-based system. Section 5 discusses the signal processing system, and before concluding, section 6 presents synthesis, validation results, and a performance analysis.

2. ALTIUM DESIGNER RELATED TECHNIQUES

Before starting the development of the FBS project, all steps in Altium Designer tool must be created which are [22]:

- The basis of every electronic product design is the project

- The project links the elements of the design together, including the source schematics, the PCB, the netlist, and any libraries or models that kept in the project.

- The project also stores the project level options, such as the error checking settings, the multi-sheet connectivity mode, and the multi-channel annotation scheme.

- There are six project types- PCB projects, FPGA projects, core projects, embedded projects, script projects and

library packages (the source for an integrated library).

- Altium Designer allows accessing all documents related to the project via the projects panel.

- Related projects can also be linked under a common workspace, giving easy access to all files related to a particular product.

- When documents are added to a project, such as schematic sheet, a link to each document is entered into the project file. The documents can be stored anywhere on the network; they do not need to be in the same folder as the project file. If they do exist in a directory out side where the project exists or its sub-directories, then a small arrow symbol appears on the document's icon in the projects panel.

After studying the various details of the Altium Designer environment, a strategy of the FBS project must be designed; these steps were detailed in section 3.

3. DEVELOPMENT STRATEGY

Increases in FPGA capabilities, combined with growing system complexity, have created many FBS design challenges. One key challenge is choosing the right FPGA for the design needs, and maximizing the use of FPGA resources. Altium Designer offers recommendations for power supply connections, pin selections and assignments, and other tips and methodologies to help customers design high-quality FBS.

The main concept of the new designed FBS is that by using a 18F4550 microcontroller us an A/D converter. This component includes 13 channel analog to digital converter (A/D) module with 10-bit resolution, 35 pins which can be programmed us I/O. The microcontroller 18F4550 is ideal for low power (nanoWatt) and connectivity applications that benefit from the availability of three serial ports: FS-USB (12Mb/s), I²C™ and SPI™ (up to 10 Mbit/s) and an asynchronous (LIN capable) serial port (EUSART). Large amounts of RAM memory for buffering and Enhanced Flash program memory make it ideal for embedded control and monitoring applications that require periodic connection with a (legacy free) personal computer via USB for data upload/download and/or firmware updates. Resulting, all analogue inputs information from sensors can be converted to numerical ones which are then processed by the FPGA unit. In this FPGA, volatile memory devices can also be programmed via an AS mode normally during development work via an USB Blaster. In addition, newer parts, for example cyclone III, have internal capability accessible via the RS232 port and the RX and TX mode to install the RF module on the FBS.

4. THE NEW DESIGN OF THE FPGA-BASED SYSTEM

4.1 Designing the FPGA-Based System

The problems inherent in FBS designs are related principally to three categories. The functionality whose issues causes the design not to work correctly, electrical issues that cause the board not to work, and marginal issues that allows the board to work most of the time but cannot be guaranteed to work all the time.

4.2 Power Supplies

The FBS needs a high number of power supplies. In this project all the newly designed board will require the power supplies shown in figure 1.

A power budget was created for each power supply voltage system. The objective of this operation is to ensure that the power supplies can adequately supply the current required by the FPGA Cyclone III family and all the interfaces on the board. Moreover, decoupling capacitors were added for each of these different power supplies after determining them by electrical simulations.

4.3 Connecting the Peripherals

a- The Serial Digital Interface, is a protocol for transmission or distribution of the various digital formats. This interface presents the advantage of using serial configuration devices, cheaper and use of the minimum of pins. The AS-mode connector is connected to the FPGA through the Flash memory.

Table 1. Identification of the connection FPGA-AS_mode

PIN FPGA	PIN AS-mode
DCLK	1
GND	2,10
CONFIG_DONE	3
VCC=3.3V	4
nconfig	5
nCE	6
DATA0	7
nCS0	8
ASD0	9

b- The Joint Test Action Group (JTAG) is the name of the standard IEEE 1149.1 untitled Standard Test Access Port and Boundary-Scan Architecture. It is designed to facilitate and automate the testing of digital electronic cards. It gives access to auxiliary pins input-output digital components which present high integrated density. The JTAG connector is connected directly to the FPGA (10pins) with corresponding pins of the FPGA.

Table 2. Identification of the connection FPGA-JTAG

PIN FPGA	PIN JTAG
TCK	1
GND	2,10
TDO	3
VCCA=3.3V	4
TMS	5
NC	6,7,8
TDI	9

c- The Universal Serial Bus (USB) is a lot faster than the serial port input-output interface. The resources of the microcontroller 18F4550 were exploited to make a USB port to ensure the connection between the card and the computer

for programming the microcontroller which is used in this case as an ADC component.

d- RS232 could be suitable for this design, and was connected and implanted for many uses such as transferring data to a computer.

4.4 Development and Interfacing of FPGA with all the Constituent Modules

The first step to evaluate analog inputs acquired from sensors and digital outputs could also be suitable for this design. Analog inputs are connected directly to the microcontroller, and the digital outputs are defined after processing sensors data by the FPGA.

The second step regards the development of the prototype board based on an FPGA cyclone III EP3C 40Q240C8 to interface with the microcontroller, Bus switch IDTQ S3861QG8, SRAM memory 71V 416 L10 PHG, RF module XBee1, EPCS memory configuration and the Max 232. After the proper interfacing, all peripherals are tested and their responses are adjusted accordingly. Therefore the outputs are an adaptive hardware that continuously change in response to the input analog data from sensors. The trends of this new design of this FPGA board are towards optimized size, high integration and fast real processing.

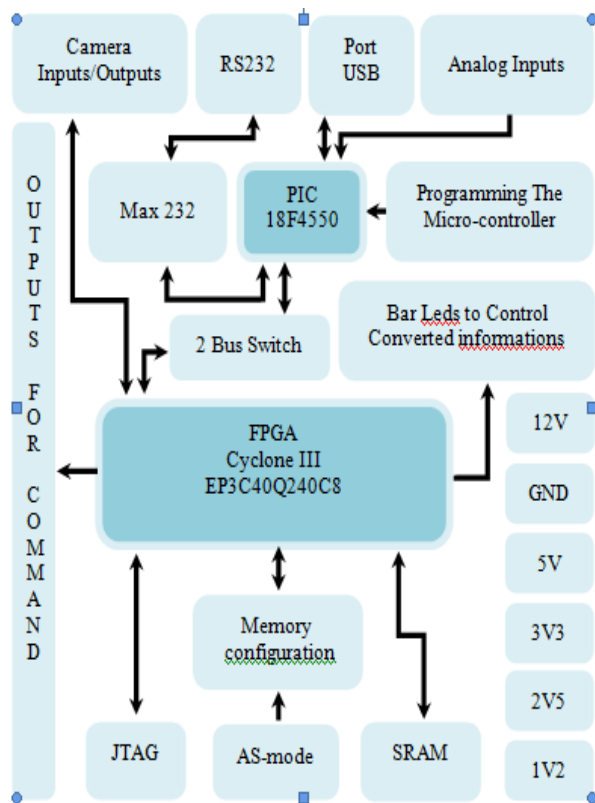Figure 1 show the general block diagram of the new designed FBS.

Figure 1: Block diagram of the new designed FPGA-based system

5. THE SIGNAL PROCESSING SYSTEM

The new designed FBS card is adapted respectively for both types of signals, analog as well as digital. Real time signal processing design was verified. This new card simplifies the overall design process for many applications in the field of

robotic. Microcontroller outputs are stored in the SRAM. All information are processed with FPGA.

6. VALIDATION AND DISCUSSION

All components shown in figure 1 were routed straight through the shortest path available by using Altium Designer. Figure 2 shows the PCB outline for the new FBS.
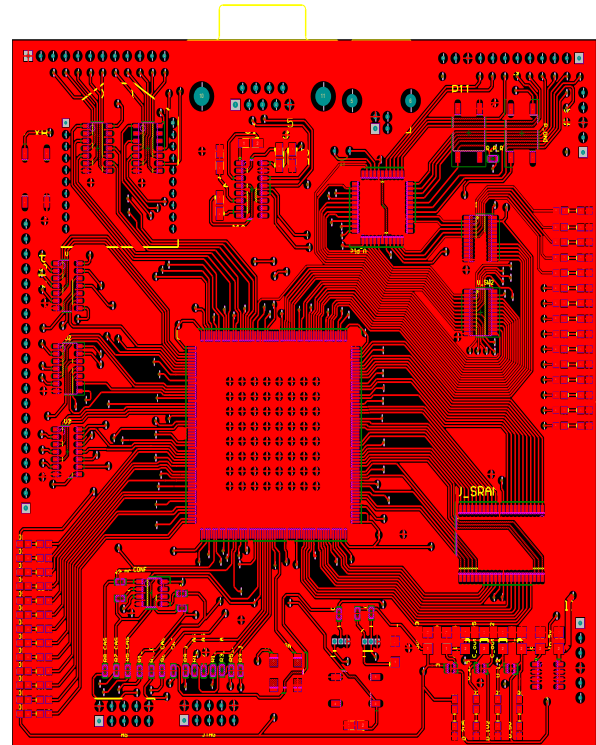

Figure 2: PCB Outline

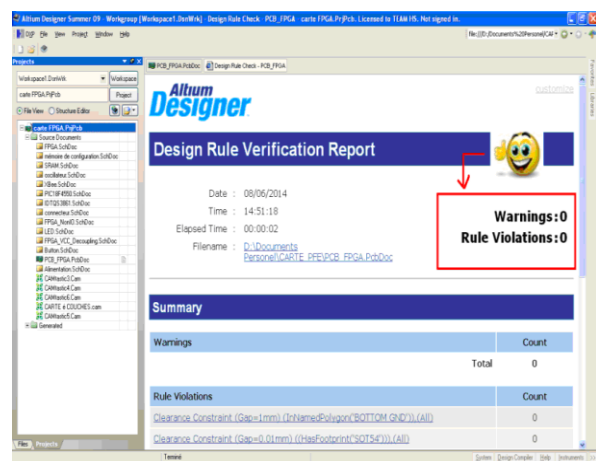Figure 3 presents the simulation result of the FBS.

Figure 3: Simulation result

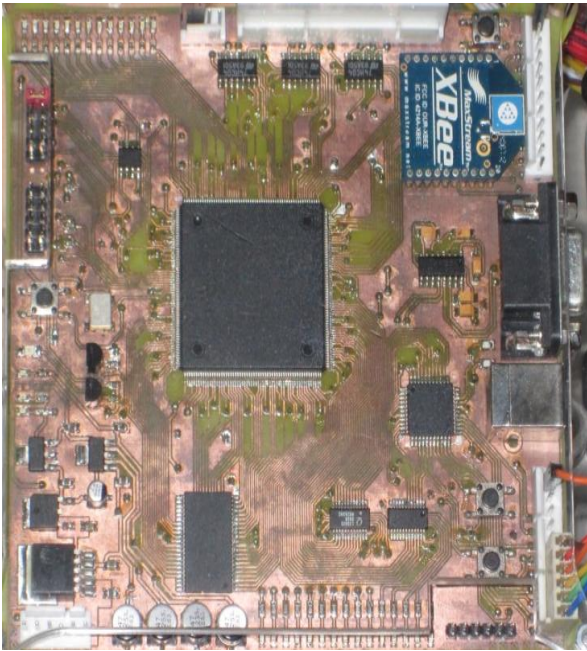Figure 4 presents the photo of the developed card.

Figure 4: Photo of the developed card

To demonstrate and validate effectiveness of the developed card, an intelligent parallel parking algorithm, presented in [18] was tested and implemented on the FBS which was applied to a newly prototype of mobile robot type-vehicle.

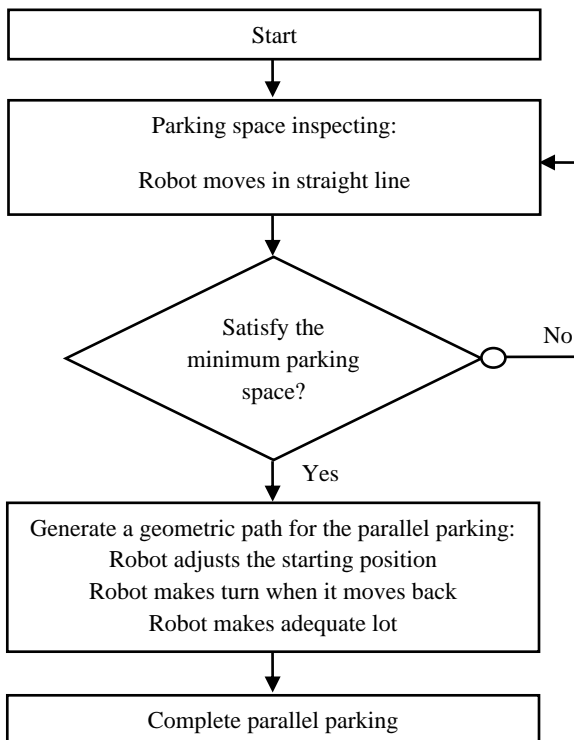Figure 5 illustrates the developed real time algorithm for the parallel parking process diagram.

Figure 5: The parallel parking process diagram

Figure 6 presents a general view of the architecture of the designed mobile robot.
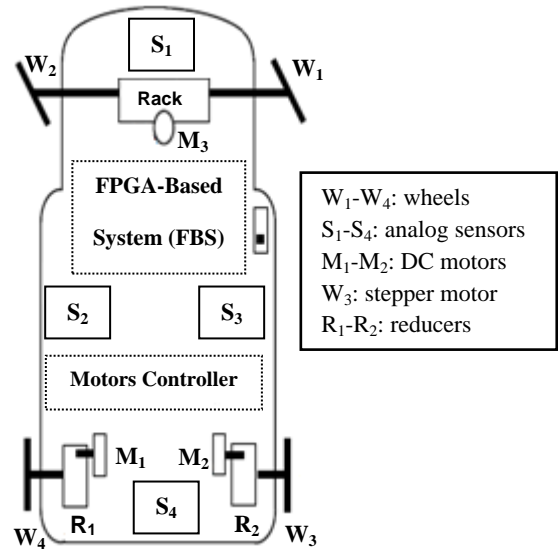

Figure 6: Architecture of the designed mobile robot

The following images are obtained from the experiment results and illustrate the whole procedure of autonomous parallel parking manoeuvres.
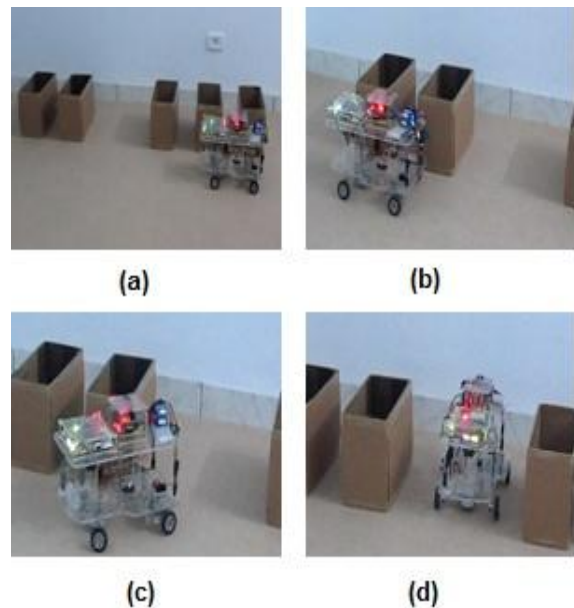

Figure 7: Experiment results. (a) Robot moves in straight line, (b) Robot adjusts the starting position, (c) Robot makes turn when it goes back, and (d) Robot takes adequate lot of parking.

These experimental results proved that the FBS was robust to decode signals from analog sensors, implement fast Real Time processing algorithms and control the movement of the mobile robot.

7. CONCLUSION

Contents High computational demand makes it difficult to use intelligent algorithms for real-time applications using general purpose processors. In this paper, a new hardware design for an F.P.G.A Cyclone III card has been developed specifically for applications in the field of mobile robot. Before hardware

implementation, the expected design performance in terms of accuracy and resource utilization was carefully evaluated. These issues range from understanding both the sampling rates and computational rates of different mobile robot applications with the aim of understanding how these requirements affect the final FPGA implementation. In another ways, this paper leads to conclude the advantages of the new design of an FPGA Cyclone III board over general purpose microcontrollers like very high data rate, flexibility, data security, parallel processing which are necessary for real time applications. FPGA based platform is addressing the problems by allowing add-on cards to meet application-specific feature and performance requirements. Many algorithms were tested on both synthesis and real sequences. The proposed design works well on synthesizes sequences and satisfactory on the real sequence. Some revisions are proposed to improve the system design which requires more hardware resources, which is the goal of a next research.

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