International Journal of Signal Processing, Image Processing and Pattern Recognition
Vol.9, No.6 (2016), pp.115-120
http://dx.doi.org/10.14257/ijsip.2016.9.6.10

Application of FPGAs in EEG Analysis

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Abstract

In this paper, a technique for processing data produced from an EEG though the use of an FPGA architecture is proposed. The proposed FPGA architecture should efficiently determine the wavelet transform of the inputted data. The transformed signal would then be used for diagnosis and monitoring of patients. The application of the wavelet transformed signal for the diagnosis of an epileptic patient is also proposed.

Keywords*: EEG (electroencephalogram) Analysis using FPGA(Field Programmable Gate Arrays); CWT (Continuous Wavelet Transforms); WT (Wavelet Transform) using FPGA DWT (Discrete Wavelet Transforms);FFT(Fast Fourier Transform); Automated EEG Analysis; Heat Stress on EEG*

1. Introduction

Brain cells communicate via electrical impulses. The EEG (electroencephalogram) is a test that detects electrical activity in the brain using small, flat metal discs (electrodes) attached to your scalp [1].The potential difference between the two electrodes over time is what is seen on the EEG diagram. Multiple electrodes could be placed on different parts of the brain and so multiple potential differences for different locations of the brain could be recorded over time. The resultant wave forms –seen by the EEG are categorized in terms of the frequency band they occupy. Waves are categorized as Delta if their frequencies lie in the 0.5-4 Hz range, Theta if their frequencies lie in the 4-8 Hz range, Alpha if their frequencies lie in the 8-13 Hz range, Beta if their frequencies lie in the 14-30 Hz range and Gamma if their frequencies lie in the range that is greater than 30 Hz. The analysis of the EEG aids in the monitoring of epilepsy, tumors, sleep disorders etc. Analysis of the EEG could also lead to the diagnosis of brain diseases such as Alzheimer's disease [2].

In order to extract features from EEG signals, the wavelet transform (WT) has been widely applied which results in the representation of the wavelet coefficients in the time-frequency plane. By performing this operation on the EEG signals, the doctor would be able to better analyze the EEG signals. This process, when done in software, requires a great deal of computational resources and so it is not practical to implement such a method for real time analysis of the EEG signals. As a result by placing such an operation in the hardware domain with the use of FPGAs, it would ease the processing power required for a system that is required to analyse EEG signals through the use of the WT transform [3].

This research paper investigates the operation of the WT and a possible implementation of the wavelet transform though the use of a proposed concept model of the FPGA architecture. From the proposed, architecture, an application into the actual diagnosis of an epileptic using the obtained wavelet transform of the EEG signals will be proposed.

2. Literature Survey

This section surveys the different methods of EEG analysis that currently exists.

An automated seizure detection algorithm (used by the Persyst P12 software) was investigated in [8]. This algorithm will give an alert when a seizure is detected. The color-coded rhythmicity and fast Fourier transformed (FFT) power spectrograms, averaged for each hemisphere, were investigated to determine the presence of patterns suggestive of electrographic seizures. These took between 30 minutes to 1 hour to analyze and were used to evaluate the performance of the automated seizure detection algorithm. The algorithm proved to detect only 76.1% of the seizures and gave several false positives. Further, the method of evaluation of the algorithm may have been flawed since the inspection of the power spectrograms may be subjective. Therefore this proves that there is a need for a more accurate method of EEG analysis. Since there was no evidence of the implementation of the CWT, there were so many false positives detected in the implemented method of EEG analysis.

The epileptogenic zone (EZ) boundary was investigated in [9]. The EZ is determined pre-surgery for removal of problematic sections of the brain so as to treat focal epilepsy. The EZ is determined using intracerebral stereo-electroencephalography (SEEG) electrodes which implies that electrodes are to be physically placed in the brain. The following parameters are required to be determined from the SEEG to determine the EZ:

- specific fast activity (FA),
- transient slow polarizing shift (SPS),
- electrographic trace depression or"flattening" (FLT) of background activity.

A software package developed by VG in LabView was used to aid in the determination of these parameters. The EZ takes several hours to be determined. This may be due to the length of time it takes for EEG analysis. By possible introduction of FPGA architecture to aid in the calculations and correlations made for this application, the speed at which this is done may be accelerated. Therefore, this paper shows that there is a need for faster computation which therefore validates the significance of this research paper.

From [10] the Wavelet Transform of the EEG signals was used to determine the effects of heat stroke on a patient. This paper focused on analysis of the delta, theta, alpha, and beta signals of the brain as they are the most dominant frequency components. Data with regard to the effect of heat on three sleep states was collected and examined. These states are:

- AWAKE,
- rapid eye movement (REM) sleep and
- low wave sleep (SWS)

From the results it was seen that heat exposure significantly decreases the beta frequencies in the AWAKE state.

Chronic heat stress resulted in the power of the delta frequency component to decrease in AWAKE and REM states. Little change in theta and alpha components was noticed when under chronic heat stress. This paper emphasised that the wavelet transform provides a superior resolution of data analysis resulting in more refined data analyses on sleep EEG data compared to traditional Fourier analysis. This paper therefore highlights the importance of the wavelet transform in EEG analysis in addition to an application.

The research done in [3-4] all explored methods of implementing CWT on an FPGA architecture. In [4], the Mallart algorithm was used to transform to determine the one dimensional DWT of the inputted waveform. This involved convolving the original signal with multiple filters. In [3], the Morlet wavelet function along with the Fast Fourier Transform (FFT) was used to determine the CWT. Both methods of implementation were successful in the respective papers. However the approach in [3] was better due to a more comprehensive documentation of the algorithm used. Further, [3] included much less calculations than seen in [4].Therefore, the requirements of the FPGA resources for implementing the algorithm in [3] would be less resulting in a greater probability of finding FPGA devices for which the algorithm in [3] could be tested on compared to the algorithm implemented in [4].

3. Implementation of the wavelet transform

According to [3], the CWT could be calculated via the following formula:

$$C(s,b) \int_{-\infty}^{\infty} X(t).\varphi_{s,b}^{*}(t).dt \tag{1}$$

Where:

- X(t) is the inputted signal
- C(s,b) is the coefficient of the wavelet transform at scale s and time b.
- Ψ* is the complex conjugate of the wavelet basis function

Therefore the output of this function would be a series of wavelet coefficients. This shows that the (1) shows the convolution of the inputted signal of each scale with a daughter wavelet. The scales are used to analyze the signal at different frequencies which are inversely proportional to s. High scales would stretch the wavelet function allowing the determination of changes in low frequency components whilst low scales would compress the wavelet function allowing the determination of high frequency components in the signal.

There are different methods of implementing the CWT. According to [4] the Mallart Algorithm was suggested which involved the convolution between the original signal data and the tap coefficients of the high-pass, low-pass filter banks, and then even sample the series after convolution to obtain a discrete wavelet transform. This has already been successfully implemented. However, for this application, the Morlet wavelet function together with the FFT is suggested as it involves the use of simple multiplications and summations rather than complex convolutions [3]. This involves computing FFT of the product of the signal and the wavelet scales according to the following equation:

$$W_n(s) = \sum_{k=0}^{N-1} \widehat{x_k}\, \hat{\varphi} * (sw_k) e^{iw_k.n\delta t} \tag{2}$$

Where:

- $W_n(s)$ is the CWT coefficient
- k=0…N-1 is the frequency index
- $\hat{x}_k$ is the signal in the frequency domain
- $\hat{\psi}(sw)$ is the Fourier Transform of the Wavelet function
- * is the complex conjugate of the value proceeding it
- n is the time index
- δt is the time step of the time series
- w_k is the angular frequency

The Morlet wavelet function is as follows:

$$\widehat{\varphi}(sw) = \pi^{-\frac{1}{4}} H(w) e^{-\frac{(sw-w_0)^2}{2}} \tag{3}$$

Where:

- H(w) is the Heaviside step function
- w_0 is the non-dimensional frequency

- s is the scale
- $\pi^{-1/4}$ is the normalization factor

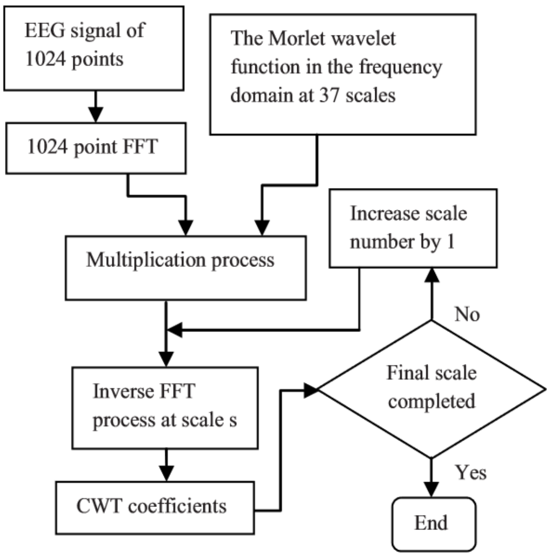
From [3] the computation of the CWT of the inputted EEG signal could be reduced to the following flow diagram.

Figure 1. The algorithm for the computation of the CWT [3]

From Figure 1 it is observed that the EEG signal is sampled in time such that 1024 samples of the EEG signal is taken and stored in memory. For a 1024 point FFT, 37 wavelet scales are required each of length 1024. The Morlet wavelet function is computed and stored in memory for each scale. The EEG signal is taken into the frequency domain by applying a 1024 point FFT to it which is then multiplied by the wavelet function at each scale. The inverse FFT is then found of the result at each wavelet scale to produce the CWT coefficients for that scale. The previous step is repeated for every scale and completed when the final scale has been computed [3].

4. Proposed Concept Model of the FPGA Archtecture

The flow chart described in Figure 1 could be implemented in VHDL. Therefore, when the VHDL file is implemented in on an FPGA board, the configuration bits consisting of the information pertaining to the interconnections of the logic elements is loaded which so as to achieve the goal of the VHDL coded file. Consequently a hardware based design is made for the determination of the CWT of the inputted EEG signal. Therefore the following figure shows a concept model as to how the FPGA could be used to analyze EEG signals.



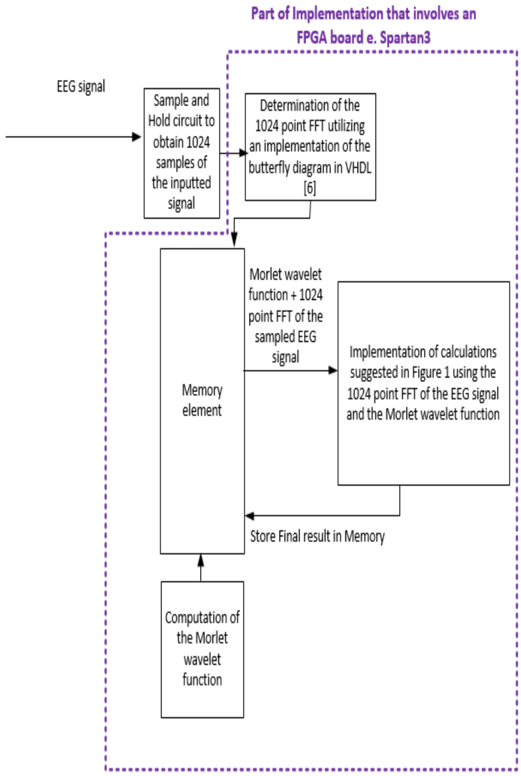


Figure 2. A Concept Model of the FPGA Implementation of the WT

5. Application of the FPGA implemenation for diagonosis of an epileptic

Now that the WT of the EEG signal is obtained, analysis could be done on the obtained signal for diagnosis. The approach taken in [7] could be adopted. This involves determining the WT of the EEG signal of several patients both epileptic and non-epileptic. As data is accumulated, a pattern recognition software, such as a statistical vector machine (SVM), could be used to determine if the WT of the EEG signal inputted corresponds to an epileptic or non-epileptic patient. Such an implementation is investigated in [7] and this paper does not cover the entire scope of the solution proposed as it is a very detailed process.

The classification of the EEG signal could be done through an FPGA implementation, however, due to the complexity of the processes involved in such a process, the resources of the architecture may be strained. Therefore, there should be consideration in terms of the computational resources provided by the selected FPGA architecture. If one FPGA cannot handle the WT of the EEG signal and the classification of the signal, then multiple architectures could be used provided that the proper communication protocols are implemented. However, this method may invoke some added cost to the overall implementation since FPGAs are relatively expensive.

6. PROs and CONs of Proposed Design

Since this is an FPGA architecture, then the system is subject to issues such as clock skew and static hazards. Additionally, as no pipelining strategies have been implemented as there were no timing simulations on each element since this is just a concept model. Therefore, to optimize performance of this design, pipelining strategies should be implemented. Since this is just a concept model, there is no guarantee that it will work.

With regard to the application of the proposed design to determine if a patient is an epileptic, concerns of there being sufficient memory for implementation of a statistical vector machine. Therefore, an external memory element may be required. If the processing time takes too long, an FPGA that facilitates a faster clock cycle and uses GPU processing could be utilized.

7. Conclusion

A concept model was made for the determination of the WT of EEG signals through an FPGA architecture. A suggested application of this concept model was made for the diagnosis of epileptic patients. However, this model should not be limited to that one application. A similar method to that suggested in section IV to diagnose patients with brain tumors or even sleep disorders. Since this is just a concept model, it is not 100% guaranteed to work and as of such there is a need for proper testing procedures to be implemented.

Acknowledgments

I would like to thank Mr. Marcus George for his sage advice in terms of the approach to writing this IEEE paper. Additionally, many thanks to the authors of the published papers that were referenced. These papers were very important in the conclusions made from this investigations.

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