The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process

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***Abstract*—We present the receiver in the first single-chip GSM/GPRS transceiver that incorporates full integration of quad-band receiver, transmitter, memory, power management, dedicated ARM processor and RF built-in self test in a 90-nm digital CMOS process. The architecture uses Nyquist rate direct RF sampling in the receiver and an all-digital phase-locked loop (PLL) for generating the local oscillator (LO). The receive chain uses discrete-time analog signal processing to down-convert, down-sample, filter and analog-to-digital convert the received signal. A feedback loop is provided at the mixer output and can be used to cancel DC-offsets as well to study linearization of the receive chain. The receiver meets a sensitivity of −110 dBm at 60 mA in a 1.4-V digital CMOS process in the presence of more than one million digital gates.**

***Index Terms*—All-digital phase-locked loop (ADPLL), built-in self-test (BIST), cellular, GPRS, GSM, low-area, low-cost, mobile phones, multi-tap direct sampling mixer (MTDSM), radio frequency (RF), sigma-delta, single-chip, system-on-chip (SoC), transceiver.**

I. Introduction

LOW-COST wireless handsets are expected to find widespread use in the next few years in Asia and Africa. Investment in cellular infra-structure is now the preferred choice in developing and under-developed nations for improving the communication infrastructure and consequently, improving the standard of living of their people. Cost reduction is traditionally achieved by developing highly integrated solutions in addition to reducing the cost of individual components that make up the solution. A wide spectrum of choices exist ranging from highly integrated *system in a package* (SIP) to highly integrated *system on a chip* (SoC). The entire phone solution includes SAW filters, RF switches, power amplifiers, RF transceivers for several indoor and cellular standards, power management ICs, audio and video codecs, baseband processors, application processors, FLASH memory and several peripherals. Considering the diverse technologies needed to construct a mobile phone, the best solution appears to be a combination of SoC and SIP technologies. Recent research attempts to address various low-cost integration options [1]–[3] for wireless transceivers. An interesting side effect of this interest is that it paves the way for development of economical multi-standard RF transceivers that would enable deployment of commercial software defined radio.

Despite the focus on cost reduction, performance requirements on wireless transceivers are not relaxed. In fact, it is quite the opposite that is true. Recent industry R&D focuses on developing very low-cost and high-performance wireless handsets supporting significantly extended applications ranging from basic voice and data communication to personal entertainment. Superior RF performance and state-of-the-art application support such as FM and digital TV reception offer competitive advantages. Hence, it is imperative to migrate to the latest digital CMOS process node as early as possible to support future applications in a cost-effective manner. The solution cost is kept low by integrating the RF transceiver circuits on the same state-of-the-art digital CMOS process. The new paradigm in analog design in the most recent digital CMOS process is presented in [4].

One of the first challenges in RF SoC integration is to assess whether integration of high-performance RF transceiver together with large number of digital gates is practical. The first successful attempt of integration of RF transceivers with digital baseband processors addressed Bluetooth radio [5]–[10] since Bluetooth specification requires RF sensitivity of only −70 dBm [11] in contrast to the −102 dBm [12] required by GSM. Despite the fact that the reported results surpassed the sensitivity required for official Bluetooth certification by more than 10 dB, the concern of degradation of noise performance of a highly integrated receiver while meeting GSM quality sensitivity performance was not adequately addressed. This paper addresses this question and presents the first single-chip GSM receiver in a 90-nm digital CMOS that achieves a sensitivity of −110 dBm without any process enhancements, which implies that it does not require any cost adder step to the baseline digital CMOS process.

One significance of this work is in demonstrating the feasibility of obtaining low noise figure in a receive chain in the presence of more than a million digital gates. Another significance is the development of very low-area, simple and highly programmable analog blocks that are controlled by software to guarantee best achievable performance. A third significance is the architecture of analog structures that are amenable to migration from one process node to the next without significant re-work. The approach used is to use signal processing to reduce analog area and complexity. The radio solution was tar-

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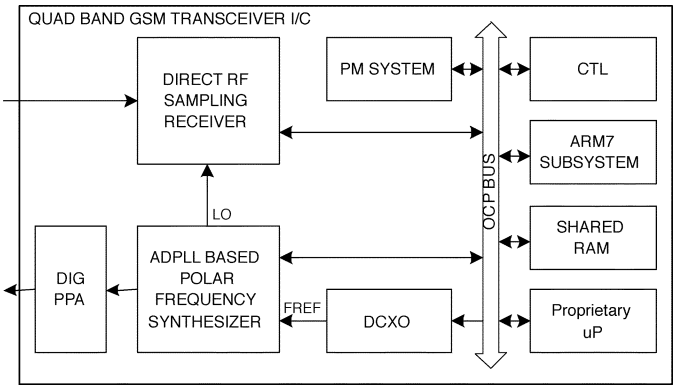


Fig. 1. First single-chip GSM transceiver.

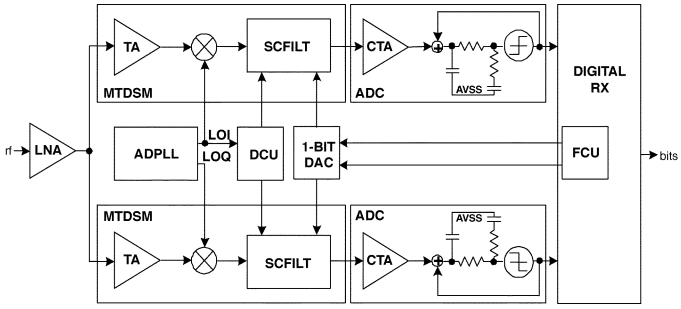


Fig. 2. Simplified block diagram of the receiver.

geted to meet quad-band GSM/GPRS specification in addition to supporting several experimental modes of operation.

The simplified block diagram of the RF SoC is shown in Fig. 1. This IC features full integration of quad-band receiver, transmitter, memory, power management, dedicated ARM processor and RF built-in self test (RFBIST) in a single RF SOC that is amenable to migration to newer deep submicron processes. The receiver uses direct RF sampling [10], [13], [14] of RF signal at Nyquist rate of the carrier. The transmitter uses an all-digital PLL [10], [15] together with a digital pre-power amplifier (PPA) for generating the transmit output as well as for generating the local oscillator (LO) for the receiver. The frequency reference is generated by an on-chip digitally controlled crystal oscillator (DCXO). The power supply of the analog and digital blocks is provided by an integrated power management (PM) system that comprises of several fully programmable low-dropout voltage regulators. The data flow through the single-chip radio is accomplished using an OCP bus that allows a proprietary micro-processor as well as an ARM7 sub-system (that has its own RAM and ROM) to control the radio functions. A small shared RAM is provided for the proprietary microprocessor. The control functions of the DRP are managed by the *control* (CTL) block that also incorporates system-wide JTAG control.

II. Receiver Architecture

The analog receive chain uses direct sampling of RF at Nyquist rate of the carrier frequency. Following the sampling operation, we use discrete-time analog signal processing to down-sample, filter and analog-to-digital convert the received signal. The fundamental philosophy is to move all filtering as close to the antenna as possible simplifying the design of subsequent analog blocks. The receiver architecture is shown in Fig. 2 and has similarities to the architecture presented in [10], [13]. The distinguishing characteristics of the presented receiver is that it offers additional filtering while significantly improving the linearity and noise performance. The additional filtering is needed to meet the extremely challenging GSM blocking specification where the received power of blocker at 3 MHz offset frequency can be 76 dB above the signal of interest. In addition, the design is also migrated from 135-nm to 90-nm CMOS process node. The supply voltage is reduced to 1.4 V in the 90-nm process. The presented transceiver addresses the stringent GSM specifications [12] in contrast to the relaxed Bluetooth specification addressed in [10] and [13].

III. Analog Receive Chain

The received signal is amplified in the low-noise amplifier (LNA), split into I/Q paths and converted to current using a transconductance amplifier (TA) stage. The current is then down-converted to a programmable low-IF frequency (defaults to 100 kHz) and integrated on a sampling capacitor at the LO rate. Considering plus and minus sides, the input signal is sampled at the Nyquist rate of the RF carrier. After initial decimation through a sinc filter response, a series of infinite impulse response (IIR) filtering follows RF sampling for close-in interferer rejection. These signal processing operations are performed in the multi-tap direct sampling mixer (MTDSM). A sigma-delta analog-to-digital converter (ADC) containing a front-end gain stage converts the analog signal to a digital representation. A feedback control unit (FCU) provides a single-bit feedback to the MTDSM to establish the common mode voltage for the MTDSM while canceling out differential offsets. The output of the I/Q ADCs are passed on to digital receive (DRX) chain that performs decimation, down-conversion to 0-IF and adjacent channel interference removal.

A. Analog Front-End

The analog front-end comprises of four LNAs for the four GSM bands, namely, GSM850, EGSM900, DCS1800, and PCS1900. The LO is generated by an all-digital PLL (ADPLL) that uses a digitally controlled oscillator (DCO) constructed by using an *LC* oscillator with several banks of digitally controlled varactors [10]. The RF input signal is amplified by the LNA and splits into I/Q paths where it is further amplified in the TA. It is then down-converted to a low intermediate frequency (IF) that is fully programmable (but defaults to 100 kHz) by the following mixers driven by an integrated local oscillator (LO). The output of the AFE are two replica current signals that are fed to the MTDSM.

1) LNA: Fig. 3 shows a simplified schematic diagram of the LNA. The LNA is actually implemented in a differential configuration to improve noise figure from potential substrate coupling from digital baseband circuits since the real impact of the switching noise of more than a million digital gates on the same substrate was not known to us. A variable gain feature with seven digitally configurable steps is implemented and shown in

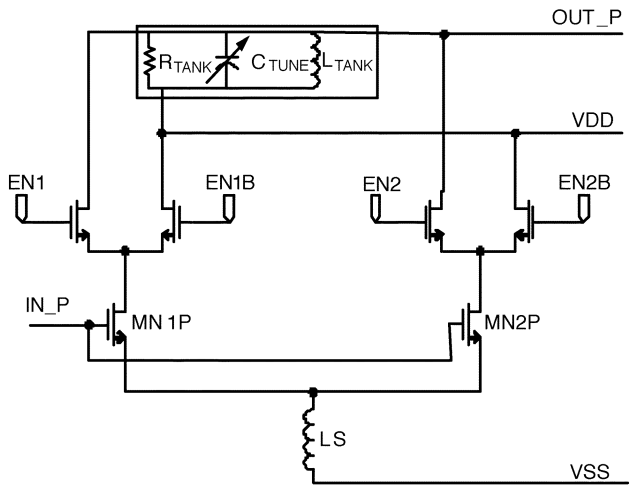


Fig. 3. Low noise amplifier. Only half section is shown for simplicity.

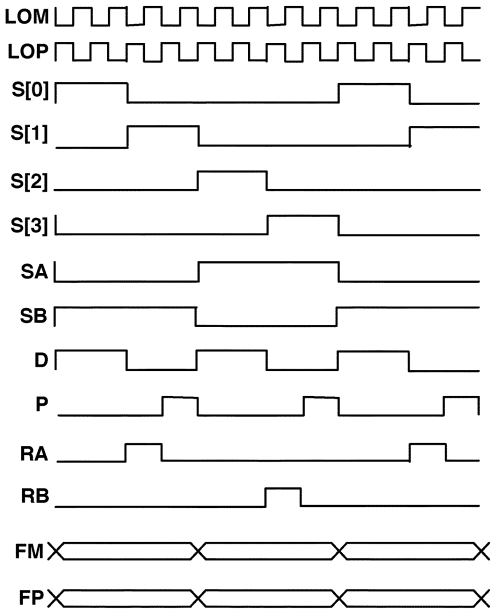


Fig. 4. Clocks supplied by the DCU.

Fig. 3. In the high gain mode, four voltage gains are realized with 2 dB step between 21 and 29 dB. In the low gain mode, there are three gain steps with 2 dB step between 3 and 9 dB. As shown in Fig. 3, the multiple cascode stages are connected in parallel with one source degeneration inductor (LS) and one inductive load. Each stage has two branches for digital configurability.

The top transistors of the cascode stage used for bypassing gain contribution are shunted to VDD. Since the bottom transistors of the cascode stage operate in all gain settings, to the first order, the input impedance is constant over gain selections which is critical for constant input power and noise matching. Inductive source degeneration using package bond wires is implemented to improve linearity. The LNA load is an on-chip spiral inductor using multiple metal layers with metal width $= 5.9$ μm, metal space $= 2$ μm, inner diameter $= 81.9$ μm, and 10 turns. This inductor is drawn as a center-tap configuration for better matching between the differential branches and achieving a higher quality factor (Q). The inductance is 8.9 nH and Q is greater than 4 at 900 MHz, where Q is defined as $||imag(y11)/real(y11)||$. To reduce the substrate effect, all doping under the inductor is blocked to preserve a higher resistivity.

B. Multi-Tap Direct Sampling Mixer

1) TA and Mixer: The second stage of the LNA consists of a transconductance amplifier (TA) which converts the input voltage to current. A highly efficient push-pull amplifier is chosen for the TA because of its low noise and good linearity characteristics. A 3-bit control word is provided to control the variable gain. A feedback amplifier is used to set the DC bias voltage of the drain node of the TA to VREF which is set to half of VDD so as to provide maximum signal swing. Large enough resistive load is provided to prevent significant input and output RF signal loading. The differential TA draws 4 mA in the maximum gain mode.

The TA and Mixer comprise the front-end of the MTDSM as shown in Fig. 2, however, the TA can be viewed as the second stage of the LNA. A double-balanced switching mixer is connected to the TA output via AC-coupling capacitors so that the DC voltage at the TA output is isolated from the mixer. This topology has an excellent feature of reduced 1/f noise because there is no DC current flow in the mixer switches, making it suitable for direct-conversion or near-zero IF receivers. By adding a capacitive load (C_H) to the mixer output, low pass filtering can be obtained to reduce large interferers. In this mixer, two switches are toggled by one of the out-of-phase LO signals (LO+, LO-) from the ADPLL. The large capacitive load introduces the first filtering stage in the receive chain that is very valuable to reduce the worst-case blocker at 3 MHz offset.

2) SCFILT: The MTDSM is shown in Fig. 2 as comprising the mixer and a switched capacitor filter (SCFILT). The clocks produced by the DCU to control the switches in the MTDSM are shown in Fig. 4. The detailed implementation of this circuit is shown in Fig. 5. The MTDSM samples the RF at Nyquist rate and provides a significantly filtered version of the signal to the following continuous-time amplifier. It is a passive switched capacitor circuit that allows highly linear, low-power, low-noise and low-area implementation of the entire filtering needed before the analog-to-digital (A/D) conversion. The power consumption of this block is dominated by the digital control unit (DCU) that generates the clock signals. Passive construction allows the possibility of ultra-high speed operation with low-power dissipation in addition to a wealth of programmability options.

The main part of DCU consists of a shift-register whose output is one-hot to reduce power dissipation. The *V–I* converted RF input signal is sampled directly on a combination of a history capacitor (C_H) and two rotating capacitors $(C_{R1} + C_{R1} = 2C_{R1})$. Two banks of rotating capacitors are provided that sample the RF input together with C_H. $N = 4$ samples are accumulated on $C_H + 2C_{R1}$ capacitor in the DCS1800 and PCS1900 bands while $N = 2$ samples are accumulated when operating in the GSM850 and EGSM900.

For N LO cycles, two rotating capacitors in the first bank sample the RF input together with C_H while the capacitors in

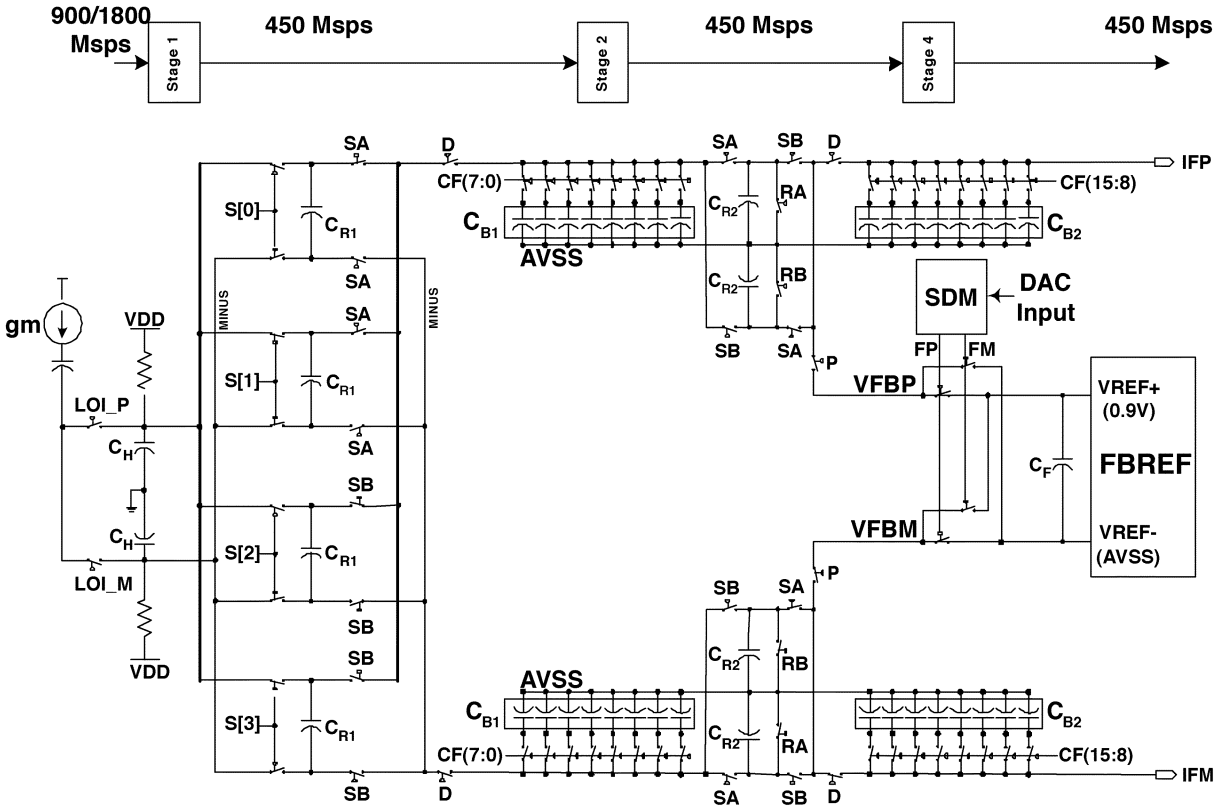


Fig. 5. Multi-tap direct sampling mixer.

the second bank charge share with C_{B1}. The decimation operation creates a sinc filter that has notches at the foldover frequencies, $kf_{\rm LO}/N$, where k is a positive integer and $f_{\rm LO}$ is the frequency of the LO. The natural response of the *gm-C* filter provides an anti-aliasing prefiltering prior to the first sinc filter.

Rotating $2C_{R1}$ on C_H creates an IIR filter response. When the two C_{R1} capacitors in one bank have completed sampling, these carry the snapshots of past N RF samples passed through the first IIR filter stage (created by the charge sharing between $2C_{R1}$ and C_H). Next, the two C_{R1} capacitors are charge shared with the buffer capacitor C_{B1} and a second rotating capacitor, C_{R2}. The overall effect is to create a second IIR filtering stage in which $2C_{R1}$ delivers input, C_{B1} holds the memory and C_{R2} captures a glimpse of the output of the second IIR filter stage. This charge is subsequently shared with a second buffer capacitor, C_{B2}, resulting in the third IIR filter stage. While charge samples are passed on from the C_H to C_{B2} through a series of charge combination, splitting and recombination operations, the input RF samples are always accumulated on C_H together with $2C_{R1}$ capacitor from one bank. Therefore, the TA sees a constant load at its output.

The three IIR filters have corner frequencies that are given by respective ratios of rotating capacitors to fixed capacitors and may be readjusted by changing the size of the capacitors. Each capacitor can be individually programmed to control the corner frequencies of the filter. The noise figure of the MTDSM is dominated by the size of the smallest rotating capacitor and can be controlled by proper selection of the C_{R1} and C_{R2} values.

After the charge sharing is completed during the readout of C_{R2} on C_{B2}, C_{R2} is reset and precharged by the 1-bit feedback circuit provided by a sigma-delta modulator that connects the output of a low-noise feedback voltage reference (FBREF) to C_{R2}. Zero digital-to-analog converter (DAC) code produces approximately 50% duty cycle output which brings the common mode exactly at half of VREF+. In the presence of a DC-offset, the duty cycle is changed with sigma-delta noise shaping to cancel the DC-offset voltage. The capacitor ratios in the MTDSM are programmable that allows the analog filter corner frequency to be adjustable over a wide range, thereby allowing its use in a multi-standard environment.

C. A/D Converter

The analog back-end consists of a pre-amplification stage preceding a second-order passive sigma-delta ADC operating at the rate of LO/N. Since this clock is generated by integer division of the LO, it has very small jitter. The loop filter consists of a *gm-C* stage followed by an *RC* filter. The quantizer produces 1-bit output at the rate between 430 MSps and 500 MSps depending upon the band and the channel. This corresponds to an over-sampling ratio greater than 1000 for which the ADC provides a dynamic range in excess of 80 dB. The pre-amplification allows this dynamic range window to be translated up or or down by the programmable gain of the continuous time amplifier (CTA).

The key feature of the ADC is the passive loop filter that is realized in the continuous time domain and allows low-power operation. The loop gain is provided by the comparator gain as no gain can be provided by the passive loop filter. The input is driven by a transconductance stage whose output sees the feedback node of the ADC that has very low swing signal.

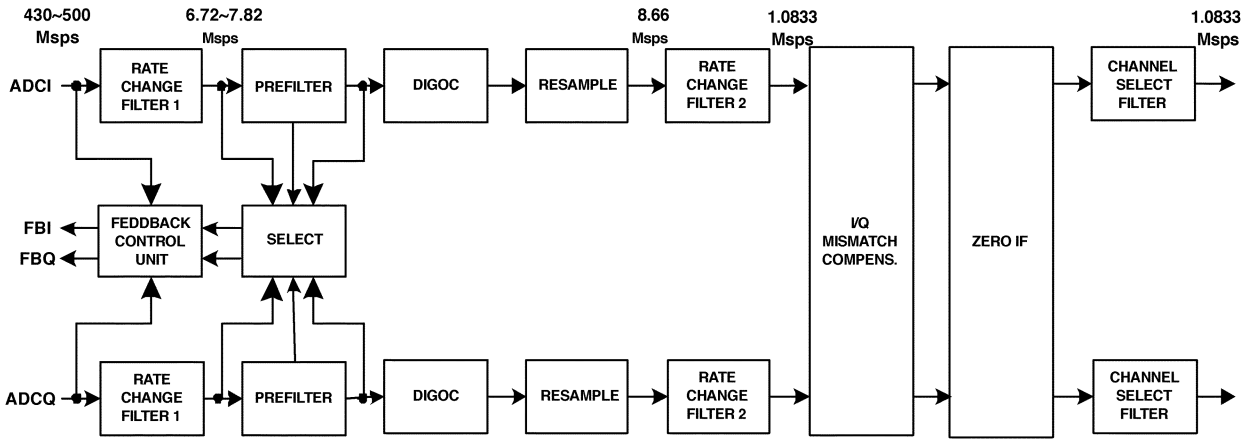


Fig. 6. Digital receive chain.

D. Feedback Subsystem

The feedback system consists of a DC estimator connected to the output of the ADC that controls the 1-bit DAC output. The DC estimation is performed after band-limiting the noise and estimating the minimum and maximum values of the remaining signal. The DC value is the average of the minimum and maximum. Other DC estimation techniques such as averaging over a programmable window are also supported.

The feedback system injects charge at C_{R2} during the precharge phase of the MTDSM. A sigma-delta engine generates a noise-shaped 1-bit output of programmable order that is applied to control the charge injection on differential C_{R2} in positive or the negative direction. The charge injected is equal to VREF/C_{R2}, where VREF $= 0.9$ V. For maximum code of all-ones, the positive side of the MTDSM is slowly charged all the way to VREF as C_{R2} mimics a switched-capacitor resistor. In this case, the negative side is discharged all the way to 0. For the most negative code of all-zeros, the negative side of the MTDSM is slowly charged all the way to VREF while the positive side is discharged to 0. For a 50% density of ones, both the positive and negative sides are charged to VREF$/2$ which is the intended bias point. Any offset of the average density of ones from 50% creates a corresponding offset voltage between the positive and negative sides of the MTDSM. The offset voltage is given as $2 \times 0.9(d - 0.5)$ V, where d is the density of ones in the sigma-delta DAC output and equals 1 for all-ones code and 0 for all-zeros code.

The feedback path transfers charge from C_{R2} to C_{B1}, thereby creating an IIR filter pole whose corner frequency is determined by the ratio of C_{R2} and C_{B1}. This is because following precharge, C_{R2} is first charge shared with C_{B1}. The result of the IIR filtering settles on C_{R2} and is consequently charge shared with C_{B2}. Hence, the feedback charge goes through a second-order IIR filter which significantly reduces the shaped noise at the sigma-delta DAC output. The noise shaping dramatically reduces the quantization noise floor for the feedback signal, pushing it below the thermal noise floor of the buffer that generates the FBREF.

IV. Digital Receive Chain

The digital receive chain shown in Fig. 6 comprises the necessary anti-aliasing filtering to lower the data rate to the final desired rate of 1.0833 MSps which is 4X the symbol rate in GSM. In order to provide the lowest jitter clock in the system to the ADC, the input sample rate is directly derived from the LO by an integer division. The LO changes frequency every time-slot when a channel is hopped and results in a variable data rate. The digital baseband, however, expects to see samples at a constant clock rate. The two requirements are simultaneously satisfied by using a digital resampler separating the digital receive chain in to two halves. The digital front-end contains circuits operating at LO dependent clock rate while the digital backend contains circuits that operate at the fixed clock rate after digital resampling.

A. Digital Front-End

The digital front-end consists of a first rate change filter (RCF1) that provides anti-aliasing and decimation filtering to reduce the clock rate to $f_{\rm LO}/64N$. It is implemented as a cascade of a $sinc^4$ polyphase structure that decimates the rate by 16 followed by two half-band finite impulse response (FIR) filters. The design of the first stage is critical in order to have low power dissipation in the digital front-end. This is because the output rate of the ADC is very high and the use of traditional CIC filtering stages create large word-lengths very early in the initial decimation stages. To relieve the design of the high-speed interface between the ADC and RCF1, the ADC output is packed to 8-bit words for transportation across the interface.

Reduction in area is achieved by interleaving I and Q data and by implementing each phase of the filter as a hard-wired lookup table. The filter provides more than 150 dB of rejection in the 400 kHz band and more than 87 dB of rejection in the 4 MHz band. For simplicity, the data paths of only three out of 16 phases is shown in Fig. 6. The sixteen 2×1 multiplexers perform I/Q interleaving. Other than sixteen 16×1 13-bit multiplexers in each phase, the only other significant combinational logic is the carry-save adder (CSA) tree that adds sixteen 13-bit numbers to

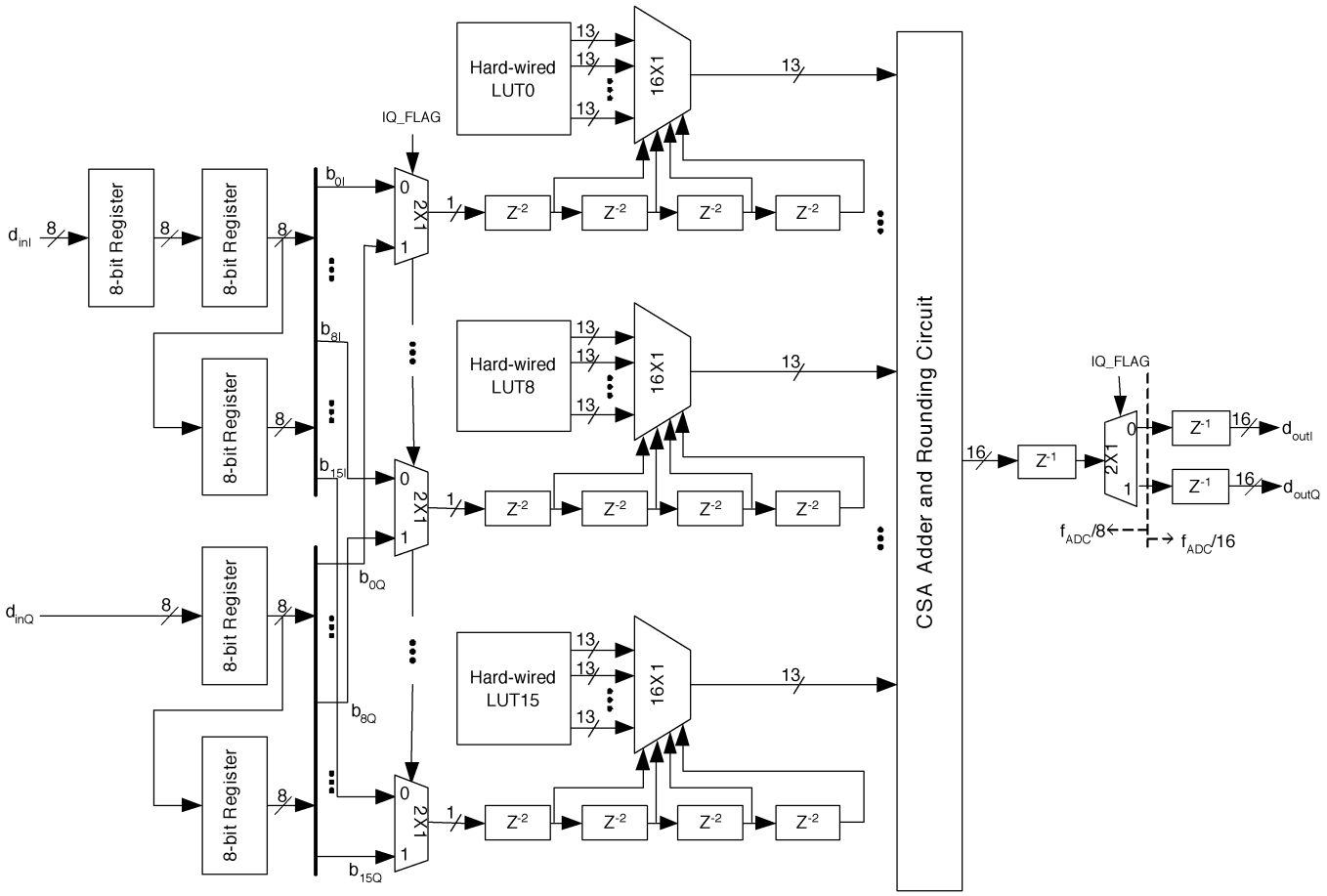


Fig. 7. I/Q interleaved polyphase implementation of RCF1.

compute a 17-bit signed 2's complement sum and then round it to 16 bits.

There is an additional 8-bit register at I-channel input in Fig. 7. In the absence of this register, an undesired phase mismatch equal to one $f_{\rm ADC}/8$ clock cycle will exist between I and Q channels, where $f_{\rm ADC} = f_{\rm LO}/N$. The IQ_FLAG in Fig. 7 is used to select between I and Q channel data. This flag is generated simply by dividing the $f_{\rm ADC}/8$ clock by 2. Finally, a de-interleaving 2×1 demultiplexer shown on the right side of Fig. 7 is used to separate I and Q data at the output and bring it to the output rate. The details of RCF1 are described in [16].

Following the RCF1, an 11-tap linear phase FIR filter is used as a prefilter preceding the resampler. Its area is reduced by using sub-structure sharing by employing common sub-expression elimination techniques. The prefilter output is used by the FCU to estimate the DC-offset at the mixer output. An inverse value is fed back to the MTDSM using the feedback loop to force the residual DC-offset to zero. Of course, the loop gain must be estimated and compensated in order to calculate the feedback value. This is done at the beginning of every packet. The fed back value is kept constant throughout the duration of the packet. Next, the residual DC-offset that could not be corrected by the FCU is corrected by the digital offset corrector (DIGOC) which supports several feed-forward and feedback modes of offset removal. Some of these modes are provided for experimental studies.

B. Digital Resampling

The resampler follows DIGOC and converts the sample rate from $f_{\rm LO}/64N$ to a fixed output rate of 8.66 Msps. The resampler needs to adapt each time slot as the channel is changed. The resampler is implemented as a Farrow structure incorporating a second-order Lagrange polynomial based resampling [17] in the default mode of operation. It supports first-, second-, and third-order Lagrange polynomial resampling.

C. Digital Backend

Following the resampler, the sample rate is further decimated by a second rate change filter (RCF2) to reduce clock rates for subsequent blocks. RCF2 is implemented as a cascade of three decimation-by-2 half-band FIR filters. The output data rate is converted to 4X the baud rate using linear phase FIR filtering.

An I/Q mismatch block reduces the mismatches between I and Q branches by ensuring that the cross-correlation and the difference between the auto-correlation between I and Q data is close to zero. It uses an LMS algorithm for adaptation that is described in detail in [18]. The IF frequency is then converted from the default low IF of 100 kHz to DC by the zero IF block. Since the selection of IF frequency is fully programmable, the zero IF block is also programmable to support the second down-conversion step. The final filtering is performed using a fully programmable 64-tap channel select filter (CSF) that uses a single

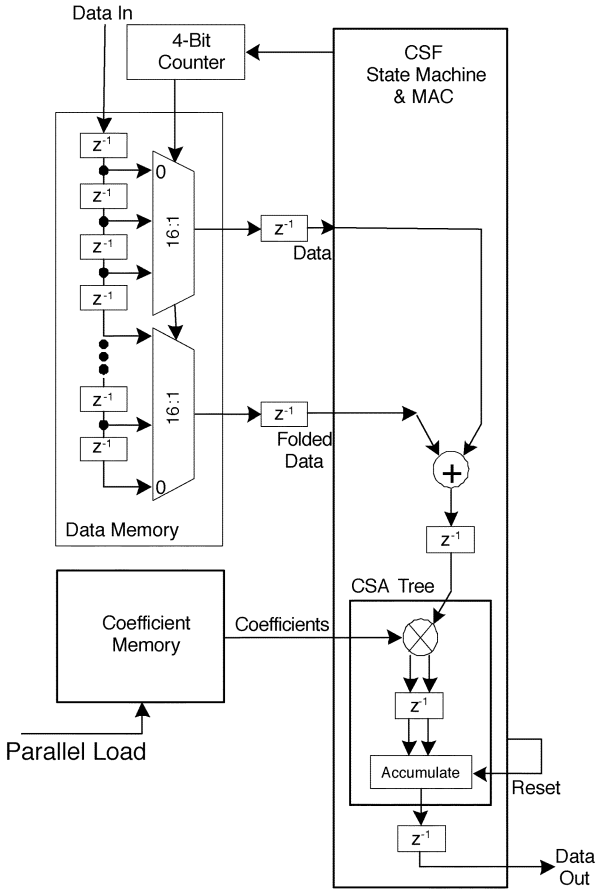


Fig. 8. One 32-tap stage of the final channel select filter.

dedicated MAC unit. It is implemented as a cascade of three 32-tap filter stages. By default, only two stages are used to address the GSM specification. The third stage was provided to support experimental modes of operation.

A simplified block diagram of one 32-tap filtering stage in CSF is shown in Fig. 8. The data is shifted in a 32-tap shift register that is 16 bits wide. A coefficient memory holds the filter coefficients. The data is folded as the filter is linear phase. The output of the filter is computed using a MAC unit implemented using CSA techniques. The CSA output is converted to normal binary format when the operation is completed. This reduces the amount of switching activity required to compute the final output, thereby reducing the power dissipation of the filter.

In a special test mode, the clocks of the receiver are changed to support Bluetooth reception. In this case, unneeded blocks are bypassed and channel select filtering is reprogrammed to adapt to the Bluetooth standard. Since the channel bandwidth is 1 MHz in Bluetooth compared to 200 kHz in GSM, the MTDSM filter poles are moved out to accommodate the received channel. The clock rates in the digital receive chain are increased by a factor of 4 following the resampler.

V. Continuous Operation of the External Feedback Loop

The feedback loop is operated in the normal operation in an open loop fashion for correcting DC-offsets. However, this is not the only way to operate this loop. When operated continuously as an experimental feedback mode, the FCU provides a continuous feedback stream that cancels the signal and interferers at C_{R2}. In this mode, the FCU routes the output of the ADC directly to control the feedback capacitor C_{R2} in a negative feedback. Hence, the sigma-delta DAC used in default functional mode is disconnected to the MTDSM. Since the ADC produces 1-bit output, the conversion to this mode is seamless.

The transfer function of the receiver chain changes since the CTA and the MTDSM are now inside the feedback loop. The CTA now provides the loop gain while the MTDSM functions as a loop filter. The top plate of C_{B1} becomes the feedback node and approximates a virtual ground. Since the MTDSM provides no isolation in the reverse direction, the feedback charge is up-converted by the mixer and makes its way all the way to the TA output, thereby linearizing the entire receive chain with the exception of the LNA. The impedance seen by the TA changes to a new value shifting the pole inside towards DC. This feature allows relaxation of linearity requirements of the baseband amplifiers in the receive chain. The overall linearity of the chain is measured to improve by 5 dB in this mode, however, it comes at the cost of slight degradation of the noise figure.

This mode demonstrates complete reconfiguration of the receiver architecture to allow entirely different tradeoffs. We found this mode to be useful since the overall system linearity could be improved in the presence of strong blockers by transforming the receiver architecture to this experimental mode. The presence of strong blockers can be detected by monitoring the signal at the output of the ADC by the dedicated processor that services the transceiver.

VI. All-Digital Transmitter

A transmitter that is well-suited for a deep-submicron CMOS implementation is shown in Fig. 9. It performs the quadrature modulation in polar domain [10], [15] in addition to the generation of the LO for the receiver. All clocks in the system are derived directly from this source.

The architecture is built using digital techniques that exploit the high speed and high density of the advanced CMOS, while avoiding problems related to voltage headroom. An ADPLL replaces the conventional RF synthesizer architecture, based on a voltage-controlled oscillator (VCO) and a phase/frequency detector and charge-pump combination, with a digitally controlled oscillator (DCO) and a time-to-digital converter (TDC). All inputs and outputs are digital at multi-GHz frequency—the 40-ps rise time makes an almost perfect square wave. The full digital control of the RF frequency allows digital implementation of the PLL [10], [15].

At the heart of the ADPLL lies a DCO. The oscillator core operates at twice the 1.6–2.0-GHz high-band frequency. The DCO tuning capacitance is split into a large number of tiny capacitors that are selected digitally. The advanced lithography allows creation of extremely fine variable capacitors (varactors)—about 40 attofarads of capacitance per step, which equates to the control of only 250 electrons entering or leaving the resonating *LC* tank. Despite the small capacitance step, the resulting frequency step at the 2-GHz RF output is 10–20 kHz, which is too coarse for wireless applications. Thus, the fast switching capability of the transistors is utilized by performing programmable

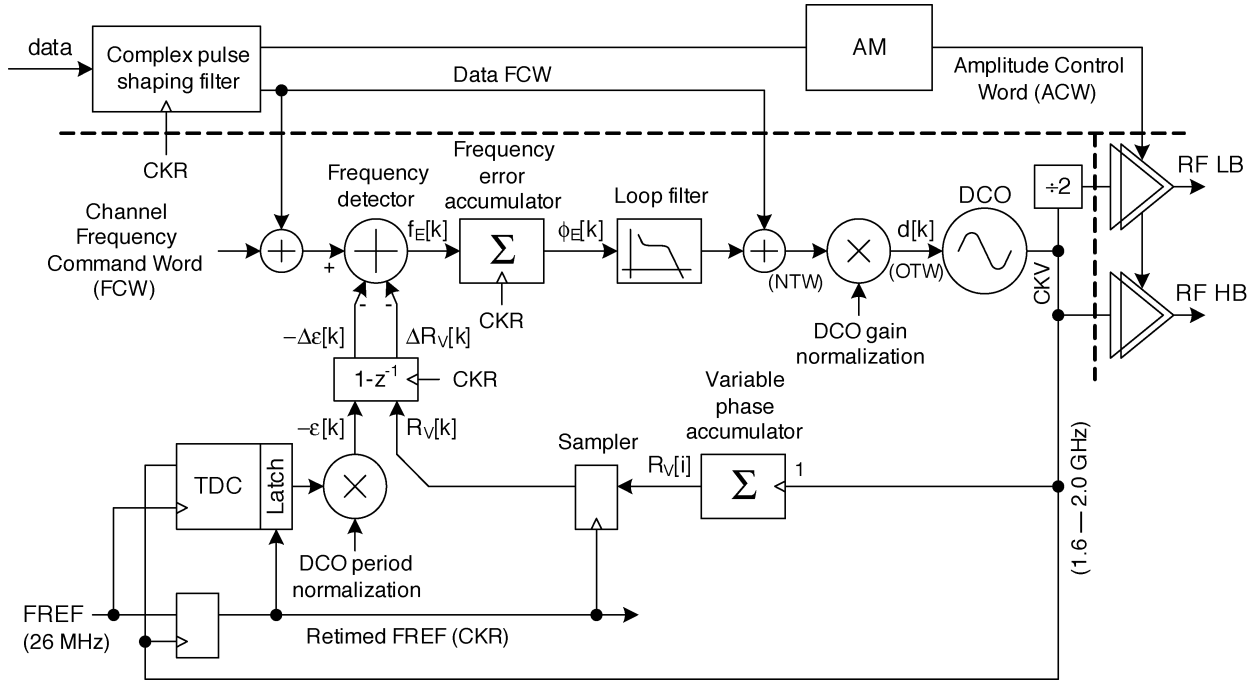


Fig. 9. All-digital PLL (ADPLL) and polar transmitter. LO is generated by the ADPLL.

high-speed (225–900 MHz) $\Sigma\Delta$ dithering of the 250 electrons in the finest varactors. The duty cycle of the high/low capacitive states establishes the time-averaged resonating frequency resolution, now less than 1 kHz. All the varactors are realized as n-poly/n-well MOSCAP devices that operate in the flat regions of their *C–V* curves.

The ADPLL operates in a digitally synchronous fixed-point phase domain as follows. The variable phase $R_V[i]$ is determined by counting the number of rising clock transitions of the DCO oscillator clock CKV:

$$R_V[i] = \sum_{l=0}^{i} 1. \tag{1}$$

The index i indicates the DCO edge activity. The FREF-sampled variable phase $R_V[k]$, where k is the index of the FREF edge activity, is fixed-point concatenated with the normalized TDC output $\varepsilon[k]$. The TDC measures and quantizes the time differences between the FREF and DCO edges. The sampled differentiated variable phase is subtracted from FCW by the digital frequency detector. The frequency error $f_E[k]$ samples

$$f_E[k] = FCW - [(R_V[k] - \varepsilon[k]) - (R_V[k-1]) - \varepsilon[k-1])] \tag{2}$$

are accumulated to create the phase error $\phi_E[k]$ samples

$$\phi_E[k] = \sum_{l=0}^{k} f_E[k] \tag{3}$$

which are then filtered by a fourth-order IIR filter and scaled by a proportional loop attenuator α. A parallel feed with coefficient ρ adds an integrated term to create type-II loop characteristics, which suppresses the DCO flicker noise.

The IIR filter is a cascade of four single stage filters, each satisfying the following equation:

$$y[k] = (1-\lambda)\cdot y[k-1] + \lambda \cdot x[k] \tag{4}$$

where $x[k]$ is the current input, $y[k]$ is the current output, and λ is the configurable coefficient. The 4-pole IIR filter attenuates the reference and TDC quantization noise at the 80 dB/dec slope, primarily to meet the GSM spectral mask requirements at 400 kHz offset. The filtered and scaled phase error samples are then multiplied by the DCO gain $K_{\rm DCO}$ normalization factor $f_R/\widehat{K}_{\rm DCO}$, where f_R is the reference frequency and $\widehat{K}_{\rm DCO}$ is the DCO gain estimate, to make the loop characteristics and modulation independent from $K_{\rm DCO}$. The modulating data is injected into two points of the ADPLL for the direct frequency modulation. A hitless gear-shifting mechanism for the dynamic loop bandwidth control serves to reduce the settling time. It changes the loop attenuator α several times during the frequency locking while adding the $(\alpha_1/\alpha_2 - 1)\phi_1$ DC-offset to the phase error, where indexes 1 and 2 stand for before and after the event, respectively. Of course, $\phi_1 = \phi_2$, since the phase is to be continuous.

The FREF input is resampled by the RF oscillator clock, and the resulting retimed clock (CKR) is used throughout the system. This ensures that the massive digital logic is clocked after the quiet interval of the phase error detection by the TDC.

The transmitter architecture is fully digital and takes advantage of the wideband frequency modulation capability of the all-digital PLL by adjusting its digital frequency command word. The modulation method is an exact digital two-point scheme, with one feed directly modulating the DCO frequency deviation while the other is compensating for the developed excess phase error. The DCO gain characteristics are constantly calibrated through digital logic to provide the lowest possible distortion

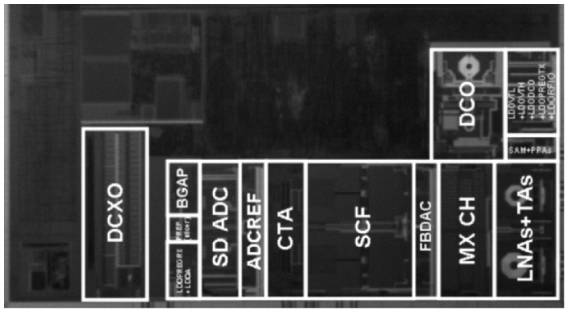


Fig. 10. Die micrograph of the single-chip GSM Radio.

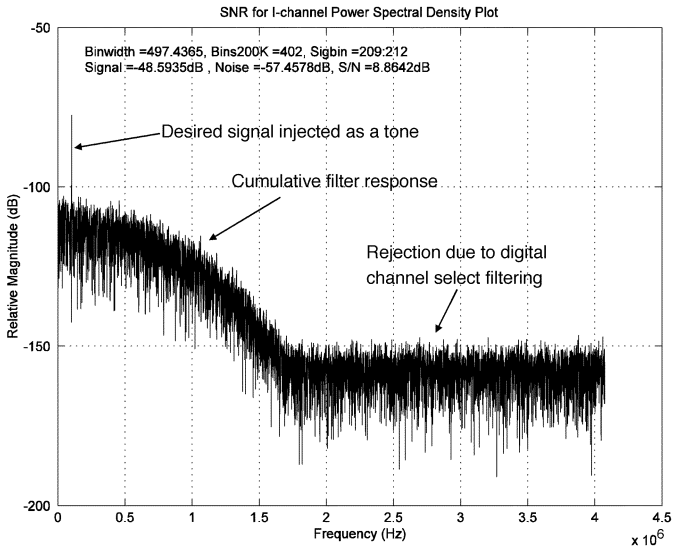


Fig. 11. Spectrum at receiver output at sensitivity of −110 dBm.

of the transmitted waveform. The amplitude modulation path is built on a digitally controlled power amplifier (DPA) with a large array of MOS switches and operates in near-class-E mode. The RF amplitude is regulated by controlling the number of active switches. Fine amplitude resolution is achieved through high-speed $\Sigma\Delta$ transistor switch dithering. Despite the high speed of digital logic operation, the overall power consumption of the transmitter architecture is lower than that of architectures to date.

VII. RFBIST

Several RF built-in self test (RFBIST) functions are supported by the receiver that includes digital loop-back, mixed-signal feedback loop (for DC-offset cancellation), and TX-RX RF loop-back at the mixer. Coupling at the package can be used to realize an external TX-RX feedback loop that incorporates the entire transceiver.

A programmable sine/cosine waveform generates feedback signals that are fed to the mixer through the offset correction loop to establish an additional analog feedback. This loop can be used to perform several calibration and test functions.

VIII. Performance, Area, and Power Dissipation

The digital baseband that implements the detection algorithms is not integrated on this test chip. The measured typical receiver sensitivity is −110 dBm which is 5 dB better than the GSM specifications. The receiver typically consumes 60 mA current at the internal regulated voltage of 1.4 V without the baseband processor. It provides an IIP2 of 46 dBm and IIP3 of −25 dBm at the NF of 2 dB in the main functional operation. The IIP3 improves by 5 dB in the second feedback mode, meeting the GSM specifications with significant margin. A raw image-regection ratio between 35–40 dB is achieved that is improved to 50–55 dB using the I/Q mismatch circuitry [18].

The die micrograph of the complete single-chip GSM radio is shown in Fig. 10 and it occupies 7.36 mm^2. This chip is fabricated in a 90-nm digital CMOS process with copper interconnects, 0.27 μm minimum metal pitch, 2.9-nm gate oxide thickness, and no extra processing steps.

The measured spectrum at the final receiver output is shown in Fig. 11. Notice that the output spectrum is very clean despite the fact that 1.2 million gates are operating on this chip and it has integrated power management. Notice that the frequency of operation at this output is only 1.0833 Msps and that all out-of-band energy has been removed by the combined analog and digital filtering in the receive chain. The receive chain is designed to only protect the channel of interest against noise or spur folding. Based on this measurement, it can be seen that a clean spectrum can be obtained despite the fact that the solution is highly integrated. Also notice that the 1/f noise is also not observable in the output spectrum for the sensitivity test.

This work is the first report of a fully integrated GSM transceiver, hence, it is difficult to compare with previous published works [19]–[22] that would require selecting multiple chips. The performance of this chip, nevertheless, is the best in class. The area of the transceiver is also best in class.

IX. Conclusion

The first single-chip GSM transceiver is presented in 90-nm CMOS process. This test chip does not integrate the digital baseband processor, however, an ARM7 subsystem is integrated to study noise coupling impacts of deep-submicron integration. The chip demonstrates a sensitivity of −110 dBm showing that single-chip GSM transceivers may be constructed using direct RF sampling technique. It only consumes 60 mA current at a supply voltage of 1.4 V and occupies 7.36 mm^2.

References

[1] J. Sevenhans, F. O. Eynde, and P. Reusens, "The silicon radio decade," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pt. 2, pp. 235–244, Jan. 2002.

[2] E. McShane, M. Trivedi, X. Ying, P. Khandelwal, A. Mulay, and K. Shenai, "One-chip wonders," *IEEE Circuits Devices Mag.*, vol. 14, no. 5, pp. 35–42, Sep. 1998.

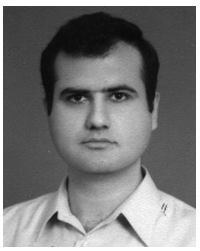
[3] T. Schafbauer *et al.*, "Integration of high-performance, low-leakage and mixed-signal features into a 100 nm CMOS technology," in *Symp. VLSI Technology Dig. Tech. Papers*, Jun. 2002, pp. 62–63.

[4] K. Muhammad, R. B. Staszewski, and D. Leipold, "Digital RF processing: toward low-cost reconfigurable radios," *IEEE Commun. Mag.*, vol. 43, no. 8, pp. 105–113, Aug. 2005.

[5] H. Darabi *et al.*, "A 2.4 GHz CMOS transceiver for bluetooth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, vol. 447, pp. 200–201.

[6] A. Ajjikuttira *et al.*, "A fully-integrated CMOS RFIC for bluetooth applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, vol. 447, pp. 198–199.

[7] F. O. Eynde *et al.*, "A fully-integrated single-chip SOC for Bluetooth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, vol. 447, pp. 196–197.
[8] N. Filiol *et al.*, "A 22 mW Bluetooth RF transceiver with direct RF modulation and on-chip IF filtering," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, vol. 447, pp. 202–203.
[9] A. Zolfaghari, A. Chan, and B. Razavi, "A 2.4 GHz 34 mW CMOS transceiver for frequency-hopping and direct-sequence applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, vol. 447, pp. 418–419.
[10] R. B. Staszewski, K. Muhammad, and D. Leipold *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.
[11] Specification of the Bluetooth System: Core System Package [Controller volume], Part A, Radio Specification. Nov. 5, 2003 [Online]. Available: https://www.bluetooth.org
[12] GSM Specification: Radio Transmission and Reception, GSM 05.05 version 8.5.1, ETSI EN 300 910, Version 8.5.1. Nov. 2000 [Online]. Available: http://www.etsi.org
[13] K. Muhammad *et al.*, "Discrete-time Bluetooth receiver in 0.13 μm digital CMOS process," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 268–269.
[14] K. Muhammad and R. B. Staszewski, "Direct RF sampling mixer with recursive filtering in charge domain," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2004, vol. 1, pp. 577–580.
[15] R. B. Staszewski, J. Wallberg, and S. Rezeq *et al.*, "All-digital PLL and GSM/EDGE transmitter in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2005, pp. 316–317.
[16] K. Muhammad, I. Elahi, and T. Jung, "A low-area decimation filter for ultrahigh speed 1-bit $\Sigma\Delta$A/D converters," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2005, pp. 77–80.
[17] L. Erup, F. M. Gardner, and R.A. Harris, "Interpolation in digital modems. II. Implementation and performance," *IEEE Trans. Commun.*, vol. 41, no. 6, pp. 998–1008, Jun. 1993.
[18] I. Elahi, K. Muhammad, and P. T. Balsara, "I/Q mismatch compensation in a low-IF receiver in 90 nm CMOS process," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2005, pp. 542–543.
[19] P. Orsatti, F. Piazza, and Q. Huang, "A 20-mA-receive, 55-mA-transmit, single-chip GSM transceiver in 0.25 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1869–1880, Dec. 1999.
[20] S. Tadjpour, E. Cijvat, E. Hegazi, and A. Abidi, "A 900 MHz dual conversion low-IF GSM receiver in 0.35 μm CMOS," in *IEEE J. Solid-State Circuits*, Jun. 2002, pp. 292–293.
[21] J. Ryynanen *et al.*, " A dual-band RF front-end for WCDMA and GSM applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1198–1204, Aug. 2001.
[22] M. Stayert *et al.*, "A single-chip CMOS transceiver for DCS-1800 wireless communications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1998, pp. 48–49, 411.



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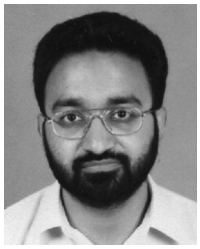

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