

## Citations of Lukas Sekanina's work

(collected from IEEE Xplore, ACM DL, Springer, Scopus, and Internet)

Papers with non-zero citations	125
Citations	1051
H-index	17

last update: 19.5.2017

		Year	Type	ISI	Cited	Inserted
	<b>2016</b>					
	<b>Vasicek Z., Sekanina L.: Evolutionary Design of Complex Approximate Combinational Circuits. Genetic Programming and Evolvable Machines, vol. 17, no. 2, 2016, p. 169-192</b>				<b>1</b>	
1	Alsadoon A., Prasad P.W.C., Beg A.: Using software simulators to enhance the learning of digital logic design for the information technology students. European Journal of Engineering Education 2016 TBD	2016	J			28.7.2016
	<b>Mrazek V., Sarwar S. S., Sekanina L., Vasicek Z., Roy K.: Design of Power-Efficient Approximate Multipliers for Approximate Artificial Neural Networks. In: Proc. of the IEEE/ACM International Conference on Computer-Aided Design. ACM, 2016, p. 811-817</b>				<b>1</b>	
1	Jiang H., Liu C., Liu L., Lombardi F., Han J.: A Review, Classification and Comparative Evaluation of Approximate Arithmetic Circuits. ACM Journal on Emerging Technologies in Computing Systems, Vol. V, No N, 2017, p. TBD	2017	JIF			19.5.2017
	<b>Sekanina L. Introduction to Approximate Computing: Embedded Tutorial. In: 19th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems. IEEE, 2016, p. 90-95</b>				<b>1</b>	
1	Qiqieh I., Shafik R., Tarawneh G., Sokolov D., Yakovlev A.: Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression. In Desing, Automation and Test in Europe (DATE), IEEE, 2017, p. 1-6	2017	CIEEE			19.5.2017
	<b>2015</b>					
	<b>Vasicek Z., Sekanina L.: Evolutionary Approach to Approximate Digital Circuits Design. IEEE Transactions on Evolutionary Computation. vol. 19, no. 3, 2015, p. 432-444</b>				<b>12</b>	
1	Wang L., Yang B., Wang S., Liang Z.: Building Image Feature Kinetics for Cement Hydration using Gene Expression Programming with Similarity Weight Tournament Selection. IEEE Trans. on Evolutionary Computation, Vol. 19, No. 5, 2015 p. 679-693	2015	JIF	1		18.12.2014
2	GARG SHIVANI, BIRLA, SHILPI, SHUKLA NEERAJ K. R.: A Survey on FPGA Prototyping of Digital Architectures of Edge Detection Techniques. International Journal of Engineering Science & Technology, Vol. 6, No. 10, 2014, p. 670-696	2014	J			18.12.2014

3	Tao Y., Zhang Q., Zhang L., Zhang Y.: A systematic EHW approach to the evolutionary design of sequential circuits. <i>Soft Computing</i> , Vol. 20, No. 12, 2016, p. 5025-5038	2016	JIF	1		30.12.2015
4	Yang Q. et al.: Adaptive Multimodal Continuous Ant Colony Optimization. <i>IEEE Transactions on Evolutionary Computation</i> , Vol. 21. No. 2, 2017, p. 191-205	2017	JIF	1		28.7.2016
5	Liu T., Jiao L., Ma W., Ma J., Shang R.: A new quantum-behaved particle swarm optimization based on cultural evolution mechanism for multiobjective problems. <i>Knowledge-Based Systems</i> , 2016, p. 1-10 TBD	2016	JIF			28.7.2016
6	Slowik A.: On fast randomly generation of population of minimal phase and stable biquad sections for evolutionary digital filters design methods. In 8th Asian Conference on Intelligent Information and Database Systems, ACIIDS, LNCS 9621, 2016, p. 511-520	2016	LNCS			28.7.2016
7	Trefzer M.A., Lawson D. M. R., Bale S. J., Walker J., Tyrrell A. M.: Hierarchical Strategies for Efficient Fault Recovery on the Reconfigurable PAnDA Device. <i>IEEE Transactions on Computers</i> , vol. PP, no.99, 2017?, p.1-16 TBD	2016	JIF	1		1.12.2016
8	Yang P., Tang K., Yao X.: Turning High-dimensional Optimization into Computationally Expensive Optimization. <i>IEEE Transactions on Evolutionary Computation</i> , 2017, vol.PP, no.99, pp.1-1	2017	JIF	1		19.5.2017
9	Babu K.S., Balaji N.: Approximation of Digital Circuits Using Cartesian Genetic Programming. In International Conference on Communication and Electronics Systems (ICCES), IEEE, 2016, p. 1-6	2016	CIEEE			19.5.2017
10	Martens M., Kuipers F., Van Mieghem P.: Symbolic Regression on Network Properties. In Proc. of European Conference on Genetic Programming (EuroGP), LNCS 10196, Springer, 2017, p. 131-146	2017	LNCS			19.5.2017
11	Jiang H., Liu C., Liu L., Lombardi F., Han J.: A Review, Classification and Comparative Evaluation of Approximate Arithmetic Circuits. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , Vol. V, No N, 2017, p. TBD	2017	JIF			19.5.2017
12	Qiqieh I., Shafik R., Tarawneh G., Sokolov D., Yakovlev A.: Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression. In Desing, Automation and Test in Europe (DATE), IEEE, 2017, p. 1-6	2017	CIEEE			19.5.2017
	<b>Mrazek V., Vasicck Z., Skramna L.: Evolutionary approximation of software for embedded systems: median function. In: Genetic Improvement Workshop, GECCO 2015 Companion. ACM, 2015, p. 795-801</b>					<b>6</b>
1	Langdon W.B.: Genetic Improvement of Software for Multiple Objectives. In 7th International Symposium on Search Based Software Engineering 2015, LNCS 9275, 2015, p. 12–28, 2015	2015	LNCS			30.12.2015
2	Langdon W.B., Lam B.Y.H., Modat M., Petke J., Harman M.: Genetic Improvement of GPU Software. <i>Genetic Programming and Evolvable Hardware</i> , 2016 TBD	2016	JIF			28.7.2016
3	Petke J., Haraldsson S., Harman M., Langdon W., White D., Woodward J.: Genetic Improvement of Software: A Comprehensive Survey. <i>IEEE Transactions on Evolutionary Computation</i> , vol.PP, no.99, 2017, p.1-1	2017	JIF			19.5.2017
4	Langdon W.B., Veerapen N., Ochoa B.: Visualising the Search Landscape of the Triangle Program. In Proc. of European Conference on Genetic Programming (EuroGP), LNCS 10196, Springer, 2017, p. 96-113	2017	LNCS			19.5.2017

5	White D.R., Joffe L., Bowles E., Swan J.: Deep Parameter Tuning of Concurrent Divide and Conquer Algorithms in Akka. In EvoApplications 2017, Part II, LNCS 10200, Springer, 2017, p. 35–48	2017	LNCS			19.5.2017
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	<b>Vasicek Z., Sekanina L.: Circuit Approximation Using Single- and Multi-Objective Cartesian GP. In: 18th European Conference on Genetic Programming. LNCS 9025, Springer, 2015, p. 217-229</b>				1	
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1	Naseer A.A., Ashraf R.A., Dechev D., DeMara R. F.: Designing Energy-Efficient Approximate Adders using Parallel Genetic Algorithms. In SoutheastCon 2015, IEEE, 2015	2015	CIEEE			18.6.2015
2	Fathima B.A., Vasanthanayaki C.: Design and Implementation of Energy Efficient Approximate Multiplier. International Journal of Computer Applications (0975 – 8887)/National Conference on Information and Communication Technologies (NCICT 2015), 2016, p. 19-23	2016	C			1.12.2016
	<b>Hrbacek R., Sekanina L.: Towards highly optimized cartesian genetic programming: From sequential via SIMD and thread to massive parallel implementation. In Genetic and Evolutionary Computation Conference, 2014, p. 1015–1022</b>				2	
1	Ha S., Moon B.-R.: Fast Knowledge Discovery in Time Series with GPGPU on Genetic Programming. In Proceedings of the 2015 Annual Conference on Genetic and Evolutionary Computation, ACM, 2015, p. 1159-1166	2015	CACM			30.12.2015
2	Takamura S., Shimizu A.: Concurrent evolution of pixel predictor and context modeling for image coding. In 2016 IEEE International Conference on Image Processing (ICIP), Phoenix, AZ, USA, 2016, p. 2147-2151	2016	CIEEE			1.12.2016
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	<b>Salvador, R., Otero, A., Mora, J., De la Torre, E., Riesgo, T., Sekanina, L.: Self-Reconfigurable Evolvable Hardware System for Adaptive Image Processing. IEEE Transactions on Computers, Vol. 62, No. 8, 2013, p. 1481-1493</b>				17	
1	Chmaj G., Selvaraj H., Gewali L.: Tracker-Node Model for Energy Consumption in Reconfigurable Processing Systems. In Advances in Intelligent Systems and Computing, Volume 240, 2014, p. 503-512	2014	BCH			19.9.2013

2	Jaiswal V., Tiwari A.: A Survey of Image Segmentation based on Artificial Intelligence and Evolutionary Approach. IOSR Journal of Computer Engineering, Vol. 15, No. 3, 2013, p. 71-78	2013	J			26.6.2014
3	Oreifej R.S., Al-Haddad R., Ashraf R.A., DeMara R.F.: Sustainability Assurance Modeling for SRAM-based FPGA Evolutionary Self-Repair. In Proc. of Evolvable Systems: From Biology to Hardware SSCI-ICES 2014, IEEE, p. 17 - 22	2014	CIEEE			18.12.2014
4	Chen, N.-J., Feng, Z.-Y., Jiang, J.-H.: Bypass node non-redundant adding algorithm for crossing-level data transmission in two-dimension reconfigurable cell array. Journal on Communications, Vol. 36 (4), 2015, 17p	2015	J			18.6.2015
5	Chen, N., Jiang, J.: Considering communication-cost and hardware-fragment utilization cluster partitioning algorithm. Journal of Computer-Aided Design and Computer Graphics, Vol. 27(4), 2015, p. 754-763	2015	J			18.6.2015
6	Qu Y. R., Prasanna V. K.: High-performance and Dynamically Updatable Packet Classification Engine on FPGA. IEEE Transactions on Parallel and Distributed Systems, 27 (1), 2016, p. 197-209	2016	JIF	1		18.6.2015
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8	Ranjith C., S. P. Joy Vasantha Rani, Priyadharsheni B., Medhuna Suresh, Madhusudhanan M.: Optimizing GA operators for system evolution of evolvable embedded hardware on Virtex 6 FPGA. ARPN Journal of Engineering and Applied Sciences. Vol. 10, No. 11, 2015, p. 4908-4914	2015	J			30.12.2015
9	Haddow P.C.: Developmental Evolvable Hardware. In Trefzer M.A., Tyrrell A.M.(eds). Evolvable Hardware: From Practice to Application, Springer Verlag, 2015, p. 349-372	2015	BCH			30.12.2015
10	Yao R., Sun Y., He K., Yang Y.: Online Evolution of Image Filters Based on Dynamic Partial Reconfiguration of FPGA. In 11th International Conference on Natural Computation, IEEE, 2015, p. 999-1005	2015	CIEEE			28.7.2016
11	Prasada Kumari K.C.: Self-Adaptive Image Processing Using Blind Image Quality Assessment Technique. Self-Adaptive Image Processing Using Blind Image Quality Assessment Technique. Perspectives in Science (2016) TBD	2016	J			28.7.2016
12	Wang H. and (Shawn) Blanton R.D.: Ensemble reduction via logic minimization. ACM Trans. Des. Autom. Electron. Syst. 21, 4, Article 67 (May 2016), 17 p.	2016	JIF			28.7.2016
13	Khatri S., Tiwari S., Rizvi N.Z.: Electronic Model of Human Brain using Verilog. International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), IEEE, 2016, p. 1-5	2016	CIEEE			28.7.2016
14	Soleymani S., Noore A.: Dynamically reconfigurable evolutionary multi-context robust cellular array design. Int. J. Circuits and Architecture Design, Vol. 2, No. 1, 2016, p. 1-12	2016	J			1.12.2016
15	Kamarujjaman Sk, Manali Mukherjee, Mausumi Maitra: FPGA-Based Re-Configurable Architecture for Window-Based Image Processing. In Multi-Core Computer Vision and Image Processing for Intelligent Applications (eds. S. Mohan, V. Vani), IGI Global, 2016, p. 1-46	2016	BCH			1.12.2016

16	Almeida M. A., Pedrino E. C., Nicoletti M. C.: A Genetically Programmable Hybrid Virtual Reconfigurable Architecture for Image Filtering Applications. In 29th SIBGRAPI Conference on Graphics, Patterns and Images (SIBGRAPI), IEEE, 2016, p. 152-157	2016	CIEEE			19.5.2017
17	Wang J., Huang C., Ran Q., Deng X., Chen Q.: AdaBoost-based ensemble learning of evolvable hardware for classification of DNA microarray data. Journal of Jiangsu University (Natural Science Edition), Vol. 38, No. 1, 2017, p. 86-92, 102	2017	J			19.5.2017
	<b>Sekanina, L., Vasicek, Z.: Approximate Circuit Design by Means of Evolvable Hardware. In: 2013 IEEE International Conference on Evolvable Systems (SSCI-ICES), IEEE CS, 2013, p. 21-28</b>					<b>6</b>
1	Man, Menghua, Liu, Shanghe, Chang, Xiaolong et al.: The Biological Property of Synthetic Evolved Digital Circuits with ESD Immunity - Redundancy or Degeneracy?. Journal of Bionic Engineering, Vol. 10, No. 3, 2013, p. 396-403	2013	JIF	1		19.9.2013
2	Oreifej R.S., Al-Haddad R., Ashraf R.A., DeMara R.F.: Sustainability Assurance Modeling for SRAM-based FPGA Evolutionary Self-Repair. In Proc. of Evolvable Systems: From Biology to Hardware SSCI-ICES 2014, IEEE, p. 17 - 22	2014	CIEEE			18.6.2014
3	Tao Y., Zhang Q., Zhang L., Zhang Y.: A systematic EHW approach to the evolutionary design of sequential circuits. Soft Computing, Vol. 20, No. 12, 2016, p. 5025-5038	2016	JIF			30.12.2015
4	Bao, Z.-G., Wan, J.-L., Ma, X.-F: Optimization design of fault-tolerant image filter based on genetic algorithm. Journal of Shanghai Jiaotong University, Vol. 49, No. 8, 2015, p. 1181-1185	2015	J			30.12.2015
5	Almeida M. A., Pedrino E. C., Nicoletti M. C.: A Genetically Programmable Hybrid Virtual Reconfigurable Architecture for Image Filtering Applications. In 29th SIBGRAPI Conference on Graphics, Patterns and Images (SIBGRAPI), IEEE, 2016, p. 152-157	2016	CIEEE			19.5.2017
6	Babu K.S., Balaji N.: Approximation of Digital Circuits Using Cartesian Genetic Programming. In International Conference on Communication and Electronics Systems (ICES), IEEE, 2016, p. 1-6	2016	CIEEE			19.5.2017
	<b>Dobai R., Sekanina L.. Towards Evolvable Systems Based on the Xilinx Zynq Platform. In: 2013 IEEE International Conference on Evolvable Systems (SSCI-ICES), IEEE CS, 2013, p. 89-95</b>					<b>22</b>
1	Magdaleno, E., Rodríguez, M., Pérez, F., Hernández, D., García, E.: A FPGA embedded web server for remote monitoring and control of smart sensors networks. Sensors (Switzerland), Vol. 14, No. 1, 2013, p. 416-430	2013	JIF	1		26.6.2014
2	van de Belt J., Sutton P.D., Doyle L.E.: Accelerating software radio: Iris on the Zynq SoC. Proceedings of 2013 IFIP/IEEE 21st International Conference on Very Large Scale Integration (VLSI-SoC), IEEE, 2013, p. 294-295	2013	CIEEE			26.6.2014
3	Glette K., Kaufmann P.: Lookup Table Partial Reconfiguration for an Evolvable Hardware Classifier System. In IEEE Congress on Evolutionary Computation, IEEE, 2014. p. 1706-1713	2014	CIEEE			26.6.2014
4	Sabouri P., Gholam Hosseini H., Collins J.: Border Detection of Melanoma Skin Lesions on a Single System on Chip (SoC). Journal of Computers, Vol. 25, No. 1, 2014, p. 1-7	2014	J			26.6.2014

5	Shaowu Pan, Shuxiang Guo, Liwei Shi, Yanlin He, Zhe Wang, Qiang Huang: A Spherical Robot based on all Programmable SoC and 3-D Printing. In Proc. of 2014 IEEE Int. Conf. on Mechatronics and Automation, China, IEEE, 2014, p. 150-155	2014	CIEEE			1.9.2014
6	Calderon H.: Next Generation of Smart Machines: a survey of enabling technologies. Ciencia y Cultura, Vol. 18, No. 32, 2014, p. 89-119	2014	J			1.9.2014
7	Ho N., Kaufmann P., Platzner M.: Towards Self-Adaptive Caches: a Run-Time Reconfigurable Multi-Core Infrastructure. In Proc. of Evolvable Systems: From Biology to Hardware SSCI-ICES 2014, IEEE, p. 31-37	2014	CIEEE			18.12.2014
8	Sawma J., Khatounian F., Ghosn R., Idkhajine L., Monmasson E.: Quasi-Continuous Real-Time Simulation of an RLE Load with a Current MPC Regulation. In 2015 Third International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE), IEEE, 2015, p. 289 - 294	2015	CIEEE			18.6.2015
9	Sawma J., Khatounian F., Monmasson E., Ghosn R., Idkhajine L.: Evaluation of the new generation of system-on-chip platforms for controlling electrical systems. In Proc. of 2015 IEEE International Conference on Industrial Technology (ICIT), IEEE, 2015, p. 1570 - 1575	2015	CIEEE			18.6.2015
10	Kryjak, T., Komorkiewicz, M., Gorgon, M.: Hardware-software implementation of vehicle detection and counting using virtual detection lines. In Proc. of Design and Architectures for Signal and Image Processing (DASIP), IEEE, 2014, p. 1-8	2014	CIEEE			18.6.2015
11	Abdelgawad H. M, Safar M., Wahba A. M.: High Level Synthesis of Canny Edge Detection Algorithm on Zynq Platform. Int. Journal of Computer, Control, Quantum and Information Engineering, Vol. 9, No. 1, 2015, p. 148-152	2015	J			18.6.2015
12	Elnokity O., Mahmoud I. I., Refai M.K., Farahat H.M.: Hardware implementation of virtual reconfigurable circuit for fault tolerant evolvable hardware system on FPGA. American Journal of Engineering and Technology Research, Vol. 15, No. 1, 2015, p. 183-190	2015	J			18.6.2015
13	Reddy T.T., Madhavi, B.K., Kishore, K.L.: Improved block based processing with dual partial reconfiguration memory approach. In 2015 International Conference on Communications and Signal Processing (ICCSP), IEEE, 2015, p. 327-331	2015	CIEEE			30.12.2015
14	Smith F., van den Berg A.E.: Hardware Genetic Algorithm Optimization by Critical Path Analysis using a Custom VLSI Architecture. South African Computer Journal, Vol. 56, 2015, p. 120-135	2015	J			30.12.2015
15	Trefzer M.A., Tyrrell A.M.: Devices and Architectures for Evolutionary Hardware. In Trefzer M.A., Tyrrell A.M.(eds). Evolvable Hardware: From Practice to Application, Springer Verlag, 2015, p. 27-87	2015	BCH			30.12.2015
16	Bao, Z.-G., Wan, J.-L., Ma, X.-F: Optimization design of fault-tolerant image filter based on genetic algorithm. Journal of Shanghai Jiaotong University, Vol. 49, No. 8, 2015, p. 1181-1185	2015	J			30.12.2015
17	Govindan P., Wang B., Ravi P., Saniie J.: Hardware and software architectures for computationally efficient three-dimensional ultrasonic data compression. IET Circuits Devices Syst., 2016, Vol. 10, No. 1, p. 54-61	2016	J			30.12.2015

18	Huang C. M., Yang C. C., Wu C.M., Chen C.Y., Cheng C. W., Liu Y.J.: A Dual-Core FPGA-Based Embedded System Development Platform. 2016 International Symposium on Computer, Consumer and Control (IS3C), Xi'an, 2016, p. 1026-1030	2016	CIEEE			1.12.2016
19	Bean A.: Improving memory access performance for irregular algorithms in heterogeneous CPU/FPGA systems. PhD Thesis, Imperial College of Science, Technology and Medicine, Department of Electrical and Electronic Engineering, 2016, p. 140	2016	PHD			1.12.2016
20	Makryniotis T., Dasygenis M.: Rapid Implementation of Embedded Systems using Xilinx Zynq Platform. In Proceedings of the SouthEast European Design Automation, Computer Engineering, Computer Networks and Social Media Conference (SEEDA-CECNSM '16). ACM, 2016, p. 1-5	2016	CACM			1.12.2016
21	Shaikh S., Pujari S.: Migration from Microcontroller to FPGA based SoPC Design. In International Conference on Automatic Control and Dynamic Optimization Techniques, IEEE, 2016, p. 129-134	2016	CIEEE			19.5.2017
22	Pan S.-W., Li X.-Q., Han J.: Zynq-7000 SoC-based portable uncooled infrared imaging system. Journal of Beijing Institute of Technology (English Edition), Vol. 25, No. 3, 2016, p. 435-440	2016	J			19.5.2017
	<b>Vasicek, Z., Bidlo, M., Sekanina, L.: Evolution of efficient real-time non-linear image filters for FPGAs. Soft Computing, Vol. 17, No. 11, 2013, p. 2163-2180</b>					<b>3</b>
1	Tao Y., Zhang Y., Huang W., Zheng J.: A multi-objective evolutionary approach for design of image filter at function level. Jisuanji Fuzhu Sheji Yu Tuxingxue Xuebao/Journal of Computer-Aided Design and Computer Graphics, Vol. 26, No. 9, 2014, p. 1487-1493	2014	J			18.12.2014
2	Ono, K., Hanada, Y.: Assembling bloat control strategies in genetic programming for image noise reduction. In Proc. of Intelligent Systems Design and Applications (ISDA), IEEE, 2014, p. 113-118	2014	CIEEE			18.12.2014
3	Liu M., Chen L., He J., Zhang P.: A novel evolutionary method of structure-diversified digital filter design and its experimental study. Soft Computing, 2017 TBD	2017	JIF			19.5.2017
	<b>Dobal R., Sekanina L.: Image Filter Evolution on the Xilinx Zynq Platform. In: Proceedings of the 2013 NASA/ESA Conference on Adaptive Hardware and Systems. IEEE Circuits and Systems Society, 2013, pp. 164-171</b>					<b>7</b>
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2	Thi Khanh Hong Nguyen. Low power architecture for fall detection system. PhD Thesis, Universite Nice Sophia Antipolis, 2015, p. 177	2015	PHD			28.7.2016
3	Kryjak T., Komorkiewicz M., Gorgon M.: Real-time hardware–software embedded vision system for ITS smart camera implemented in Zynq SoC. Journal of Real-Time Image Processing, 2016 TBD	2016	JIF	1		28.7.2016



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6	Gobel M., Elhossini A., Chi C., Alvarez-Mesa M., Juurlink B.: A Quantitative Analysis of the Memory Architecture of FPGA-SoCs. In 13th International Symposium on Applied Reconfigurable Computing, Springer, LNCS 10216, 2017, p. 241–252	2017	LNCS			19.5.2017
7	Picek S., Yang B., Rozic V., Vliegen J., Winderickx J., de Cnudde T., Mentens N.: PRNGs for masking applications and their mapping to evolvable hardware. In 15th International Conference on Smart Card Research and Advanced Applications, CARDIS, LNCS 10146, Springer, 2017, p. 209-227	2017	LNCS			19.5.2017
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	<b>Petrlik J., Sekanina L.: Multiobjective evolution of approximate multiple constant multipliers. In: IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems 2013. IEEE Computer Society, 2013, pp. 116-119</b>					<b>3</b>
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1	Seaton T., Miller J. F., Clarke T.: Semantic Bias in Program Coevolution. In: Proc. of the 16th European Conference on Genetic Programming, LNCS 7831, Springer, 2013, p. 193-204	2013	LNCS			6.6.2013
	<b>Sekanina L.: Evolvable hardware. In Handbook of Natural Computing, Berlin, Springer, 2012, p. 1657-1705</b>					<b>4</b>



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	Citations in 2010	90			
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	Citations in 2013	87			

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Citations in 2015	86			
Citations in 2016	93			
Citations in 2017	24			
<b>Citations total</b>	<b>1050</b>		<b>1051</b>	
<b>Citations discovered in ISI Web of Knowledge (self-citations removed)</b>			<b>313</b>	
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Sum		1050		