A Frequency Tunable Resonant Clock Distribution Scheme Using Bond-Wire Inductor

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Abstract— **In this paper, we propose a frequency control method for a resonant clock distribution scheme using a bond-wire inductor. The resonant clock distribution using the embedded planes in a package and an inductive load suppresses the clock source jitter and significantly reduces the clock skew by replacing the cascaded repeaters of a conventional on-chip clock distribution. The resonant frequency can be controlled by the inductance of the load and the size of cavity planes. We use a bond-wire inductor instead of a chip inductor for fine tuning of resonant frequency and reducing the parasitic capacitance of integration. We have successfully demonstrated a 1.35 GHz clock delivery network with the transmission line matrix model of the plane cavity and the lumped model of bond-wire inductor. The simulation results show that the source jitter is suppressed by the resonance effect and the skew is minimized and the frequency is controlled by the inductance of a bond wire.**

I. INTRODUCTION

In a high-speed synchronous digital system, it is critical to minimize timing uncertainties of the clock signal, because the clock signal has a significant role in providing a reference for data transmission and all circuit blocks. In order to distribute the clock signals to the entire digital chip, a global on-chip clock distribution is normally used and multiple cascaded repeaters should be inserted into the on-chip interconnections to overcome the loss and delay of the on-chip interconnections. However, the cascaded repeaters can be sources of significant jitter and skew problems affected by the power supply switching noise generated by the digital logic blocks [1], [2]. Furthermore, the latency goes up in an H-tree structure of on-chip clock distribution network (CDN) to match the length of the clock source to every destination. A hybrid clock distribution scheme is proposed using a package substrate, which provides less resistance and capacitance of interconnections than those of on-chip interconnects [3]. The hybrid clock distribution scheme is able to remove the effect of simultaneous switching noise (SSN) on the clock signal delivery through interconnects of package layers. However if the clock source signal has an amount of jitter, distributed signals have also a lot of jitter.

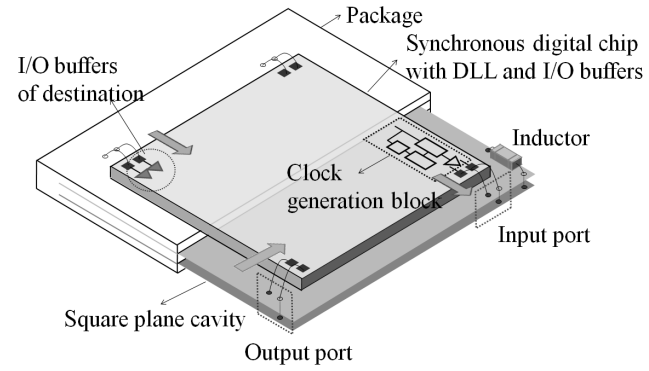
The resonant clock distribution technique is also proposed, which uses an off-chip standing wave resonator for on-chip clock distribution[4]. A plane cavity resonator consists of a package plane and an inductive load. The resonant clock frequency is varied by the size of the plane cavity and the inductance of the inductive load. Although off-chip inductors have high quality factors, the reduced board level complexity is evident in a direct reduction of associated costs. As an alternative to off-chip inductors, some radio frequency integrated circuits have utilized bonding wires as inductors [5].

In this paper, we propose a quarter-circle shaped plane resonator with a bond wire inductor as a resonant CDN. Low jitter and low skew clocking is achieved by resonator filter, and desired clock frequency is adjusted by a bond wire inductor. We successfully demonstrate time-domain and frequency-domain simulation results including the excitation circuits and the package plane modelled by a transmission line matrix (TLM) method [6].

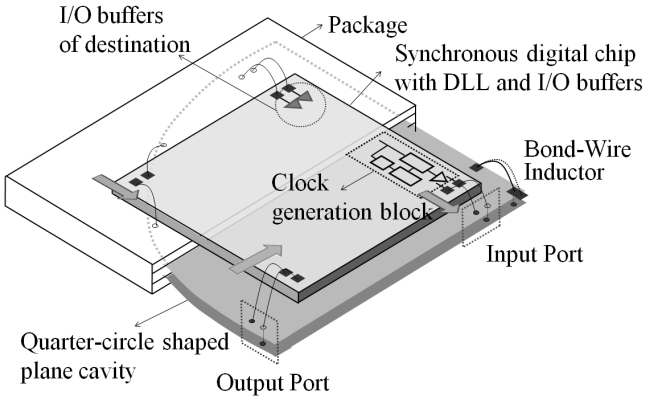
II. PROPOSED FREQUENCY TUNABLE RESONANT CDN USING QUARTER-CIRCLE SHAPED PLANE CAVITY RESONATOR

Fig. 1(a) shows the square plane cavity resonator with an off-chip inductor, which is utilized clock distribution network scheme. The differential clock signals which are generated from voltage-controlled oscillator (VCO) are converted into sine wave signals by a harmonic rejection mixer (HRM) output driver [7]. The single frequency sine wave through HRM driver excites the resonator and distributes through a plane cavity. The proposed quarter-circle shaped plane cavity resonator as a CDN is shown in Fig. 1(b). In a plane cavity resonator, a standing wave has the same phase in the whole plane, however the amplitude is different with the position of the plane. The different amplitude of the standing wave makes the clock signal skew, which is related to the length from the incident point of the signal to the destination point. In the square plane resonator a diagonal corner from the incident point has a relative long distance, and so it can be a source of clock skew of CDN. The quarter-circle shaped plane cavity resonator can compensate the mismatch of the length.

The resonant clock frequency just decided by the plane size and an inductive load is hard to control. An inductive load works as the extension of the plane, so the resonant frequency is decreased comparing to the short-ended parallel plane. In the case of an off-chip inductor, an 1nH inductor has a tolerance about 0.2nH, and this varies the resonance frequency by about 50MHz around 1GHz. If we use the bond-wire inductor instead of an off-chip inductor, comfortable integration is possible with lower parasitics and is tunable by the length of bond-wire inductor or the turns of solenoid bond wire.



(a)



(b)

Fig. 1. Schematic view of (a) the previous square plane cavity resonator for clock distribution [4], (b) the proposed quarter-circle shaped plane cavity resonator using bonding wire inductor. The proposed scheme has a bond-wire inductor for tuning resonance frequency of plane cavity.

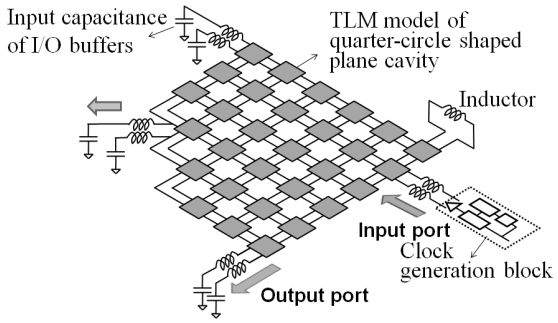
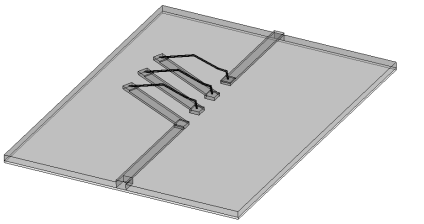


Fig. 2. Simulation model of quarter-circle shaped pane cavity resonator and bond-wire inductor. Input capacitance of I/O buffer and clock generation block are also included.



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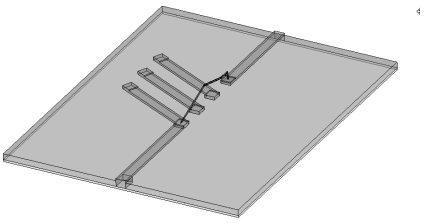


(b)

Fig. 3. The 3-D simulation model of bond wire inductor (a) solenoidal loop type with 3 turns, (b) minimum bond wire inductance for a given solenoidal type structure. The inductance of (a) is 4.3nH and (b) has 2.3nH. The summed length of three-turn bond wire of a solenoid inductor is about 4.5 mm, and that of directly connected bond wire is about 1.7 mm and the diameter of bond-wire is 1mil.

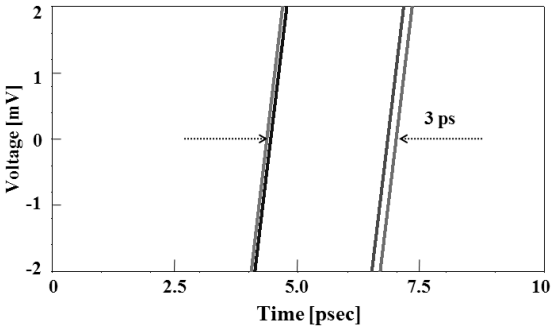
Fig. 2 shows the whole model of the CDN using package plane resonance. On-chip circuits and the inductive load are located in the right-top corner of the plane. TLM model is used for a plane cavity and bond wires are modelled as inductors and input capacitance of local buffers is also included. Square plane and quarter-circle plane cavity are compared in the view of skew.

The inductance of a bond-wire inductor varies with the length of a bond wire and the rule of thumb indicates 1nH per 1mm. If we need a bond wire as an off-chip inductor of 4nH, about 4mm bond wire should be used, however it is hard to integrate and control the length. Fig. 3(a) shows the solenoidal loop type bond-wire inductor with three turns. We can use the maximum length of bond wire as described in Fig. 3(b). The inductance of solenoid bond wire varies from 2.3nH to 4.3nH.

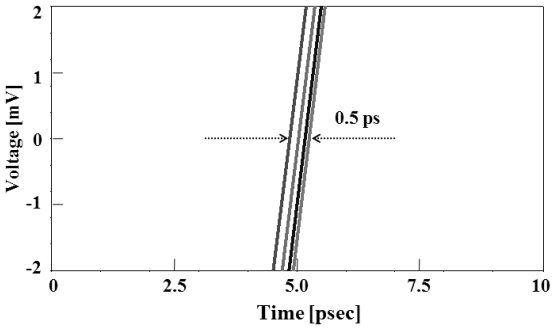
III. Verification of the Proposed CDN

Time-domain differential clock signals at all output ports are compared and the simulated skew is measured in Fig. 4. Although the VCO generates square wave, the source clock is almost sinusoidal due to the HRM output driver. The target frequency of the clock source is controlled by VCO control voltage and resonant frequency of the plane resonator is controlled by the loaded inductance. The resonant frequency of the radius 10mm quarter-circle plane with 1nH inductance is 1.37 GHz. Time domain simulation is performed with clock cycle time 741ps. In the case of square plane resonator the skew of output ports is 3ps. The clock signal at the diagonal corner of the input port has a delay, which causes the skew. The length from the input port to diagonal output port is larger than the other ports. The additional length has additional phase delay and different standing wave amplitude. Quarter-circle plane resonator can reduce the mismatch of the length between input port and output ports. The skew is reduced from 3ps to 0.5ps with a quarter-circle plane resonator as shown in Fig. 4(b).

The tunable resonance frequency is simulated with varying the inductance of the bond wire. Fig. 4(a) describes the self impedance at the input port of a plane cavity. Without inductor there is no series resonance in the plane cavity less than 3GHz, however, with inductance the additional resonance occurs. The inductive load acts like the extension of



(a)



(b)

Fig. 4.Simulated time-domain clock signal at the output ports (a) skew of square plane resonator, (b) skew of quarter-circle shaped plane resonator

the plane cavity, and so the resonance frequency reduces as the inductance of bond wire increases as shown at Fig. 4(b).

IV. CONCLUSIONS

We have described a CDN using plane cavity resonance. A skew-free clock distribution is possible with a quarter-circle plane resonator. The skew improvement due to a quarter-circle plane resonator was verified with chip-package hybrid simulation. The resonant frequency of the resonator is tunable with an inductive load. A bond-wire inductor is used as the inductive load, and the solenoidal loop type bond wire varies the inductance with comfortable integration.

ACKNOWLEDGMENT

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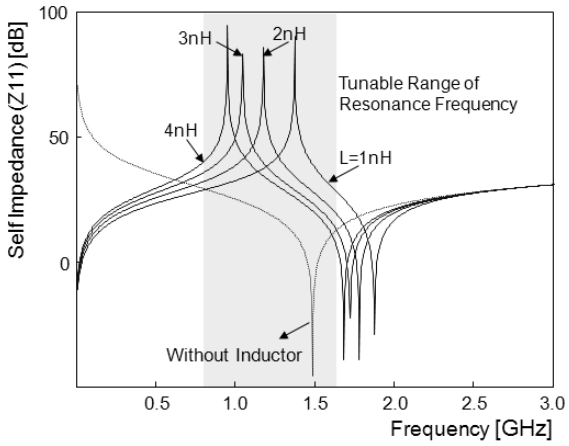

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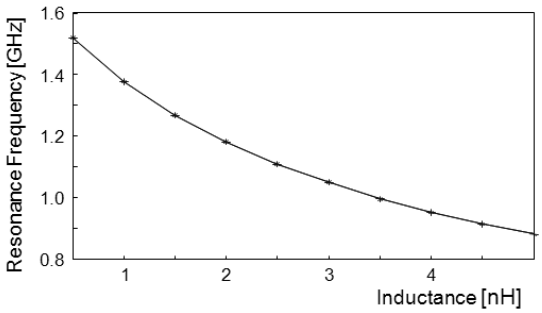

Fig. 5. (a) Self impedance monitored at the input port of a plane cavity resonator, (b) the resonance frequency with varying the inductance of impedance load. The resonance frequency reduces as the inductance increases.

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