Survey of Low-Power Testing of VLSI Circuits

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The author reviews low-power testing techniques for VLSI circuits. He prefaces this with a discussion of power consumption that gives reasons for and consequences of increased power during test. The article ends with a discussion of the opportunity to use such techniques in varying situations.

THE SYSTEM-ON-A-CHIP (SoC) revolution challenges both design and test engineers, especially in the area of power dissipation. Generally, a circuit or system consumes more power in test mode than in normal mode. This extra power consumption can give rise to severe hazards in circuit reliability or, in some cases, can provoke instant circuit damage. Moreover, it can create problems such as increased product cost, difficulty in performance verification, reduced autonomy of portable systems, and decrease of overall yield. Low power dissipation during test application is becoming increasingly important in today's VLSI systems design and is a major goal in the future development of VLSI design.

The challenge to test

Modern chip design has greatly advanced with recent silicon manufacturing technology improvements that escalate transistor counts, increasing a chip's complexity while maintaining its size. This phenomenon will continue, resulting in at least 10 of today's microprocessors fitting onto a single chip by 2005.[1] Consequently, design and test of complex digital circuits imposes extreme challenges to current tools and methodologies. VLSI circuit designers are excited by the prospect of addressing these challenges efficiently, but these challenges are becoming increasingly hard to overcome.

Test currently ranks among the most expensive and problematic aspects in a circuit design cycle, revealing the ceaseless need for innovative, test-related solutions. As a result, researchers have developed several techniques that enhance a design's testability through DFT modifications and improve the test generation and application processes. Traditionally, test engineers evaluated these techniques according to various parameters: area overhead, fault coverage, test application time, test development effort, and so forth. But now, the recent development of complex, high-performance, low-power devices implemented in deep-submicron technologies creates a new class of more sophisticated electronic products, such as laptops, cellular telephones, audio- and video-based multimedia products, energy-efficient desktops, and so forth. This new class of systems makes power management a critical parameter that test engineers cannot ignore during test development.[2]

Test or DFT engineers find their main motivation in considering power consumption during test in a circuit's consumption of more power in test mode than during normal operation.[3-5] Zorian showed that the test power (the power consumed during test) could be twice as high as the power consumed during the normal mode.[3] Several reasons cause this increased power usage. First, test efficiency correlates with

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toggle rate; therefore, in the test mode the switching activity of all nodes is often several times higher than during normal operation. Second, test engineers use parallel testing in SoCs to reduce the test application time, which might result in excessive energy and power dissipation. Third, the DFT circuitry designed to reduce the test complexity is often idle during normal operation but might be intensively used in the test mode. Fourth, successive functional input vectors applied to a given circuit during system mode have a significant correlation. In contrast, the correlation between consecutive test patterns can be low.[6]

For example, in a signal-processing circuit for speech recognition, the input vectors behave predictably, with the least-significant bits more likely to change than the most-significant bits. Similarly, in high-speed circuits that process digital audio and video signals, the inputs to most of those modules change relatively slowly. In fact, designers of low-power circuits take advantage of this consistent behavior when they determine a circuit's thermal and electrical limits, and system packaging requirements.

In contrast, there is no definite correlation between the successive test patterns generated by an automatic test-pattern generator for external testing or the patterns produced by a linear feedback shift register (LFSR) for built-in self-test (BIST). This lack of correlation can result in significantly greater switching activity in the circuit during test than during normal operation. Because power dissipation in CMOS circuits is proportional to switching activity, test's excessive switching activity can cause catastrophic problems, as detailed later.

Although academic research on low-power design remains nearly independent of that for test, industrial practice requires ad hoc solutions for considering power consumption during test application.[7] Practiced solutions include

- oversizing power supply, package, and cooling to withstand the increased current during testing (test engineers insert breaks into the test process to avoid hot spots);
- testing with reduced operating frequency; and
- system-under-test partitioning and appropriate test planning.

The first solution increases both hardware costs and test time. Although the second proposal uses less hardware, the reduced frequency increases test time and might lead to a loss of defect coverage because the reduced frequency can mask dynamic faults. Moreover, this solution reduces power consumption but lengthens test time, so it does not reduce the total energy consumed during test. The third solution of test partitioning and test planning detects dynamic faults, but increases hardware costs and test time.

To provide an adequate response to these industrial needs, various researchers have proposed solutions for power problems encountered during test. I classify these solutions into those applicable for external testing and those applicable for BIST. But first, test engineers and designers need to understand the qualities of power under test, as defined in the "Terminology" sidebar (next page) and the next two sections.

Energy and power modeling

Power consumption in CMOS circuits can be static or dynamic. Leakage current or other current drawn continuously from the power supply causes static power dissipation. Dynamic dissipation occurs during output switching because of short-circuit current, and charging and discharging of load capacitance. For existing CMOS technology, dynamic power is the dominant source of power consumption, although this might change for future high-scale integration.[8] The average energy consumed at node i per switching is $1/2\ C_i V_{DD}^2$, where C_i is the equivalent output capacitance, and V_{DD} is the power supply voltage.[9] Therefore, a good approximation of the energy consumed in a period is $1/2 C_i s_i V_{DD}^2$ where s_i is the number of switchings during the period. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, as a first approximation we assume capacitance C_i to be proportional to the fan-out of node F_i.[10] Therefore, an estimation of the energy E_i consumed at node i during one clock period is $E_i = 1/2\ s_1 F_i c_0 V_{DD}^2$, where c_0 is the circuit's minimum parasitic capacitance. According to this expression, estimating energy consumption at the logic level requires the calculation of fan-out F_i

Terminology

Test power is a possible major engineering problem in the future of SoC development.[1] As both the SoC designs and the deep-submicron geometry become prevalent, larger designs, tighter timing constraints, higher operating frequencies, and lower applied voltages all affect the power consumption systems of silicon devices. More precisely, these factors affect energy, average power, instantaneous power, and peak power, so I define these characteristics here.

- *Energy.* The total switching activity generated during test application, energy affects the battery lifetime during power up or periodic self-test of battery-operated devices.
- *Average power.* Average power is the total distribution of power over a time period. The ratio of energy to test time gives the average power. Elevated average power increases the thermal load that must be vented away from the device under test to prevent structural damage (hot spots) to the silicon, bonding wires, or package.
- *Instantaneous power.* Instantaneous power is the value of power consumed at any given instant. Usually, it is defined as the power consumed right after the application of a synchronizing clock signal. Elevated instantaneous power might overload the power distribution systems of the silicon or package, causing brown-out.
- *Peak power.* The highest power value at any given instant, peak power determines the component's thermal and electrical limits and system packaging requirements. If peak power exceeds a certain limit, designers can no longer guaranteee that the entire circuit will function correctly. In fact, the time window for defining peak power is related to the chip's thermal capacity, and forcing this window to one clock period is sometimes just a simplifying assumption. For example, consider a circuit that has a peak power consumption during only one cycle but consumes power within the chip's thermal capacity for all other cycles. In this case, the circuit is not damaged, because the energy consumed—which corresponds to the peak power consumption times one cycle—will not be enough to elevate the temperature over the chip's thermal capacity limit (unless the peak power consumption is far higher than normal). To damage the chip, high (not only highest) power consumption must last for several cycles.

Reference

1. B. Pouya and A. Crouch, "Optimization Trade-offs for Vector Volume and Test Power," *Proc. Int'l Test Conf.* (ITC 00), IEEE Press, Piscataway, N.J., 2000, pp. 873-881.

and the number of switchings on node i, s_i. Circuit topology defines the fan-out of the nodes, and a logic simulator can estimate the switchings (in a CMOS circuit, we calculate the number of switchings, including hazard switching, from the moment the input vector changes until the moment the internal nodes reach the new stable state). Product s_iF_i is called the weighted switching activity of node i and represents the only variable part in the energy consumed at node i during test application.

According to the previous formulation, the energy consumed in the circuit after application of successive input vectors (V_{k-1}, V_k) is $E_{Vk} = 1/2\ c_0 V_{DD}^2 \Sigma_i s(i,k) F_i$, where i ranges all the circuit's nodes and $s(i, k)$ is the number of switchings provoked by V_k at node i. Consider a pseudorandom test sequence of $Length_{test}$, the test length required to achieve the targeted fault coverage. The total energy consumed in the circuit during application of the complete test sequence is $E_{total} = 1/2\ c_0 V_{DD}^2 \Sigma_k \Sigma_i s(i,k) F_i$.

T will denote the clock period. By definition, the instantaneous power is the power consumed during one clock period. Therefore, we can express the instantaneous power consumed in the circuit after application of vectors (V_{k-1}, V_k) as $P_{inst}\ (V_k) = E_{vk}/T$.

The peak power consumption corresponds to the maximum instantaneous power consumed during the test session. It therefore corresponds to the highest energy consumed during one clock period, divided by T. More formally, we can express it as $P_{peak} = \max_k\ [P_{inst}\ (V_k)] = \max_k(E_{vk})/T$.

Finally, the average power consumed during the test session is the total energy divided by the test time $P_{ave} = E_{total}/[(Length_{test})T]$.

Note that this model for power and energy consumption is crude and simplified, but it suffices quite well for power analysis during test.

According to these expressions of power and energy consumption, and assuming a given CMOS technology and supply voltage for the circuit design, number of switchings s_i of a node i in the circuit is the only parameter that affects the energy, peak power, and average power consumption. Similarly, the clock frequency used during testing affects both the peak and average powers. Finally test length—the number of test patterns applied to the circuit under test (CUT)—affects only the total energy consumption. Consequently, when deriving a solution for power and energy mini-

mization during test, a designer or a test engineer has to keep these relationships in mind.

Problems induced by excessive test power

When dealing with high-density systems such as modern ASICs and SoCs, a nondestructive test must satisfy all the power constraints defined in the design phase. In addition to preventing destruction of the CUT, cost, reliability, autonomy, performance-verification, and yield-related issues motivate power consumption minimization during test.[5]

The cost constraints of consumer electronic products typically require plastic packages, which impose a tight limitation on power dissipation. Unfortunately, excessive switching activity during test leads to increased current flows in the CUT, making the use of expensive packages for the removal of excessive heat imperative. Moreover, electromigration causes the erosion of conductors and subsequently leads to circuit failure.[11] Because temperature and current density are major factors that determine electromigration rate, elevated temperature and current density (caused by the test's excessive switching) severely decrease CUT reliability. This phenomenon is even more severe in circuits equipped with BIST because such circuits might be tested frequently in, for example, online BIST strategies.

Not only the reliability but also the autonomy of battery-powered remote and portable systems suffers from increased activity. Remote system operation occurs mostly in standby mode with almost no power consumption, interrupted by periodic self-tests. Hence, power savings during test mode directly prolong battery lifetime.

Two points emphasize the relevance of this power minimization problem. First, the current trend in circuit design toward circuit miniaturization (for portability, for example) prevents the use of special cooling equipment for removing excessive heat during test. Second, the growing use of at-speed testing for identifying slow chips no longer permits compensating for increased power dissipation by reducing test frequency. In the past, tests typically ran at lower rates than a circuit's normal clock rate, because they needed to cover only stuck-at faults. Now, aggressive timing makes it essential for tests to identify slow chips through delay testing, which manufacturers use to performance certify cores for use in SoC designs.[12]

A circuit isn't as capable of dissipating power during test as it is in normal operation, a serious problem. During functional testing of the die just after wafer etching, the unpackaged bare die has very little provision for power or heat dissipation. During normal use, its packaging corresponds to the amount of required power dissipation, and sometimes has additional provisions like heat-dissipating fins. This lack of packaging prevents the use of traditional heat-removal techniques during bare-die testing. This might be a problem for applications based on multichip module technology, for example, in which designers cannot realize the potential advantages in circuit density and performance without access to fully tested bare dies.[13] If bare-die testing doesn't carefully control power dissipation, it can destroy the die under test, decreasing the overall yield and increasing product cost.

Problems in two other test areas motivate test power reduction. The first area is testing memories using wafer probes.[14] Wafer probing, with its poor power-supply connections, results in significant, high power and ground noise caused by high switching activity during testing. This excessive noise can erroneously change the logic state of circuit lines, causing some good die to fail the test and thus leads to unnecessary yield loss.

The second area is BIST. Modern design and package technologies make external testing increasingly difficult, and BIST has emerged as a promising solution to the VLSI testing problem. BIST is a DFT methodology aimed at detecting faulty components in a system by incorporating test logic on chip. BIST is well known for its numerous advantages such as improved testability, at-clock-speed test of modules, reduced need for ATE, and support during system maintenance.[4] Moreover, with the emergence of core-based SoC designs, BIST represents one of the most favorable testing methods because it allows preservation of a design's intellectual property.[15] In BIST, an LFSR, with its compact

size and ability to operate as a signature analyzer, usually generates test patterns.

Unfortunately, LFSR-generated tests tend to take longer to reach acceptable levels of fault coverage, which increases the total energy consumption. Increasing energy consumption reduces the autonomy of portable equipment, mainly in applications that apply periodic tests. Also, test vectors applied at nominal operating frequency will have a higher average power dissipation than normal mode. This is because in normal mode, successive functional input vectors applied to a given circuit have significant correlation; the consecutive vectors of an LFSR-generated test sequence have a lower correlation.[6] This would force the use of special packages and cooling systems to keep the thermal conditions under specifications, thus increasing final product cost. So to satisfy cost, performance verification, autonomy, and reliability constraints, it is important to reduce the power and energy dissipation during testing.

Another point concerns scan-based BIST. Scan-based, self-test architectures are popular because of their low impact on performance and area.[16] But these scan-based architectures are expensive because each test pattern requires a power-consuming shift operation to provide test patterns and evaluate test response. This phenomenon is well known in industry. To meet specified power limits during test and avoid system destruction, it is really important to reduce power dissipation during scan shifting.

Low-power external testing techniques

The literature offers several technique categories to ensure nondestructive external testing of a design with an ATE.

Low power ATPG algorithms

The first category consists of automatic test-pattern generation (ATPG) techniques, in which authors propose new automatic test-pattern generators with the intent of generating test patterns able to reduce the test power in addition to meeting classic ATPG objectives. Wang and Gupta[17] propose a new version of the path-oriented, decision-making (Podem) algorithm where the clever assignment of *don't-care* bits minimizes the number of transitions that occur in the CUT between two consecutive test vectors. The tests generated by the proposed combinational ATPG algorithm decrease both the average and peak power dissipated during test application. Wang and Gupta adapt their approach for full-scan, sequential circuits and the proposed ATPG minimizes switching activity by exploiting all don't cares that occur during scan shifting, test application, and response capture.[18]

Corno et al. presented another ATPG technique that reduces the test power of full, sequential circuits.[19] The proposed approach exploits the redundancy introduced during test pattern generation via *fault dropping*, in which the algorithm eliminates a fault from the fault list only if at least M sequences cover it. M is the redundancy factor. This process selects a sequence subset that reduces the power consumed without reducing fault coverage. Experiments based on International Symposium on Circuits and Systems (ISCAS) benchmarks showed that these subsets did maintain fault coverage and used from 45% to 86% less power than the original sequences (the ones that ignored heat dissipation).

Ordering techniques

The second category consists of ordering techniques that reduce the switching activity by modifying the order in which testers apply test vectors to the CUT. These techniques, though normally used in external testing, can also be used in deterministic BIST. In the work by Chakravarty and Dabholkar, the authors construct a complete directed graph in which each vertex represents a test vector and each edge represents the number of transitions activated in the circuit after application of the vector pair.[20] Next, the authors use a greedy algorithm to find a Hamiltonian path of minimum cost in the graph. With number of test vectors n, the graph's construction requires $n(n-1)$ logic/timing simulations of the circuit to compute the number of transitions on each edge. This might be a problem when testing circuits that require many test patterns to ensure high fault coverage. To solve this problem, Girard et al. propose using the Hamming distance between test vectors rather than the number of transitions in the circuit to evaluate the switching activity produced in the

CUT by a given input test pair.[21] Using the Hamming distance makes it possible to apply test vector reordering to large VLSI designs.

In an improved version of this work, the authors propose reducing the internal switching activity by lowering the transition density at circuit inputs via test vector reordering.[22] By considering a circuit's structural characteristics during processing, this modified technique obtains better results in terms of average and peak power saved during external test application.

During scan testing performed with an ATE—as is the case for circuits designed with a scan path structure—DFT engineers can reduce the test power by modifying the order in which scan flip-flops are chained to form the shift register. Dabholkar et al. proposed two heuristics for scan-latch ordering: a random-ordering heuristic and a simulated-annealing algorithm.[23] Experimental results show that scan-latch ordering can reduce test power by 10% to 25%. Bonhomme et al. proposed another heuristic procedure that operates in two steps.[24] The first step determines the chaining of the scan cells to minimize the occurrence of transitions in the scan chain during shifting operations. The second step identifies the input and output scan cells of the scan chain to limit the propagation of transitions during scan operations. This proposed approach works for any conventional scan design and reduces test power up to 34%. In both of these techniques, the test sequence remains unmodified to preserve the initial fault coverage.

Input control

Huang and Lee's basic idea involves identifying an input control pattern for a full-scan circuit.[25] They then apply the pattern to the circuit's primary inputs during scan, thereby minimizing or eliminating switching activity in the combinational part of the circuit. Using this input control technique with existing vector- or latch-ordering techniques reduces the power consumption even more than these techniques used by themselves.

Vector compaction and data compression

Sankaralingam, Oruganti, and Touba propose a static compaction technique to minimize the scan vector power dissipation.[26] Carefully selecting the merging order of test cube pairs during static compaction reduces both average and peak power for the final test set. This technique is more effective than conventional static compaction techniques that randomly merge test cubes. The proposed approach is simple yet effective, and it is implementable in the conventional test vector generation flow used in industry today. Chandra and Chakrabarty propose a novel technique using test data compression for SoC testing that reduces both test data volume and scan power dissipation.[27] They use Golomb codes for compressing (encoding) the scan vectors of cores under test, which reduces both average and peak power consumption after decompression and application of the vectors to the cores.

Scan chain transformation

Whetzel's approach transforms conventional scan architecture into a scan path having a desired number of selectable, separate scan paths.[28] Each separate scan path is in turn filled with stimulus and emptied of response. The author adds an adaptor circuit to intercept the scan control output from the tester and translate it into separate scan control outputs to each new scan path. The proposed architecture maintains the test time, enables reuse of the conventional scan architecture's test patterns, and avoids decreasing the scan clock rate. Lee, Huang, and Chen propose an interleaving scan architecture based on adding delay buffers among the scan chains.[29] This scan architecture can significantly reduce peak power consumption, by up to 76%.

Clock scheme modification

Considering Pouya and Crouch's results,[30] which demonstrate that the test power's major contributor is the clock tree, two groups of authors propose novel techniques for lowering test power in scan circuits. Sankaralingam, Pouya, and Touba's technique uses full-scan circuits with multiple scan chains.[31] This technique depends on generating and ordering the test set so that some scan chains can have their clocks disabled for portions of the test set. Disabling the clock prevents flip-flops from transitioning and reduces test power in the CUT and in the clock tree. Bonhomme et al. present a second tech-

nique based on a gated-clock scheme for the scan path and the clock tree feeding the scan path.[32] This technique reduces the clock rate on the scan cells during shift operations without increasing the test time. Using such a modified clock scheme during scan operations lowers the transition density in the CUT, the scan path, and the clock tree feeding the scan path. This minimizes average and peak power, and energy consumption. Applying this technique offers numerous advantages in terms of fault coverage, test time, and area overhead.

Low-power BIST techniques

Various authors reported on techniques to cope with power problems during BIST. In the following, I categorize these techniques for low power BIST.

Test scheduling algorithms

Zorian presented the first technique, which consists of a distributed BIST control scheme that simplifies the BIST execution of complex ICs, especially during higher test activity levels.[3] This approach can schedule the execution of every BIST element to keep the power dissipation under specified limits. The technique reduces average power and consequently avoids temperature-related problems, thanks to an increase in test time. On the other hand, the total energy remains constant, so the system's autonomy does not increase. Chou, Saluja, and Agrawal follow a similar strategy to diminish the average power consumption.[33] Iyengar and Chakrabarty propose an integrated framework to address several test scheduling problems for SoC designs.[34] They propose techniques that determine optimal SoC test schedules with precedence constraints as well as a new method for determining optimal power-constrained schedules in a reasonable computation time.

Low-power test pattern generators

Wang and Gupta propose a BIST strategy, called dual-speed LFSR, based on two different-speed LFSRs.[6] Its objective is to decrease the circuit's overall internal activity by connecting inputs that have elevated transition densities to the slow-speed LFSR. This strategy significantly reduces average power and energy consumption without decreasing fault coverage. Corno et al. present another low-power test pattern generator.[35] They base the test pattern generation on cellular automata and design it to effectively reduce test power in combinational circuits while attaining high fault coverage. Test time and area overhead remain unaffected.

Girard et al. present another low-power test pattern generator based on a modified LFSR.[36] As in the work of Bonhomme et al., the proposed low-power BIST technique relies on a gated-clock scheme for the test pattern generator and the clock tree feeding it; this scheme reduces test power in the CUT, generator, and clock tree.[32] The technique achieves important test power savings with no penalty to circuit performance, fault coverage, test time, or design time.

Other authors propose two other low-power approaches for scan-based BIST. Zhang, Roy, and Bhawmik propose modifying the LFSR by adding weight sets to tune the pseudorandom vector's signal probabilities and thereby decrease energy consumption and increase fault coverage.[37] Wang and Gupta present a low-transition, random-pattern-generation technique to reduce signal activity in the scan chain.[38] In this technique, an LFSR generates equally probable random patterns. The authors also use a *k*-input AND gate and T-latch to generate a high correlation between neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power.

Gizopoulos et al. consider the problem of low-power BIST for data path architectures built around multiplier-accumulator pairs.[39] They propose two alternative architectures that depend on whether the goal is low energy or low power dissipation. Both proposed architectures are deterministic: The authors base both on modified binary counters, operating as Gray counters, that generate only one transition at a time. These architectures can achieve important energy and average power savings compared to conventional pseudorandom BIST.

Toggle suppression

Hertwig and Wunderlich proposed a low-power strategy for scan-based BIST architectures.[16] This technique modifies the scan-path structure's scan cells in such a way that CUT

inputs remain unchanged during a shift operation. This novel design for scan-path elements allows for energy savings that are from 70% to 90% of that for a standard, scan-based BIST architecture. At the same time, however, the technique increases the area overhead and may lead to performance degradation.

LFSR tuning

Girard et al. address the problem of energy minimization during test application for BIST-enabled circuits.[40] The main constraint is reducing energy consumption without modifying the stuck-at fault coverage. In this work, the authors first analyze the impact of an LFSR's polynomial and seed selection on the circuit's switching activity during test application. They determine that the polynomial selection does not influence energy consumption; the LFSR's seed selection is a more important parameter. Therefore, the authors propose a method based on a simulated-annealing algorithm to select an LFSR's seed and provide the lowest energy consumption.

Vector filtering BIST

Girard et al. propose a test-vector-inhibiting technique to filter out some nondetecting subsequences of a pseudorandom test set generated by an LFSR.[41] The authors use a decoding logic to store the first and last vectors of the nondetecting subsequences to be filtered. A D-type flip-flop, working in toggle mode, switches the enable/disable mode of the LFSR outputs to perform selective filtering. Manich et al. enhance this technique by extending the filtering action to all the nondetecting subsequences.[42] In this work, the key idea is unification of all the decoding logic modules. Energy and average power consumption savings can reach 90% for some benchmark circuits.

Gerstendörfer and Wunderlich exploit the same idea of filtering nondetecting patterns for scan-based BIST architectures.[43] These authors combine a pattern-filtering technique with Hertwig and Wunderlich's technique to avoid scan-path activity during scan shifting.[16] The proposed scan-based BIST architecture reduces test power by several orders of magnitude and is very low cost in terms of area and performance penalty.

Circuit partitioning

Girard et al. propose a novel low-power BIST strategy based on circuit partitioning.[44] This strategy partitions the original circuit into two structural subcircuits so that two different BIST sessions can successively test each subcircuit. Based on this strategy, DFT engineers partition the circuit and plan the test session to minimize the average and peak power consumption. Moreover, this strategy also reduces the total energy consumed during BIST because the test length required for the two subcircuits is not much more than that of the original circuit. The proposed strategy applies to either scan-based or parallel BIST with slight modification to conventional test pattern generator structures. Area overhead is very low and these is almost no penalty on circuit performance.

Low power RAM testing

Cheung and Gupta propose a methodology for low-power test of RAMs.[14] The authors base their strategy on RAM transition reduction by reordering the read and write accesses and the address counting scheme. These measures decrease the energy consumption and keep test time the same, so they also minimize the average power.

IT'S NOT EASY to select an effective low-power testing strategy, given the number and the diversity of available techniques; the ultimate selection depends on several parameters. Obviously, the first parameter is the implementation context. Whether the technique is for external testing, scan, scan BIST, or parallel BIST, each context will lead to completely different choices. For example, test engineers can use a test-vector-ordering technique during external or scan testing, but they cannot use it for pseudorandom BIST.

The second parameter concerns the way DFT engineers want to address test power minimization. Do they want to act on the test sequence or on the test architecture? In the first case, DFT engineers select test-vector-ordering or compaction techniques (for external or scan testing). In the second case, DFT engineers prefer techniques like those presented

by Whetsel; Sankaralingam, Pouya, and Touba; and Bonhomme.[28,31,32]

A third parameter is the possibility that a designer or test engineer will have to relax some of the classical test constraints when implementing such a low-power testing technique.

Actually, there are several relevant criteria to consider when selecting solutions for minimizing test power. Fault coverage and test time, among the main test constraints, must remain unaltered by the implemented technique. The area overhead from hardware modifications must be acceptably low, and the technique must maintain circuit performance. The effect on the design flow, and hence on the design time, must be small enough for the solution to be acceptable.

So, although these techniques all minimize test power, each has a different effect on the various criteria. Consequently, each individual designer or test engineer will select a different low-power testing technique, depending on the importance attached to a particular criteria for a given implementation. For example, in situations where test time is not a crucial test criterion, DFT engineers will use the test scheduling technique proposed by Zorian for test power reduction during BIST.[3] On the other hand, the techniques presented by Corno et al. and Girard et al. are preferable if test times must remain the same.[35,36]

In addition to the mentioned selection criteria, clock power—the power dissipated in the clock tree each time the clock makes a transition—is one of the most important points a DFT engineer must account for when selecting a solution for minimizing test power. Pouya and Crouch's results suggest that clock power is a significant component of the total power during test.[30] In some cases, it might dominate the logic power dissipated when logic gates in the circuit switch. For this reason, clock power design requires special care. This means that designers must make the clock tree as small as possible or disable clock signals as often as possible, as in traditional low-power systems. ■

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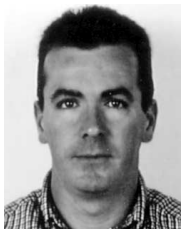

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