An Experimental Coin-Sized Radio for Extremely Low-Power WPAN (IEEE 802.15.4) Application at 2.4 GHz

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***Abstract*—An experimental 2.4-GHz CMOS radio composed of RF and digital circuits for the low-power and low-rate preliminary IEEE802.15.4 WPAN is reported, consuming 21 mW in receive mode and 30 mW in transmit mode. The RF design focus is to maximize linearity for a given power consumption using linearization methods which lead an order of magnitude improvement in LNA/mixer IIP3/power performance. Chip-on-PCB technology allows implementation of a coin-sized radio at very low cost, which also provides 3 dBi gain patch antenna and high Q (>50) inductors.**

***Index Terms*—2.4-GHz single-chip radio, chip on PCB, digital baseband, low-power RF CMOS transceiver, low-rate WPAN.**

I. Introduction

A NEW wireless communication with higher density of nodes and simple protocol is emerging for low-data-rate distributed sensor network applications such as those in home automation and industrial control. A low-power Bluetooth radio [1], [2] is standardized as IEEE802.15.1,[1] but it is relatively expensive and consumes too much power for this purpose. In 2000, IEEE started to standardize IEEE 802.15.4 exclusively for these kinds of low-rate wireless personal area network (LR-WPAN) applications.[2] In this paper, we report an experimental radio satisfying preliminary specification of this standard. The comparison of this radio and the draft standard of IEEE802.15.4 is shown in Table I.

The radio operates with variable data rate from 20 to 200 kb/s based on direct-sequence spread spectrum (DSSS) Gaussian minimum-shift keying (GMSK) modulation utilizing an 11-bit Barker code, which occupies eight channels with 3-MHz channel spacing in the 2.4-GHz industrial, scientific, and medical (ISM) band. DSSS not only helps easy timing recovery but also provides spectrum spreading required by Federal Communications Commission (FCC) regulations. The duty cycles between wake-up mode and sleep mode are programmable and can be chosen to less than 0.1% for more than one year battery life. It is assumed that the application spaces are for low latency devices.

Our first design focus is the implementation of an extremely low cost—less than 1 USD—radio system by as much monolithic integration as possible and then system packaging directly on printed circuit boards (PCB) using chip-on-board (COB) technology. The second is more emphasis on linearity/power rather than sensitivity. Since WPAN is to serve personal area space at the ISM band where lots of RF signals may exist, linearity is much more important than the sensitivity. Usually, linearity is proportional to power consumption; it is a great challenge to improve linearity at extremely low power consumption level. The third design focus is the maximum utilization of modern CMOS digital technology, which provides

TABLE I
IEEE802.15.4 Draft Standard Versus This Work

	IEEE 802.15.4	This work
Version	Draft standard (Motorola / Eaton / Philips, Nov. 2001)	Preliminary standard (Philips, Jan. 2001)
Frequency band	2.4GHz, 868/915MHz	2.4GHz
Transmit power	> 1mW	> 1mW
Data rate	250kbps	200kbps w/o ECC 66kbps(U) / 40kbps(D) w/ ECC
Data modulation	16–ary orthogonal (62.5kbaud)	~OQPSK(U) / ~CPFSK(D), (33kbaud(U) / 40kbaud(D))
Chip modulation	OQPSK, 32–chip PN sequence (2Mcps)	Precoded GMSK(U) / GMSK(D), 11–chip Barker code (2.2Mcps)
Error correction	Not specified	(3,1,7) convolutional codes(U) / 1/5 repetition codes(D)
Topology	Star, peer to peer	Star
Frame structure	Optional frame structure	Fixed, but with flexible length
Channel access	CSMA–CA (RSSI)	Simple CSMA–CA (RSSI)
Reliability	Fully handshaked	Fully handshaked (programmable)
Option	Guaranteed time slots	Periodic sleep (0.1% duty)

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[1][Online.] Available: http://www.bluetooth.com

[2][Online.] Available: http://grouper.ieee.org/groups/802/15/pub/TG4.html

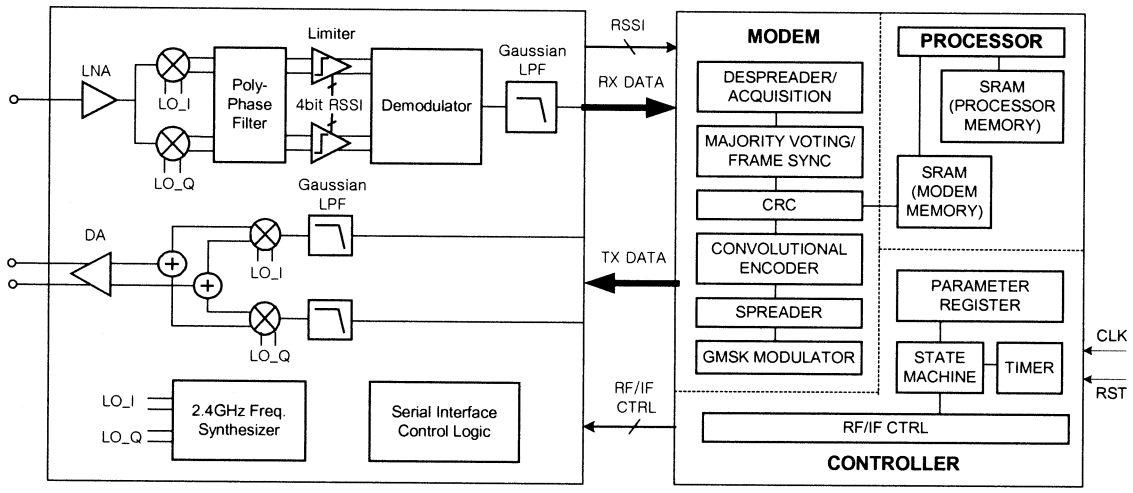

Fig. 1. Block diagram of the LR-WPAN radio and baseband chips.

programmability and digital trimming capability, as well as lower power consumption at lower frequency signal processing.

The physical (PHY) and media access control (MAC) functions have been implemented as a two-chip solution [3]. One chip consists mostly of RF circuits, and the other digital circuitry for the modem/processor as shown in Fig. 1. These ICs are fabricated using a 0.18-μm single-poly six-metal CMOS process that is provided especially for RF applications.

Section II describes the radio architecture, and the detailed circuit designs are discussed in Section III. Section IV presents the modem and MAC functions and their chip implementations. Section V reports system implementation results and Section VI concludes this paper.

II. Radio Architecture

Fig. 2 shows the architecture of a radio chip, which consists of a receiver, a transmitter, and a frequency synthesizer. The receiver adopts a low-IF architecture to have immunity against signal corruption by dc offset and $1/f$ noise. Note that a GMSK modulated signal with a time-bandwidth product BT of 0.5 has about 99% of information within 50% of its bandwidth. If the IF frequency is too low, the signal can be corrupted by $1/f$ noise, whereas too high an IF frequency results in higher power consumption in the IF block. An IF frequency of 4 MHz was chosen considering this tradeoff as well as the filtering requirement of the nearest channel signals, which are 3 MHz away from the channel of interest.

The signal is demodulated using a noncoherent detection technique that needs no carrier phase recovery and can easily be implemented in analog circuits using limiters and a discriminator. Although it gives 3-dB loss of signal-to-noise ratio (SNR) compared with coherent detection, this scheme provides enough sensitivity required by the standard. The 2.4-GHz RF signal is first amplified by a low-noise amplifier (LNA) and then downconverted to 4 MHz I/Q signals by two identical mixers driven by quadrature local-oscillator (LO) signals from a frequency synthesizer. At the first IF stage, channel selection, signal amplification, and image rejection are simultaneously performed by using a fifth-order active polyphase filter. The complex filter is designed to provide sufficient image rejection. Both the removal of external components, especially in RF frequency, and the high level of integration help to realize a low-cost and small-sized radio. Digital trimming aids to improve the filter characteristic and eventually contributes to the removal of the external filters. All nonideal circuit behaviors due to mismatches, including the frequency response characteristic of the filter, are tuned by digital trimming circuits, which are controlled through serial interface logic between radio and digital baseband chips. Instead of digital demodulation using analog-to-digital converters (ADCs), analog detection is performed using limiters, a discriminator, and a data slicer, providing 1-bit output. Frequency discrimination after hard limiting of the received signal is more power efficient than digital coherent detection for frequency-shift keying (FSK)-type modulation schemes such as GMSK, adopted for this radio. The output of each limiter outputs 1-bit received signal strength indication (RSSI) signal, which enables system-level power management monitoring of the channel condition and signal level.

The transmitter adopts a conventional direct I/Q modulation with up mixers. Baseband Barker-coded I/Q symbol signals are generated using a lookup-table-based GMSK modulator and digital-to-analog converters (DACs) followed by low-pass filters (LPFs). Note that the GMSK signal $(\mathrm{BT} = 0.5)$, which has an appreciable amount of intersymbol interference (ISI), is generated considering nearest neighboring bits, being chosen from eight signals stored in the ROM table. Two identical mixers upconvert the baseband quadrature signals directly to 2.4 GHz, which is combined by current summing at the output. Since GMSK modulation is a constant envelope modulation, a nonlinear drive amplifier with high efficiency can be used.

For generating 2.4-GHz LO signals with 3-MHz channel spacing, an integer-N frequency synthesizer derived from a 22-MHz crystal oscillator with ± 20 ppm accuracy is implemented. A 4.8-GHz LO signal is generated by a voltage-controlled oscillator (VCO) with a small area and high Q on-chip inductor. The 2.4-GHz LO I/Q signals are then generated by a divide-by-two circuit. The frequency synthesizer is designed in fully differential fashion, for immunity to the common-mode noise.

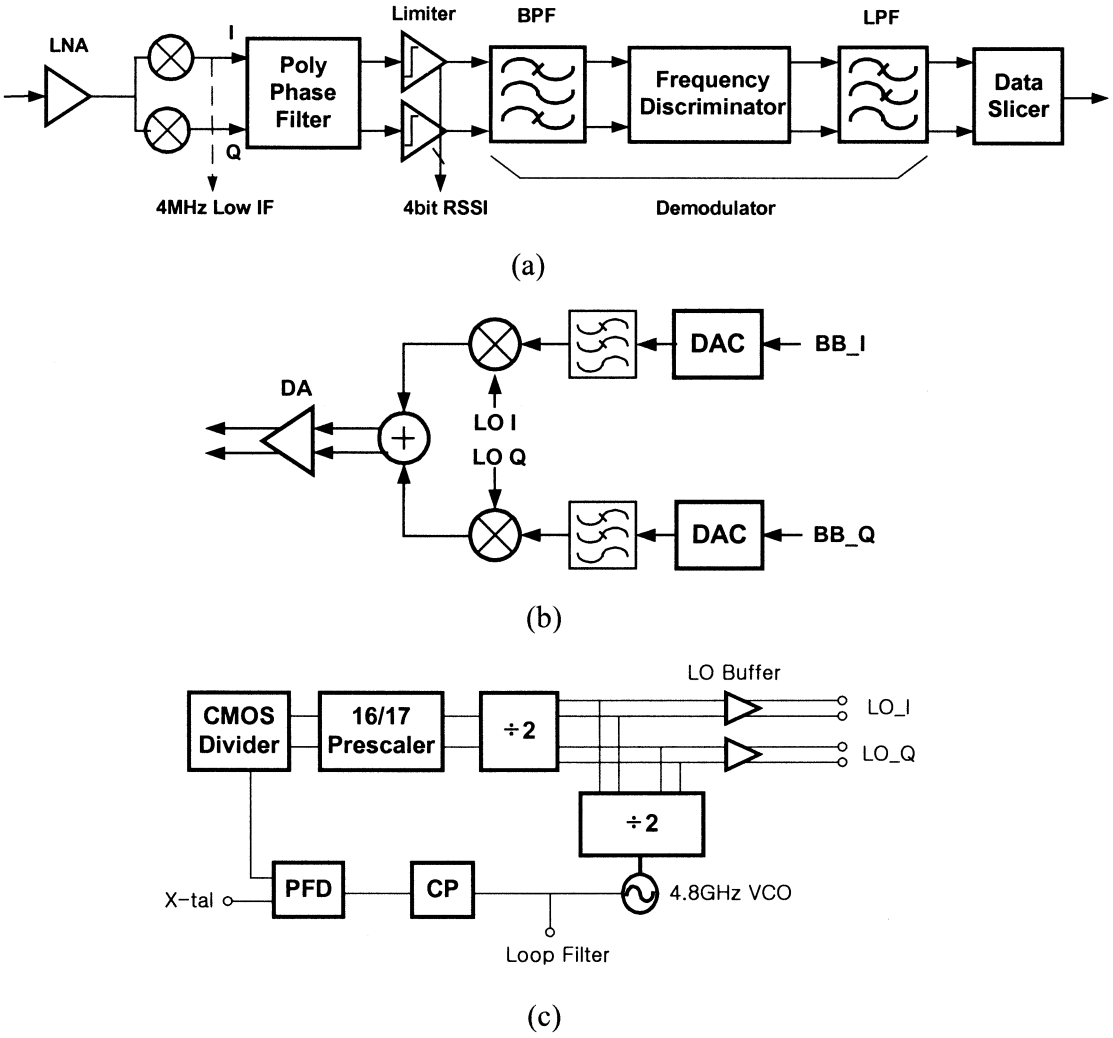

Fig. 2. The 2.4-GHz radio chip architecture. (a) Receiver. (b) Transmitter. (c) Frequency synthesizer.

III. RF Transceiver Design

RF transceiver design using 0.18-μm CMOS technology as well as PCBs are discussed in this section. The 0.18-μm CMOS devices and six metal layers with 2-μm-thick top metal provide high gain and good quality factor Q for on-chip inductors, resulting in low power consumption in RF/analog circuits. Off-chip PCB inductors are used when high Q and/or large inductance are necessary. Otherwise, we pursue as much on-chip integration as possible, because of better repeatability as well as less pin count.

A. Receiver

Fig. 3 shows the schematic of the front-end of the receiver. In the case of a low-IF structure, LO emission through antenna can be problematic. For this reason, the cascode structure is adopted for the LNA since it enhances the reverse isolation. The input noise and power matching is performed following a simple analytical design approach [4]. The size of the cascode transistor is smaller than that of the transconductor, which provides higher gain with little current consumption. The mixer adopts a folded structure and multiple gated transistor (MGTR) technique [5] in the transconductance stage, which gives an order of magnitude improvement in the third-order input intercept point (IIP3) for the same bias current. This linearization technique can effectively reduce g_m'' of the field-effect transistor (FET) by linearly superposing several common-source FET transistors with different bias and size in parallel. In a transconductor where g_m'' is linearized using the MGTR technique, however, we found that second harmonic mixing can still generate many third-order harmonic components, limiting IIP3 improvement [6]. Therefore, MGTR combined with second-harmonic termination was adopted for the mixer. It should be noted here that we have not tried to linearize the LNA, since the mixer's IIP3 dominates in the receiver front-end. Furthermore, the folded structure provides a large voltage headroom for low supply, resulting in additional improvement. The front-end gain can be chosen between high gain and low gain according to the received signal strength, providing 10-dB gain differences. The IIP3 for the RF front-end is 6 dBm at low-gain mode and -4 dBm at high-gain mode, respectively. This IIP3/power performance is an order of magnitude improvement compared with others as shown in [6]. The RF front-end provides up to 30-dB voltage gain with 3-mA current consumption at 1.8-V supply voltage.

To obtain both noise immunity and low power consumption concurrently, a single-ended LNA and single-balanced mixer

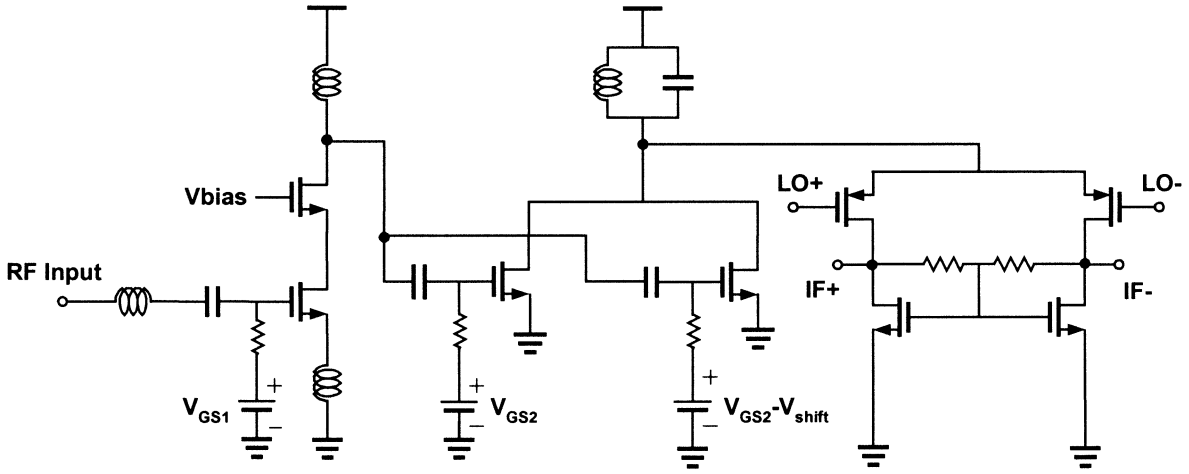

Fig. 3. Receiver front-end schematic. MGTR is adopted for the transconductor in the mixer.

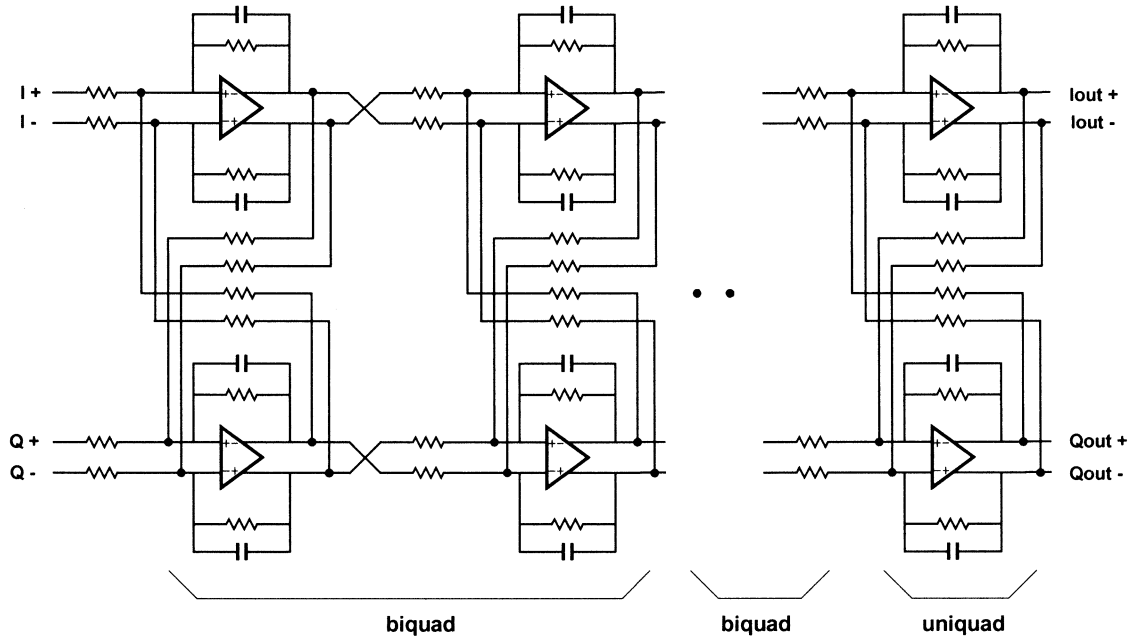

Fig. 4. Active polyphase filter schematic.

are adopted. The deep triple n-well is found to be very efficient for isolation. Utilizing the deep triple n-well technology, we succeeded in obtaining more than 60 dB of isolation [7].

Fig. 4 shows the schematic of a fifth-order active polyphase filter, which consists of two biquad filters with two poles each and one uniquad filter with one pole. The filter performs channel selection, signal amplification, and image rejection with complex signal processing. Here, the downconverted image signals are cancelled at the filter output. Layout should be done very carefully to minimize *R* and *C* mismatches which affect the performance of the filter. Nevertheless, the center frequency shows large variation over process, which is expected because it is determined by the absolute value, not by the ratio of capacitors and resistors. This is adjusted by digital trimming circuitry with a 5-bit switched capacitor array. Constant group delay within the signal bandwidth is another design parameter since the spread GMSK modulated signal has a bandwidth of 2.2 MHz. In the polyphase filter, 28-dB channel selection is achieved at 12.4-dB gain and more than 30-dBc image rejection is obtained. Fig. 5 shows the frequency response characteristic of the polyphase filter, whose center frequency is tuned by 5-bit digital codes.

The polyphase filter is followed by five stages of limiting amplifiers which saturate the signal for hard decision. A 4-bit RSSI is generated from the output of the limiters, as shown in Fig. 6, by using a quadruple rectifier and a comparator. Fig. 7 shows the schematic of the limiter circuit designed in differential amplifier with common-mode feedback (CMFB). R1, R2, and C1 determine the low-frequency limit of operation, while the high-frequency limit is determined by limiting devices and their parasitic capacitances. To be robust against the fluctuation in supply voltage, the $V_{\rm bias}$ for the limiter is also fed from the same replica of Fig. 7. Five limiting amplifiers saturate the input signal, generating the 1-V peak signal which is fed into the input of a frequency demodulator.

The demodulator is composed of a bandpass filter (BPF), differentiators, mixers, and a low-pass filter (LPF), as shown in

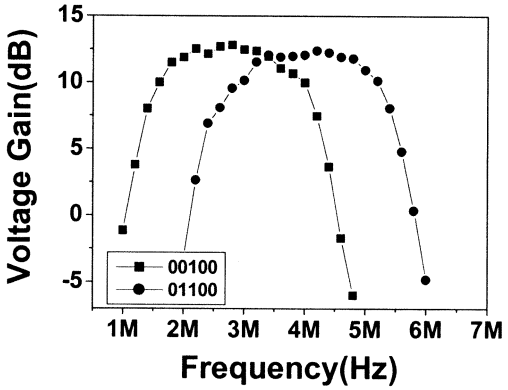

Fig. 5. Measured frequency characteristic for digitally trimmed polyphase filter. The binary number in the inset indicates the trimming code.

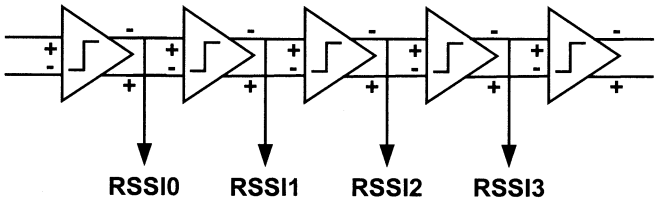

Fig. 6. Five-stage limiting amplifiers with 4-bit RSSI.

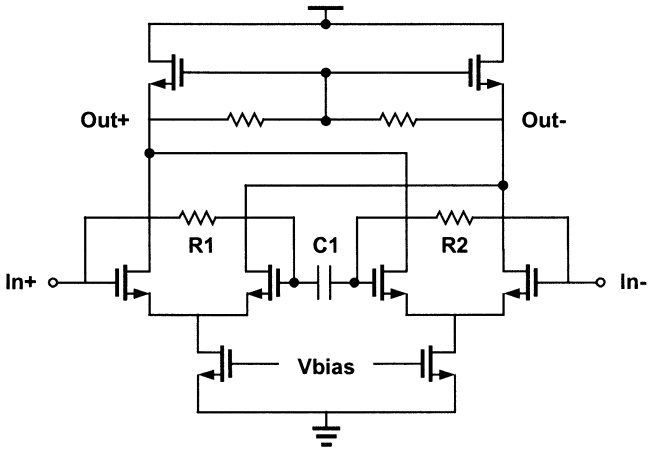

Fig. 7. Limiter schematic.

Fig. 8. First, the BPF removes the unwanted harmonics from the limiter output, and then the frequency deviation is measured using differentiators and mixers [8]. A Gaussian LPF is used to remove the spurious signals that originate from mismatches in the BPF and mixers. Fig. 9 shows the demodulator characteristic, which generates an analog baseband signal depending on the input frequency deviation. A data slicer is designed in the digital chip as a one-bit ADC. The total current consumption of the IF stage is 3.4 mA at 1.8-V supply voltage, composed of 1.4 mA for a polyphase filter, 0.5 mA for limiters, 1.1 mA for a demodulator, and 0.4 mA for a data slicer.

B. Transmitter

The DSSS GMSK modulated signal is generated by means of ROM-based digital signal synthesis and passes through the DACs and LPFs before upconversion in the mixers. An 8-bit

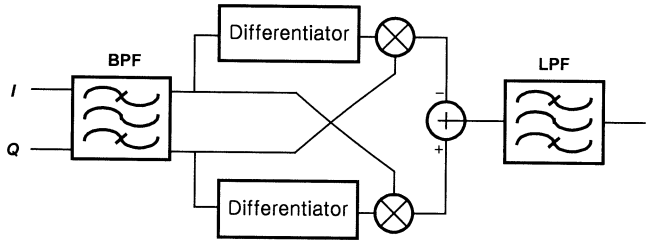

Fig. 8. Demodulator block diagram.

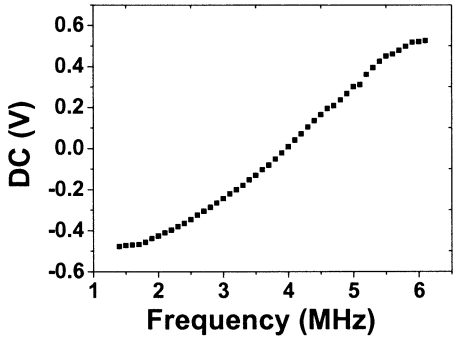

Fig. 9. Measured demodulator characteristic.

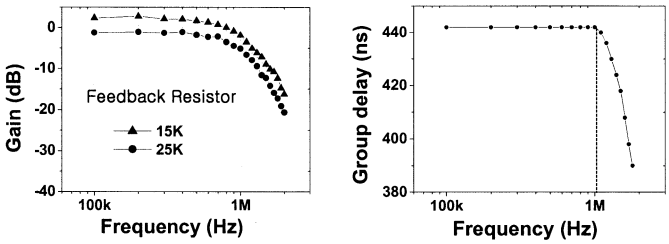

Fig. 10. Measured LPF gain and group delay characteristics. Feedback resistor changes the LPF gain.

current-steering DAC is designed in the digital chip to reduce the number of pins. The oversampling ratio is 8 $\times$ for the 1.1-MHz input signal. A fourth-order low-pass active filter is designed with constant group delay. Its gain is controlled digitally by switching the array of feedback resistors, which covers the gain control of entire transmitter chain. Fig. 10 shows the measured characteristics of a variable gain LPF with constant group delay.

Double-balanced I/Q mixers convert each baseband signal directly up to 2.4-GHz frequency and deliver -15 dBm differential signal to the input of a drive amplifier by current summing, as shown in Fig. 11. LO emission is due to differential mismatch in the mixer circuit and leakage of large LO signals, while spectrum regrowth is due to quadrature mismatch and nonlinearity of the mixer circuit. Layout is done very carefully to maintain symmetry for the differential and quadrature signals, which reduces both LO emission and spectrum regrowth. The adoption of the constant envelope modulation scheme allows an efficient drive amplifier consuming 8 mA at 0-dBm output power. As shown in Fig. 12, the drive amplifier includes a gain stage with on-chip load and a driving stage with off-chip output matching components, which operates as a class-C amplifier with 33% of drain efficiency.

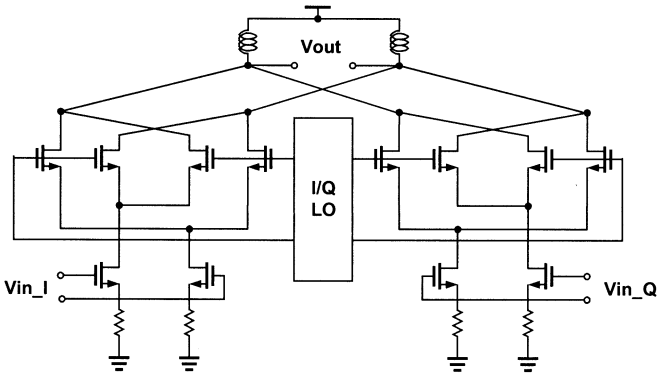

Fig. 11. Up-mixer schematic.

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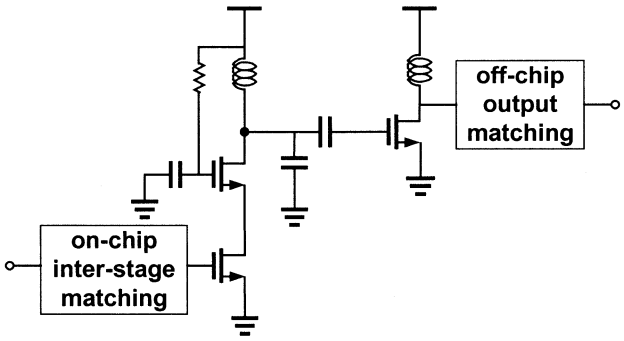

Fig. 12. Drive amplifier schematic (single path).

C. Frequency Synthesizer

An integer-N frequency synthesizer is designed because the channel separation is relatively large at 3 MHz. The 2.4-GHz differential I/Q LO signals are obtained by dividing differential signals from an integrated 4.8-GHz *LC* VCO. The entire divider chain is optimized from the viewpoint of low power consumption as well as low switching noise, resulting in the adoption of asynchronous current-mode-logic dividers at high frequencies and asynchronous static CMOS dividers at low frequencies, respectively. Furthermore, impedance matching between a 2.4-GHz output and the prescaler input is adopted, reducing the power consumption by half. Note that inductor loads are used in the 4.8-GHz divide-by-two circuit, allowing a large output voltage swing at 0.6-mA current consumption. This current level is about half compared with that adopting resistive loads.

In the VCO, pMOS and nMOS cross-coupled pairs are used for symmetry with a differential on-chip inductor in the tank circuit. The 2-bit capacitor array is switched for coarse tuning of oscillation frequency, leading to 12.5% tuning range. Fig. 13 shows the VCO tuning characteristic controlled by 2-bit digital codes.

The loop bandwidth for the phase-locked loop (PLL) is 20 kHz adjusted by external resistors and capacitors, with the settling time of the synthesizer less than 150 μs.

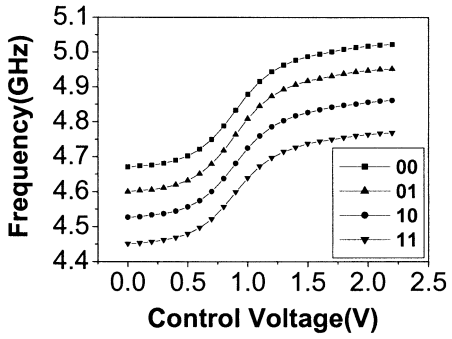

Fig. 13. Measured VCO tuning range. The binary number in inset indicates codes for coarse tuning.

TABLE II
FR-4 CHARACTERISTIC AS PCB SUBSTRATE

ε_r	4.5 ~ 4.9 (typ. 4.6)
tanδ	0.01
Metal thickness	15 ~ 30 μm
PCB thickness	0.8 ~ 3.0 mm

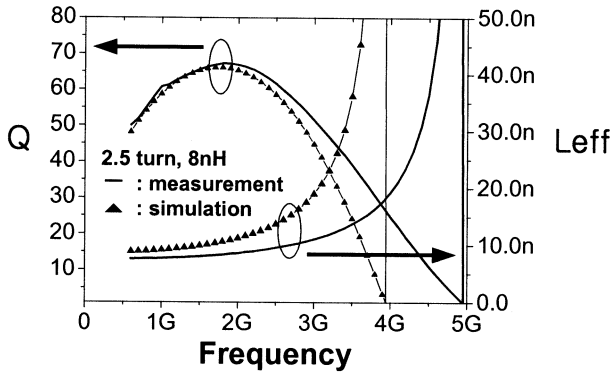

Fig. 14. Measured quality factor Q and effective inductance $L_{\rm eff}$ for a PCB inductor.

D. PCB Inductor and Antenna

CMOS on-chip inductors have two problems: large area consumption and low quality factor. Even if a very thick top metal layer is provided, the Q of on-chip inductors is hardly larger than 10 at 2.4 GHz in a 0.18-μm CMOS process. In RF applications, large inductors are often used for chokes and LNA input matching, which are usually supplied as external discrete components. As the pitch size of PCB technology scales down to about 100 μm, it becomes possible to implement high-quality inductors in a few millimeters square. Table II describes the characteristics of an FR-4 substrate. An 8-nH inductor with Q more than 50 is obtained within 3 mm $\times$ 3 mm, as shown in Fig. 14.

Implementing a small and cheap antenna in the 2.4-GHz transceiver is another delicate problem for low-data-rate WPAN applications. Using PCB technology, an inverted-F patch antenna [9]–[11] as small as 4.5 cm^2 is fabricated as shown in Fig. 15, providing 3-dBi gain and transmitter bandwidth ($<$ VSWR 1.5) of 120 MHz at 2.4 GHz. The 3-dB beam width is about 120°.

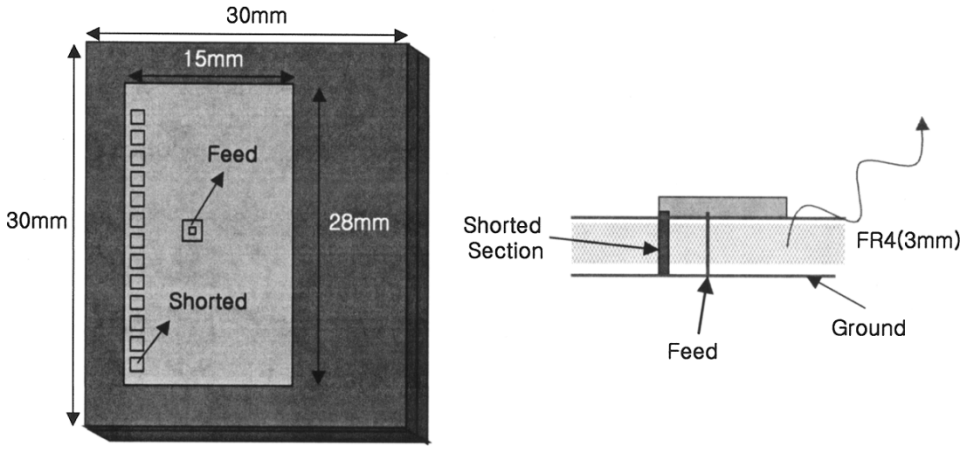

Fig. 15. Inverted-F patch antenna structure on PCB.

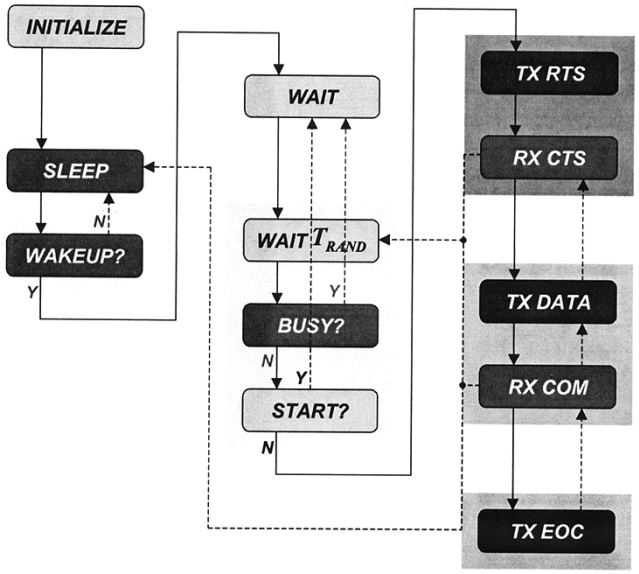

Fig. 16. Wireless connection procedure of designed LR-WPAN radio.

IV. Digital Modem/Processor Design

Fig. 16 shows the wireless connection procedure between node and base station. Once a controller is initialized, it alternates between Wakeup and Sleep modes at a programmable duty cycle. The duty cycle can be chosen less than 0.1% to extend battery life. When it receives a Wakeup frame from the base station, it leaves Sleep state, performing carrier sensing using RSSI, and determines whether it is allowed to communicate with the base station. When the channel is empty, it transmits the request-to-send (RTS) frame and then receives a clear-to-send (CTS) frame. Until the handshaking is completed, it should wait for the channel to be idle. Then it enters into the end-of-connection (EOC) state and transmits the EOC frame. The frame format chosen in this work is shown in Fig. 17. Cyclic-redundancy-check-16 (CRC-16) is used as error-detection coding.

The digital chip shown in Fig. 18 supports PHY functions including modulation, spreading and error-correction coding, MAC functions including simplified carrier sensing multiple access with collision avoidance (CSMA-CA), and system control functions such as power management. These functions are mostly designed asymmetrically for uplink and downlink so that a powerful base station lessens the complexity as well as the power consumption of the remote units. It consists of a modem, a processor, a controller, and memory.

The modem supports most of the PHY functions, which are characterized by DSSS GMSK with optional error-correction coding. While the transmitter part performs ROM-based GMSK modulation [12] that follows convolutional-coding and spreading, the receiver part simply performs despreading and majority voting for low complexity. The transmitter part supports the precoded GMSK (with BT equal to 0.5) combined with (3,1,7) convolutional coding in order to improve the sensitivity at the base station. Note that, assuming a coherent receiver, precoded GMSK yields almost the same error performance as precoded minimum-shift keying (MSK) or, more generally, offset quadrature phase-shift keying (OQPSK) [13]–[15], retaining most advantages of GMSK. For the purpose of timing synchronization, the PHY functions include code acquisition and frame synchronization.

The processor supports CSMA-CA in order to avoid collision with other WPAN nodes. With the help of glue logic, it performs core functions of p-persistent and/or nonpersistent CSMA-CA. The processor provides significant programmability for PHY and MAC functions through the assembly language for control of wireless connection process and programming of system parameters such as duty cycle.

Apart from this general-purpose processor, a controller that is a kind of application-specific processor supports occasional Wakeup operations. It can control the entire WPAN system, helping minimize the total power consumption by properly disabling unnecessary parts, resulting in system-level power management.

The size of the embedded SRAM is 3 kB and the operation clock frequency is 4.4 MHz.

V. System Implementation Results

A radio transceiver die micrograph, fabricated using 0.18-μm CMOS and six-metal-layer technology with thick top metal is

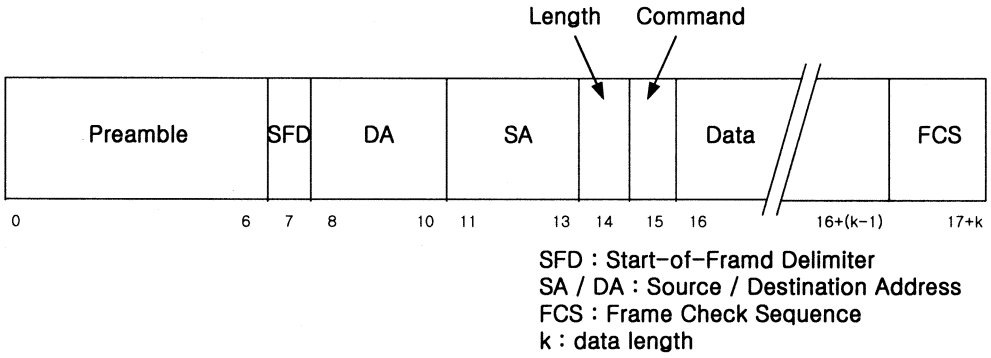

Fig. 17. Frame format.

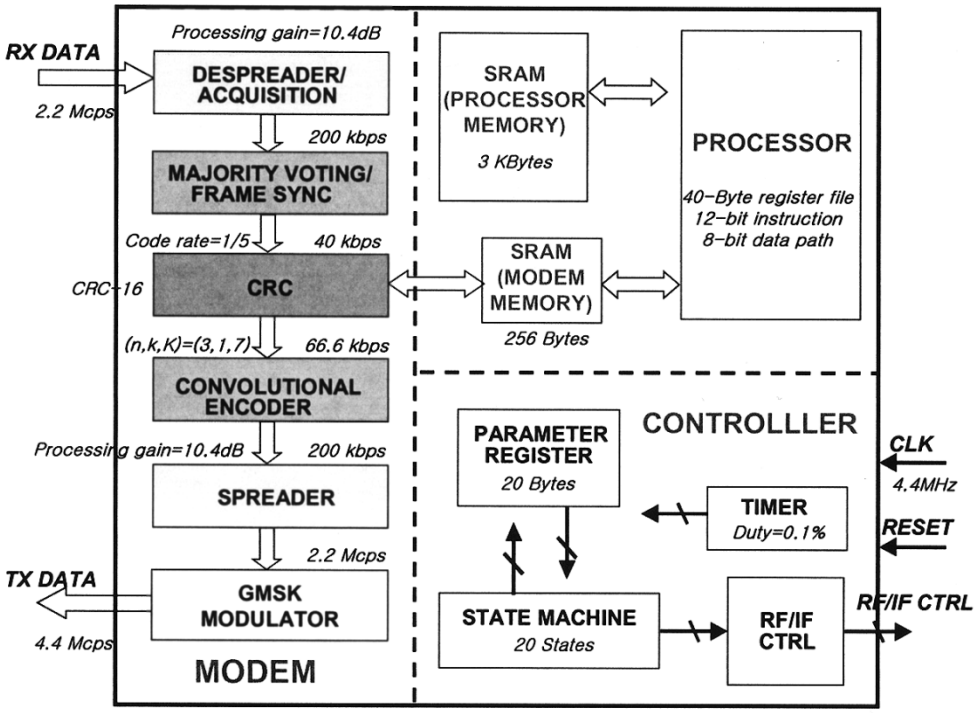

Fig. 18. Baseband chip architecture.

shown in Fig. 19. The die area is 3.5 mm $\times$ 2.5 mm and it consumes only 30 mW in the transmitter chain and 21 mW in the receiver chain, respectively. Fig. 20 shows the demodulated output signal and its eye diagram at the output of the receiver chain. Fig. 21 shows the baseband I/Q waveforms after the DACs and LPFs in the transmitter chain, which are directly upconverted and amplified through up-mixers and a drive amplifier. The spectrum at the output of a drive amplifier satisfies the required spectrum mask as shown in Fig. 22.

A digital modem/processor die micrograph, fabricated using the same process with a radio chip, is shown in Fig. 23. As we operate the digital modem/processor chip in a very low clock frequency of 4.4 MHz, its power consumption is very low at 0.5 mW both for receiver and transmitter modes. The die area of the digital chip is 3.4 mm $\times$ 2.4 mm.

Fig. 24 shows the final implementation feature of the coin-sized radio. Its final size is 3 cm $\times$ 3 cm, most of which is occupied by the antenna. A digital chip is packaged and embedded in a separate PCB for easy measurement and testing. The performance of this radio is summarized in Table III.

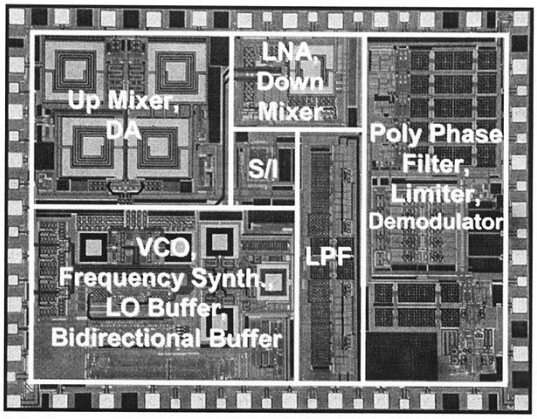

Fig. 19. Die micrograph for the fabricated radio transceiver.

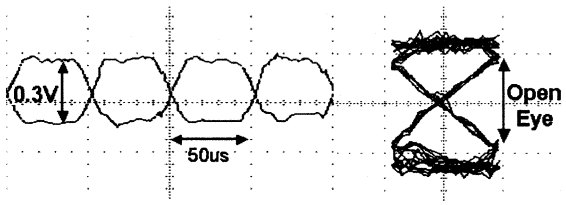

Fig. 20. Output signal and its eye diagram in the receiver chain.

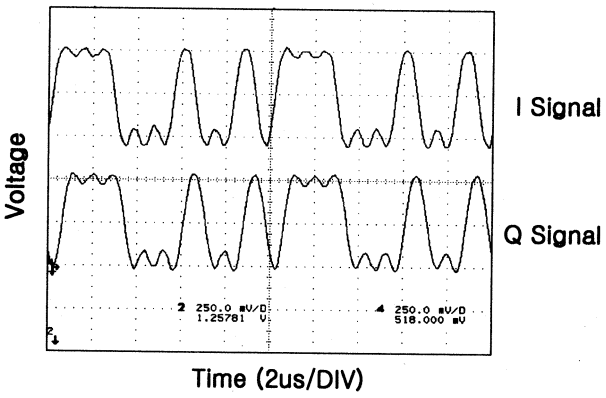

Fig. 21. Baseband I/Q waveforms in the transmitter chain.

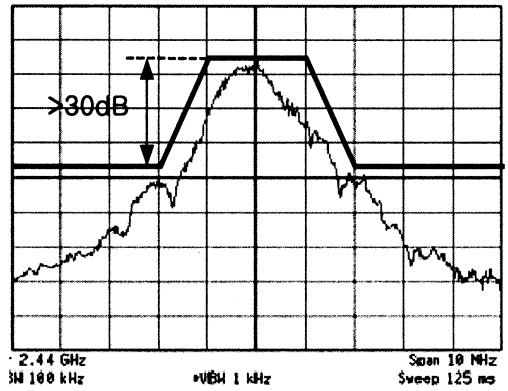

Fig. 22. Spectrum measured at the transmitter output.

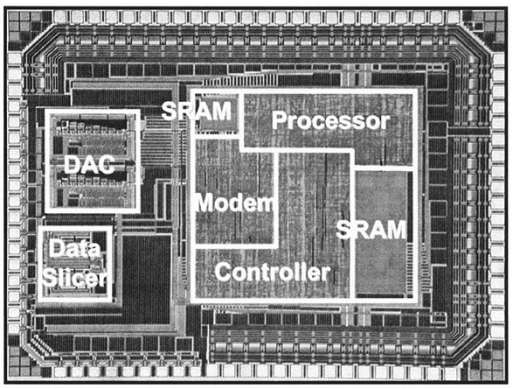

Fig. 23. Die micrograph for the fabricated digital modem/processor.

VI. Conclusion

An experimental 2.4-GHz radio for the low-power and low-rate preliminary IEEE802.15.4 WPAN is reported, implemented in a two-chip solution in 0.18-μm CMOS technology.

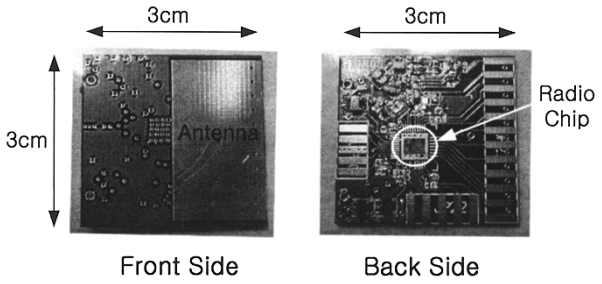

Fig. 24. Implemented radio.

TABLE III
RADIO PERFORMANCE SUMMARY

Vdd	1.8V
Tx chain power consumption	18mW
Rx chain power consumption	9mW
Frequency synth. power consumption	12mW
Digital chip power consumption	500μW@4.4MHz
Receiver sensitivity	-82dBm
IIP3 of the RF front end	6dBm (low gain) -4dBm (high gain)
Image rejection	-30dBc
Tx output power	0dBm
Technology	0.18μm 1P6M CMOS
Die size	3.5mm x 2.5mm (RF) 3.4mm x 2.4mm (Digital)

The highly integrated radio transceiver with 3.5 mm $\times$ 2.5 mm die size consumes 21 mW in receive mode and 30 mW in transmit mode with a 1.8-V supply. The receiver adopts a low-IF architecture with noncoherent data demodulation. It has a highly linear RF front-end, achieved using a linearization technique which breaks the fundamental tradeoff between IIP3 and power consumption. The direct upconversion transmitter and the frequency synthesizer offering 2.4-GHz differential and quadrature LO signals are also integrated on the radio chip. Chip-on-PCB technology allows implementation of a small-size radio at very low cost, along with a small-size patch antenna and high-Q inductors. Digital calibration helps to improve the system performance.

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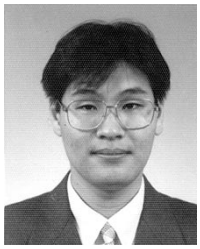

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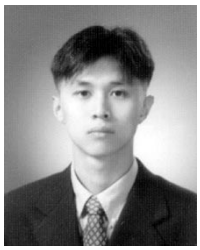

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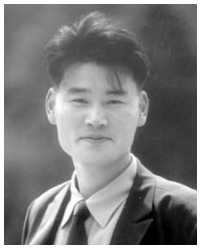

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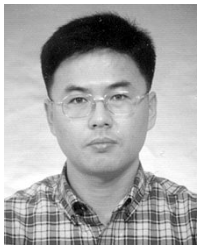

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