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A New Family of Cascaded Transformer Six Switches Sub-Multilevel Inverter with Several Advantages

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Abstract – This paper presents a novel topology for cascaded transformer sub-multilevel converter. Each sub-multilevel converter consists of two DC voltage sources with six switches to achieve five-level voltage. The proposed topology results in reduction of DC voltage sources and switches number. Single phase low frequency transformers are used in proposed topology and voltage transformation and galvanic isolation between load and sources are given by transformers. This topology can operate as symmetric or asymmetric converter but in this paper we have focused on symmetric state. The operation and performance of the suggested multilevel converter has been verified by the simulation results of a single-phase nine-level multilevel converter using MATLAB/SIMULINK.

Keywords: Sub-Multilevel inverter, Six switches, Symmetric state.

1. Introduction

Multilevel inverter is considered as one of the most significant recent advances in power electronics. The advantages of these converters approach include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability [1]. Most multilevel inverters have an arrangement of switches and DC voltage sources or DC links capacitor. By a proper control of the switching devices, they can generate staircase output voltages. The desired output of a multilevel inverter is synthesized by several sources of DC voltages. Some of the fundamental multilevel topologies include the diode-clamped [2-4], flying capacitor [4-6], and cascaded H-bridge structures [7-10]. Several combinatorial designs have also emerged by means of cascading the fundamental topologies that they are called hybrid topologies [10-12]. The main disadvantage associated with the multilevel configurations is their circuit complexity, requiring a high number of components, semiconductor switches, driver circuits and DC voltage sources. Recently, several multilevel converter topologies have been developed [13-20]. Novel topologies of cascaded multilevel inverters using a reduced number of switches and gate driver circuits are presented in [13-16].

A new topology is recommended in [13], and in [14], the optimal structures for this topology are investigated. Reduction number of switches and DC voltage sources for producing the maximum output voltage levels are main advantage of this topology. The main disadvantage of this topology is requiring multiple DC sources and bi-directional switches. In [15, 16] novel configuration of cascaded multilevel inverters have been proposed. The suggested topologies need fewer switches and gate driver circuits but they require multiple DC sources and some switches of suggested topologies have high peak inverse voltage (PIV). A symmetrical multilevel inverter has been presented in [17]. This multilevel inverter can generate DC voltage levels similar to other topologies with less number of components but it requires multiple DC sources.

A novel H-bridge multilevel pulse width modulation converter topology based on a series connection of a high-voltage diode-clamped inverter and a low-voltage conventional inverter is proposed in [18]. A DC link voltage arrangement for the new hybrid and asymmetric solution is presented to have a maximum number of output voltage levels by preserving the adjacent switching vectors between voltage levels [18] but it needs a lot of number of capacitors and operation in asymmetric state has some limitation.

In [19] novel configuration of multilevel multicell has been proposed and provide a high number of output levels, high modularity and low number of components [19] but they require multiple capacitors and some switches of suggested topologies have high PIV.

In [20] novel configuration of flying capacitor multicell Converter has been proposed. Proposed configuration of multicell inverter requires less number of switches in comparison with typical flying capacitor multicell inverters but it needs a lot of number of capacitors and some switches of suggested topology have high PIV.

Recently cascaded transformer multilevel topologies are proposed. These have the advantage of having single DC voltage source and transformer can be used to voltage transformation and isolation [21-23]. The leakage reactance

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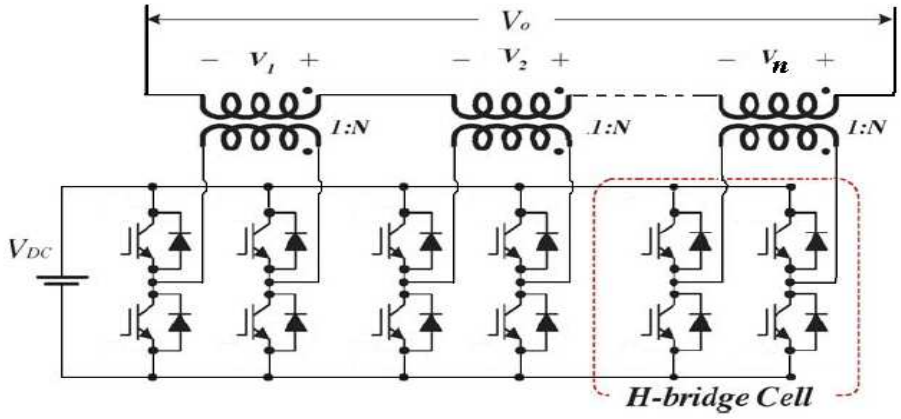

Fig. 1. Circuit diagram of a single phase cascaded transformer H-bridge multilevel inverter.

of the cascaded transformers provides high-performance filtering effect of the harmonic components of the inverter output voltage [24-26].

Fig. 1 shows a single-phase topology of a cascaded transformer converter with single DC voltage source [26]. In cascaded transformer H-bridge multilevel inverters, selection of turn ratio of transformers is main part of inverter design. The output voltages of basic units are cascaded through the secondary of the transformers. The input voltage to transformers is defined by switching functions of the basic units. Output voltage is sum of the transformers output voltages. The amplitude of the output voltage is determined by the input DC voltage source and turn ratio of the transformers. An output phase voltage waveform is obtained by summing the output voltages of transformers:

$$V_O = V_1 + V_2 + \ldots + V_n \quad (1)$$

The cascaded transformer H-bridge multilevel inverter can operate in symmetric or asymmetric state to obtain uniform step voltage. If all turn ratios of transformers are the same, the inverter is known as symmetric multilevel inverter. The maximum number of phase voltage levels is given by:

$$m = 2n + 1 \quad (2)$$

Where *n, m* are the number of DC voltage source and the maximum number of levels of phase voltage respectively.

An attempt has been made in this paper to introduce a new topology for cascaded transformer multilevel inverter which employs two single DC voltage sources and isolated single-phase low-frequency transformers. This topology consists of series connected sub-multilevel inverter blocks. By the proposed circuit configuration, a number of switches and DC voltage sources (or DC link capacitors) can be reduced, compared with traditional multilevel inverters. Proposed inverter can operates as symmetric or asymmetric converter but in this paper we have focused on symmetric state. To verify the performance of the proposed cascaded transformer multilevel inverter, we carried out computer-aided simulations and experiments using a prototype. There are several modulation strategies for multilevel inverters [27-29]. In this work, the fundamental frequency switching technique has been used.

2. Sub-Multilevel Inverter

Fig. 2 shows the suggested sub-multilevel inverter block. This consists of two DC voltage sources equal to $\frac{V_{dc}}{2}$ with six switches and single phase low frequency transformer. There are six switches in the proposed sub-multilevel inverter block to achieve five-level voltage. The H_1 and H_2 switches in sub-multilevel inverter block in Fig. 2, only can generate the positive output voltages. For generating both of the positive and negative output voltages, the H-bridge structure shown in Fig. 2 is proposed. Zero level is produced with H-bridge cell. Zero level could be produced with H_3 and H_4 or H_5 and H_6.

Fig. 3 shows six valid operating states in the sub-multilevel inverter block to generate five different voltage levels on the ac side of sub-multilevel inverter. In generation second positive level, for example, H_1, H_3 and H_6 are turned on.

The sub-multilevel inverter blocks shown in Fig. 2 can be cascaded as shown in Fig. 4. An output phase voltage is obtained by summing the output voltages of transformers:

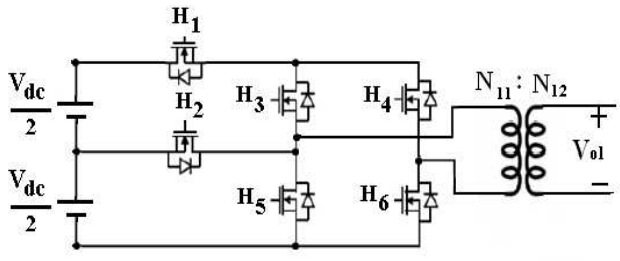

Fig. 2. Suggested sub-multilevel inverter block.

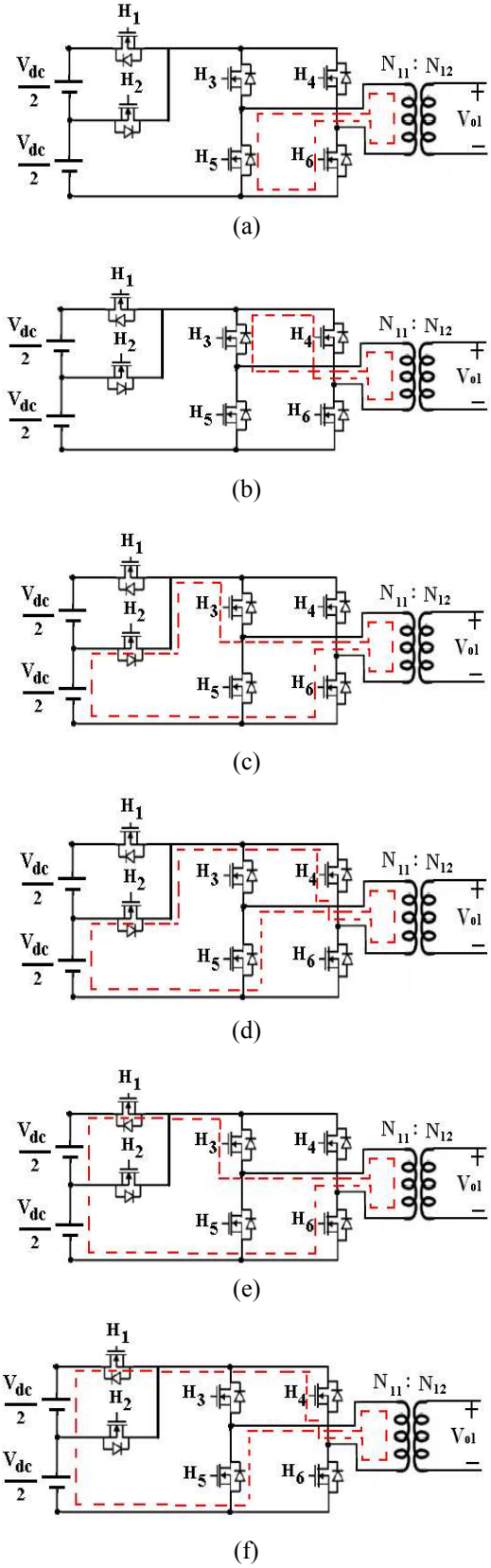

Fig. 3. Six operating states in the sub-multilevel inverter block: (a) zero level; (b) zero level; (c) first positive level; (d) first negative level; (e) second positive level; (f) second negative level.

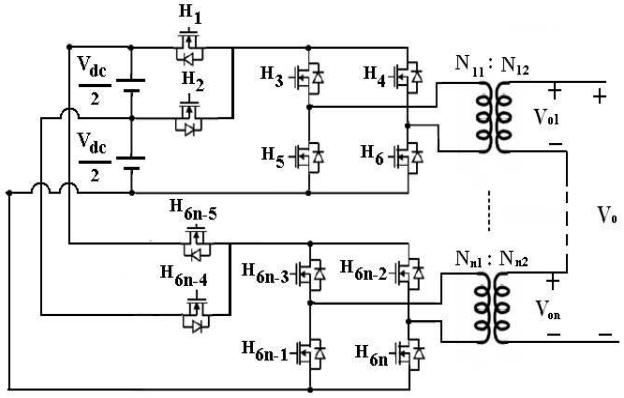

Fig. 4. Proposed multilevel inverter.

$$V_O = V_{O1} + V_{O2} + .. + V_{On} \tag{3}$$

Where n is the number of cascaded transformers. If all turn-ratio of transformers in Fig. 4 are equal to 1:N then the converter is known as symmetric multilevel inverter. The effective number of output voltage levels (m) in this topology may be related to the number of transformers (n) by:

$$m = 4n + 1 \tag{4}$$

The maximum output voltage of this n cascaded transformers is:

$$V_{Omax} = n.N.V_{dc} \tag{5}$$

The number of switches is given as:

$$SW_P = 6n \tag{6}$$

$$SW_P = \frac{3(m-1)}{2} \tag{7}$$

Where SW_p is number of switches in proposed topology.

3. Comparison study

In multilevel inverter topologies, the required number of power devices depends on the output voltage level. However, increasing the number of power semi-conductor switches increases the inverter circuit size, cost, installation area and control complexity. To provide a large number of output levels without increasing the number of switches and DC voltage sources, a new power circuit topology based symmetrical multilevel converter is proposed. To probe the reduction in component numbers achieved by this new configuration, Table 1 presents the number of components required to implement a five-level inverter using the proposed topology and four previously multilevel inverters that can be considered as the standard multilevel inverters.

Table 1. Comparison of power component requirement.

	Diode clamped	Flying capacitor	cascaded H-bridge	Cascaded transformer H-bridge	Proposed
Main Switches	8	8	8	8	6
DC Source	1	1	2	1	2
DC link capacitor	4	4	0	0	0
Main Diode	8	8	8	8	6
Clamping Diode	6	0	0	0	0
Balancing Capacitor	0	3	0	0	0
Transformer	0	0	0	2	1
Total	27	24	18	19	15

The new topology achieves a 25% reduction in the number of main switches required, using only six controlled power switches instead of the eight required in any of the other four configurations. The number of switches in four standard configurations is given as:

$$SW_S = 2(m-1) \tag{8}$$

With notice to Eqs (7) and (8) 25% reduction in the number of main switches is calculated as:

$$\frac{SW_P}{SW_S} = \frac{\frac{3(m-1)}{2}}{2(m-1)} = \frac{3}{4} = 0.75 \tag{9}$$

In comparison between diode clamped configuration and proposed topology, the new topology reduces the number of diodes and reduces the number of capacitors by 100%.

$$\frac{D_P}{D_{dc}} = \frac{\frac{3(m-1)}{2}}{2(2m-3)} = \frac{3(m-1)}{8(m-1.5)} \tag{10}$$

Where D_P and D_{dc} are number of diodes in proposed and diode clamped configurations.

The new topology achieves almost a 60% reduction in the number of diodes required when compared with the diode clamped configuration.

In comparison between flying capacitor configuration and proposed topology, the new topology doesn't need any DC link capacitor and balancing capacitor and reduces the number of capacitors by 100%. The new topology achieves a 25% reduction in the number of main diodes according to Eq. (9) when compared with the flying capacitor configuration.

In comparison between cascaded H-bridge configuration and proposed topology, number of DC voltage sources and switches are reduced.

Existence of transformers in multilevel inverter configurations may be add to circuit size and cost while three previously multilevel inverters don't need any transformers in their structures but it is important to notice this point that a case where it needs to high voltage output from low voltage source, previously multilevel inverters require additional components or step-up transformers. However, voltage transformation and galvanic isolation capability obtain in presence of transformers in proposed structure.

In comparison between transformer H-bridge multilevel inverter and proposed topology, number of transformer and switches are reduced although the proposed topology has two DC voltage source in its structure.

To provide a large number of output levels without increasing the number of components, asymmetric multilevel inverters can be used. Proposed multilevel inverter can operate as asymmetric multilevel inverter. In order to achieve asymmetric state, different methods for the determination of turn-ratio of transformers can be used. In this paper, the turn-ratio of transformers can be chosen according to a geometric progression with a factor of 2, 3 and 5.

For *n* cascaded sub-multilevel inverters, in the binary, Trinary and Fifnary method the turn-ratio of transformers are suggested to be chosen according to the following algorithm:

Binary method:

$$N_{11} = N_{21} = \cdots = N_{n1}$$
$$N_{i2} = (2^{i-1})N_{i1} \quad \text{i=1,2,...,n} \tag{11}$$

Trinary method:

$$N_{11} = N_{21} = \cdots = N_{n1}$$
$$N_{i2} = (3^{i-1})N_{i1} \quad \text{i=1,2,...,n} \tag{12}$$

Fifnary method:

$$N_{11} = N_{21} = \cdots = N_{n1}$$
$$N_{i2} = (5^{i-1})N_{i1} \quad \text{i=1,2,...,n} \tag{13}$$

Table 2 shows the number of voltage levels of asymmetric multilevel inverters based on proposed topology. These asymmetric multilevel inverter schemes efficiently increase the number of output voltage levels based on the different turn-ratio of the cascaded transformers.

The different turn-ratio of cascaded transformers means the unbalance of power distribution per individual transformer and means the different saturation conditions of the transformers [26]. In this work we have focused on symmetric state.

Table 2. Number of voltage levels of asymmetric proposed topologies.

	Binary	Trinary	Fifnary
Number of levels	$2^{n+2}-3$	$2(3^n-\frac{1}{2})$	5^n

4. Simulation Results

To verify the performance of the proposed multilevel inverter in the generation of a desired output voltage, a prototype is simulated based on the proposed topology according to that is shown in Fig. 5. As can be seen this converter uses two units in series per output phase, with an output transformer. The MATLAB software has been used for simulation. In the simulation, the switches are assumed ideal.

The first study is for investigating the waveforms of the symmetric converter. The turn-ratio of transformers in Fig. 5 are equal to 1:1. For this reason, the converter has been adjusted to produce a 50Hz, 9-level staircase voltage waveform. A simulation has been made on the R-L load (R=12Ω and L=30mH) and $\frac{V_{dc}}{2} = 50V$. Table 3 shows the ON switches look-up table for the symmetric state of multilevel converter shown in Fig. 5. Note that there are different switching patterns for producing the zero, first, second and third level, and that only one of them is shown in Table 3.

Figs. 6(a) and (b) show the input voltage of the transformer in the different units. Each unit generates a quasi-square waveform with positive, zero and negative values. The harmonic spectrums of the transformer input voltage are shown in Figs. 6(a) and 6(b), too. The DC value of input voltages of transformers is very low (near to zero). The magnitude of lower frequencies than 50 Hz is very small (near to zero) and they can't create difficult in terms of core saturation. So no problem exists about transformer saturation in proposed structure. The output voltages of transformers are the same as input voltage of transformers because the turn ratios of transformers are 1:1. The overall output voltage of the converter is the sum of the outputs of units. Fig. 6(c) shows the output voltage and Fourier analysis.

Table 3. Look-up table of switching in nine-level multilevel inverter.

On Switches	V_O(V)	On Switches	V_O(V)
1, 3, 6, 7, 9, 12	200	1, 4, 5, 7, 10, 11	-200
1, 3, 6, 8, 9, 12	150	1, 4, 5, 8, 10, 11	-150
1, 3, 6, 9, 10	100	1, 4, 5, 11, 12	-100
2, 3, 6, 9, 10	50	2, 4, 5, 11, 12	-50
3, 4, 9, 10	0	5, 6, 11, 12	0

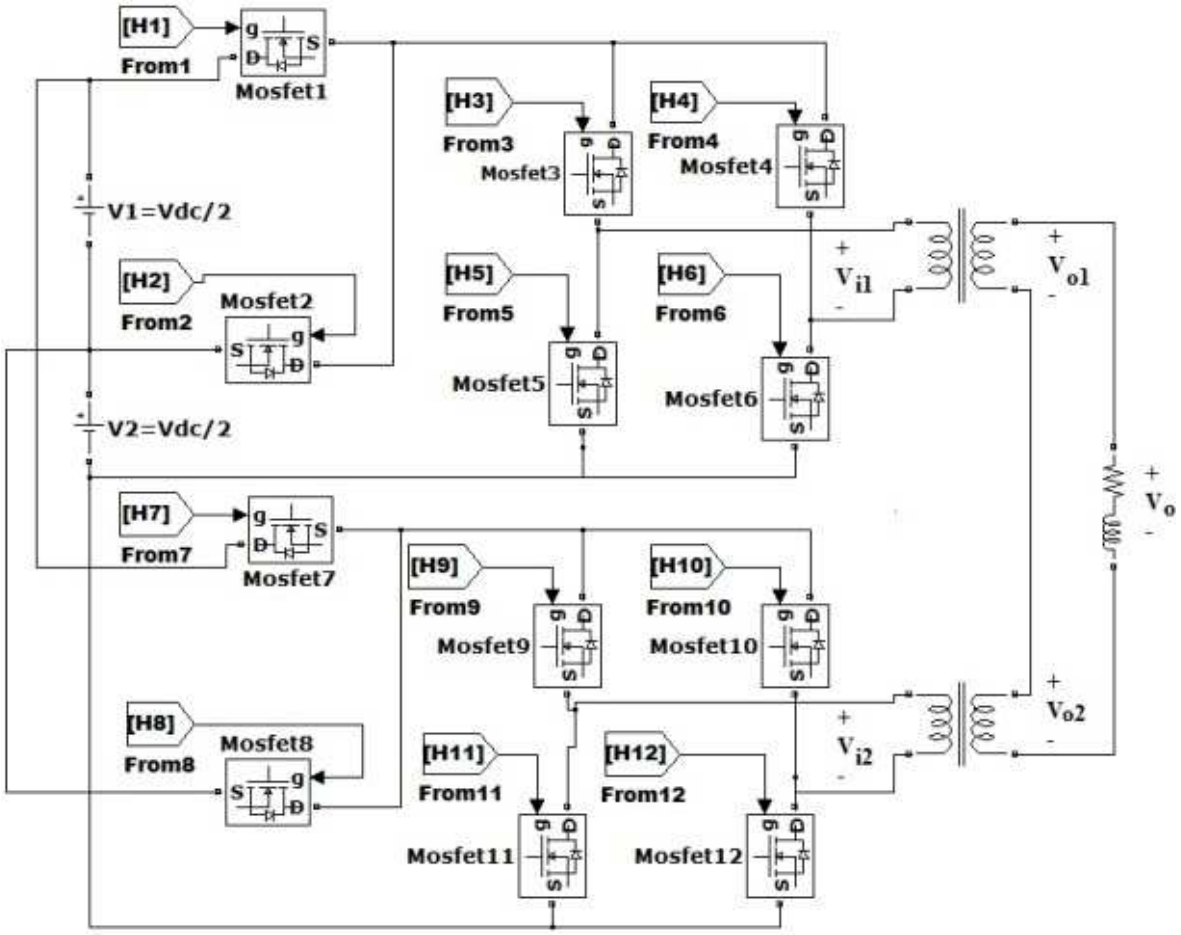

Fig. 5. Proposed 9-level symmetric multilevel inverter.

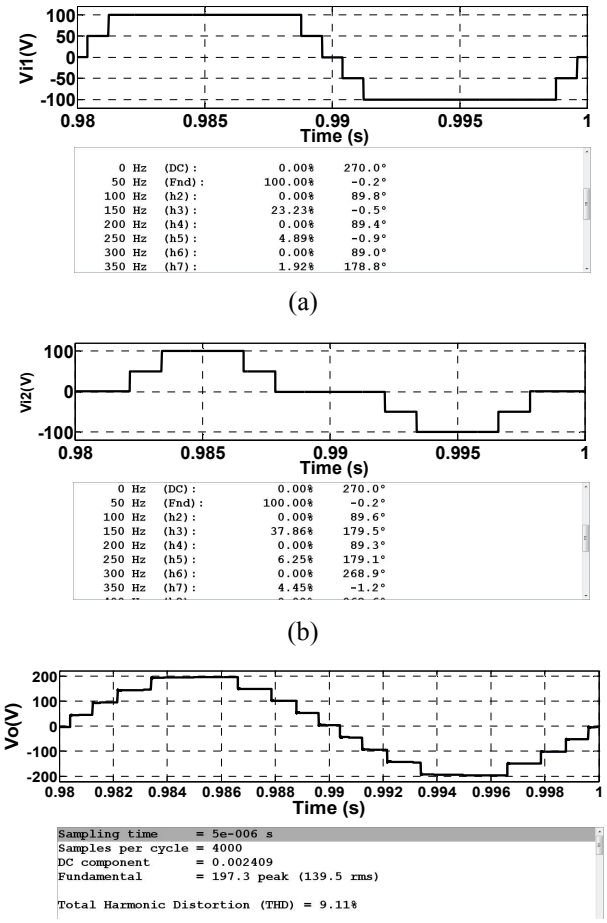

Fig. 6. 9-level multilevel inverter: (a) input voltage of the transformer, V_{i1}; (b) input voltage of the transformer, V_{i2} and (c) output voltage, V_o.

Table 4. Look-up table of switching in twenty five-level inverter.

On Switches	V_O(V)	On Switches	V_O(V)
1,3,6,7,9,12	600	1,4,5,7,10,11	-600
2,3,6,7,9,12	550	2,4,5,7,10,11	-550
2,3,4,7,9,12	500	1,5,6,7,10,11	-500
2,4,5,7,9,12	450	2,3,6,7,10,11	-450
1,5,4,7,9,12	400	1,3,6,7,10,11	-400
1,3,6,8,9,12	350	1,4,5,8,10,11	-350
2,3,6,8,9,12	300	2,4,5,8,10,11	-300
2,3,4,8,9,12	250	1,5,6,8,10,11	-250
2,4,5,8,9,12	200	2,3,6,8,10,11	-200
1,4,5,8,9,12	150	1,3,6,8,10,11	-150
1,3,6,8,9,10	100	1,4,5,7,11,12	-100
2,3,6,8,9,10	50	2,4,5,7,11,12	-50
1,3,4,7,9,10	0	2,5,6,8,11,12	0

In the second simulation, by using transformers with a turn ratio according to Fifnary method, the proposed 9-level inverter can be turned into a 25-level multilevel inverter. The turn ratio of transformer in first unit is 1:1($N_{11} = N_{12}$) and for second unit the turn ratio of transformer is 1:5($N_{22} = 5N_{21}$). In this state N_{11} is equal

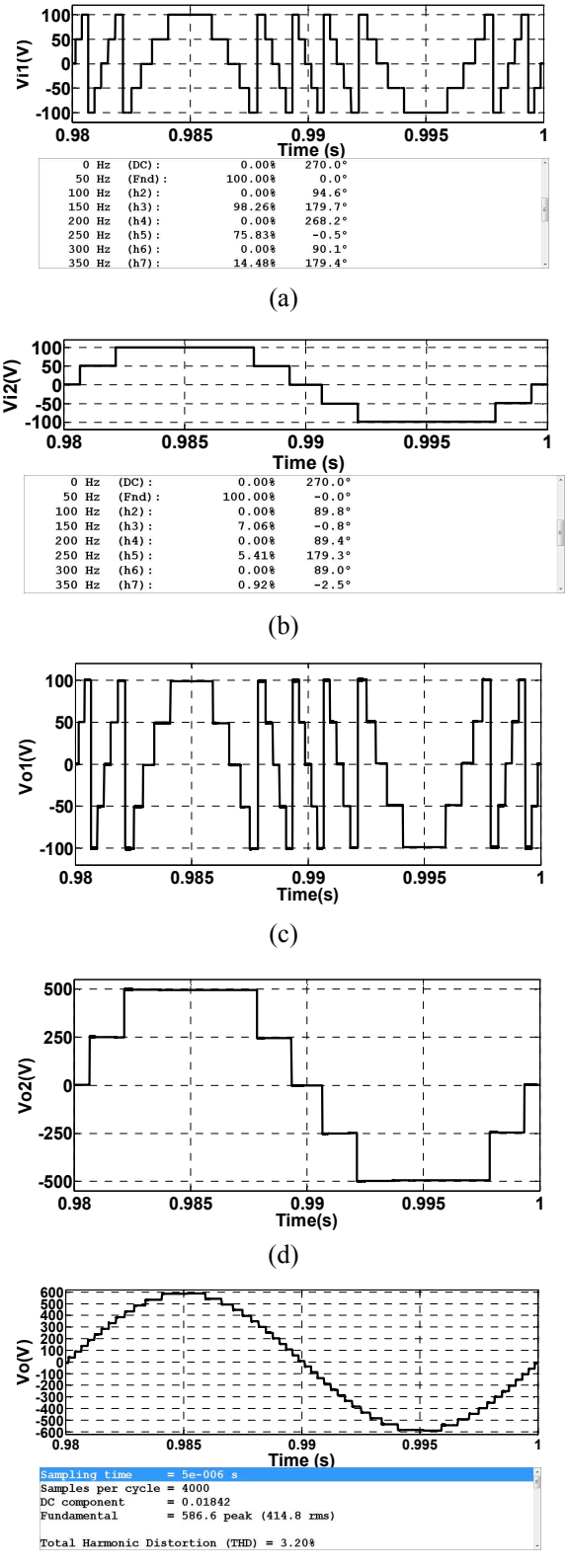

Fig. 7. 25-level multilevel inverter: (a) input voltage of the transformer, V_{i1}; (b) input voltage of the transformer, V_{i2}; (c) output voltage of the transformer, V_{o1}; (d) output voltage of the transformer,V_{o2} and (d) output voltage, V_o.

with N_{21} . Table 4 shows the ON switches look-up table for the 25-level multilevel inverter. Fig. 7(a) and (b) show the input voltage and harmonic spectrums of the transformers in the different units. The DC value of input voltages of transformers is very low. The output voltages of transformers are shown in Fig. 7(c) and (d). The output phase voltage is obtained by summing the output voltages of transformers. Fig. 7(e) shows the output voltage and harmonic spectrum. The proposed converter has 25-level voltages per phase. Total harmonic distortion (THD) of output voltage is as low as 5%. In the case study, THD is equal to 3.2%. It can be observed from the harmonic spectrum of voltages that, presented topology is effective to meet low harmonic level.

5. Conclusions

Conventional diode clamped inverter or flying capacitor inverter needs clamped diodes or flying capacitors in the circuit to achieve multilevel PWM operation. In the adopted inverter, no flying capacitor and clamped diode are used in the circuit configuration. To reduce the number of separate dc sources new configurations have also been presented. The suggested topology needs less switches and gate driver circuits. Therefore, the proposed topology leads to reduction of installation area and cost and has simplicity of control system. Simulation results show that the proposed inverter can produce the desired output voltage.

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