# On-chip Jitter Measurement Using Vernier Ring Time-to-digital Converter

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***Abstract*—This paper presents an on-chip jitter measurement technique based on the Vernier ring time-do-digital converter (VRTDC). Vernier delay line is an attractive structure for the implementation of high performance TDC due to its sub-gate-delay resolution and cancellation of the first order process, voltage and temperature (PVT) variations. In order to improve the detectable range, area cost and power consumption of the conventional Vernier delay line TDC, the Vernier ring structure is developed to place two delay lines and comparator chains in ring format for the reuse of hardware, which enables the VR-TDC to achieve a fine resolution without sacrificing detectable range. The build-in coarse and fine interpolations reduce the power and area. This on-chip jitter measurement scheme can measure a large jitter with a fine resolution smaller than 8ps. An exemplary jitter test is given in this paper to demonstrate the capability of the proposed jitter measurement scheme.**

***Keyword:*** **on-chip, jitter measurement, Vernier, time-to-digital converter, built-in self-test**

## I. INTRODUCTION

With the development of the process scaling down, the clock frequency of the communication systems keeps growing and the deviation of signal and clock from ideal position, namely jitter, becomes a severe issue since the jitter tolerant budget shrinks with the increase of clock speed. Consequently, jitter measurement is necessary but difficult to implement. The measurement using external automatic test equipments and on-chip driver can hardly achieve the results as accurate and efficient as the on-chip jitter measurement provides. It is also hard to take the deep-embedded signal out of the chip without being polluted by the environmental noise. On-chip jitter measurement can circumvent these problems and offer an easy and inexpensive BIST solution. In addition, monitoring the jitter performance locally can provide feedback mechanisms for self-healing, which is one of the most appealing techniques at ultra-deep-submicron process nodes. With the built-in jitter measurement circuit, the frequency synthesizer, including all digital phase-locked loop(ADPLL), can self-adjust loop parameters and generate a clock with the optimized jitter performance.

Recently, the time-to-digital converters (TDCs) have been used in many on-chip jitter measurement macros and BIST applications [1-3]. Time-to-digital converter quantizes the time interval between the clock and reference signal with a time resolution as tiny as several pico-seconds (ps). The histogram of the digitized time intervals obtained in the successive measurements reflects the distribution of the clock jitter assuming the reference signal is jitter free. The interval histogram can be easily processed by the digital signal processing algorism to characterize the jitter performance of the clock signal. The time resolution and detectable range of the TDC are critical to the on-chip jitter measurement. Many TDC architectures have been reported to improve time resolution, detectable range or both.

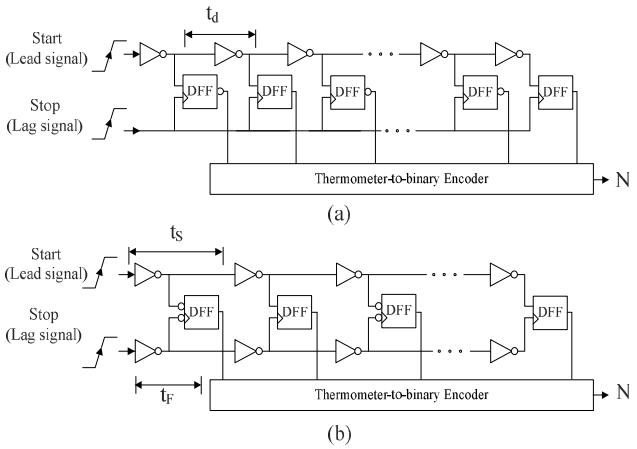


Fig.1 (a) Delay line based TDC (b)Vernier delay line TDC.

The digital inverter is widely used in the time-to-digital converter to digitize the time interval due to its digital-intensive design approach. The inverter delay thus becomes a basic scale in the quantization of time interval [4]. Fig.1 (a) shows the conventional inverter-delay-line based TDC. Its time resolution is the propagation delay of the inverter and this delay is limited by the process with which it is implemented. Its detectable range is equal to the time resolution multiplied by the total number of delay stages used. Therefore more stages are required to increase the detectable range. However both the time resolution and the detectable range of the inverter delay line TDC are very sensitive to PVT variation and matching. The inverter delay chain usually is not very long since the integral non-linearity (INL) will be increased with the length of the delay chain. As shown in Fig.1 (b), Vernier delay line TDC improves the time resolution to the fraction of an inverter delay by employing two inverter/buffer chains with slightly different delays of $T_S$ and $T_F$ , respectively. The delay difference between $T_S$ and $T_F$ becomes time resolution of the Vernier

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TDC, which can tolerate first order PVT variation if the two delay lines are well matched [5].

Recently several topologies have been developed to reduce the TDC time resolution. Two-step interpolation with coarse and fine resolutions improves the detectable range while maintain a very fine resolution [6, 7]. The time-amplifier based TDC employs time-amplification technique in conjunction with two-step interpolation [8]. The Vernier delay line is still an attractive structure for the implementation of a high performance TDC, although there are many new techniques invented to improve the time resolution of TDC. Vernier ring TDC places the delay cells in the ring format to achieve the small resolution and large detectable range simultaneously by reusing the hardware [9, 10].

The jitter of signal under test is usually compared with an approximately jitter-free reference clock. The phase error between two signals can vary in the range of one period of the test signal. Therefore, a large detectable range with a fine resolution TDC is desired in measuring the jitter of a low frequency signal. This paper presents the on-chip measurement scheme utilizing VR TDC, the fine resolution and large detectable range solution compared with other TDC designs.

This paper is organized as follows: section II describes the Vernier ring TDC architecture and explains the on-chip jitter measurement using this novel TDC. Section III describes the application of this jitter measurement technique in the ADPLL to achieve loop dynamics adjustment. Section IV gives experimental results for a proposed jitter-measurement scheme using VR TDC fabricated in 0.13μm CMOS process. Conclusions will be drawn in section V.

## II. JITTER MEASUREMENT WITH VR TDC

The Vernier Ring TDC (VRTDC) leverages the time difference between two rings of delay cells to achieve a sub-gate-delay time resolution. Unlike the conventional Vernier delay line TDC, VR TDC places the Vernier delay stages in a ring format such that the delay chains can be reused for measuring large time intervals. Arbiters compare the arrival sequence of lead and lag signals and detect the location where the lag signal catches up with the lead signal. Lap counters are used to monitor the number of laps the signals propagate along the rings. The reuse of Vernier delay stages and arbiters achieves a fine resolution and large detectable range simultaneously while both area and power consumption remain at a reasonable level. With the Vernier ring structure, detectable range can be increased to a very large number, as long as the counter has enough bits to count laps that two signals have propagate along the rings.

As shown in Fig. 2, the inner and outer chain of arbiters comprise two types of arbiters, type A and type B, which are placed alternatively along the two inverter rings. Arbiter type A is triggered by a logical rising edge while arbiter B is triggered by a falling edge. Both rings comprise the same even number of delay stages and a NAND gate as an initiating stage of the rings. The propagation delay of delay stages in the fast and slow rings are set to $\tau_F$ and $\tau_S$, respectively. Thus, the time

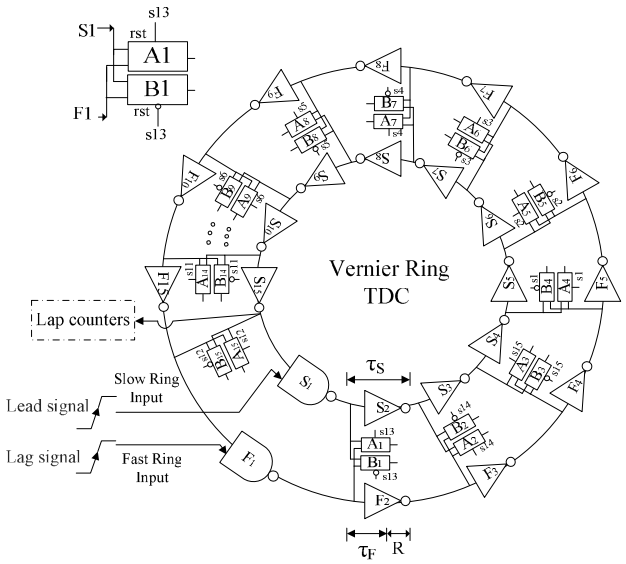



Fig. 2 Block diagram of Vernier ring TDC core.

resolution is given by $R=\tau_S-\tau_F$., which is much less than both $\tau_S$ and $\tau_F$.

In operation, a lead signal is fed into the slow ring through S1. The lag signal is fed into the fast ring through F1. Thus, the lag signal will chase the lead signal around their respective rings and eventually pass the lead signal after a certain amount of propagation. The arbiter pairs determine if the lag signal arrived before the lead signal and if so, output a logic "one" indicating so. Because A type arbiters respond only to rising edges and B type arbiters only respond to falling edges, only one of the pair of arbiters will be activated by the passing lag and lead signals, each lap depending on the orientation of the signals. A fine counter is used to track the number of laps made by the lead signal around the slow ring. A coarse counter is employed to track the number of laps that the lead signal has propagated before the lag signal arrives at the input of the ring TDC. The output of all arbiters are combined into a thermometer which is able to track the outputs of all the arbiters in the TDC ring and thereby determine which arbiter the signals were at when the lag signal passed the lead signal. The combination of thermometer and lap counters can give the total number of delay stage that the lag signal has propagated before it catch up with the lead signal, namely the digitized time interval between the lead and lag signals by the time resolution. As a result, the ring TDC of the present application is able to enjoy the benefits of high interval resolution (being able to sense very small signal delay intervals), without the need for an excessive amount of delay stages. Indeed, by using a ring, the same delay stages are theoretically able to be reused an infinite amount of times thus saving space and ultimately cost per unit.

Fig.3 shows the block diagram of the jitter measurement using Vernier ring TDC. A stable reference signal with much less jitter is required in the jitter measurement using TDC. The test signal is assumed to have a Gaussian distribution with a standard deviation of $\delta_t$ while reference signal's standard

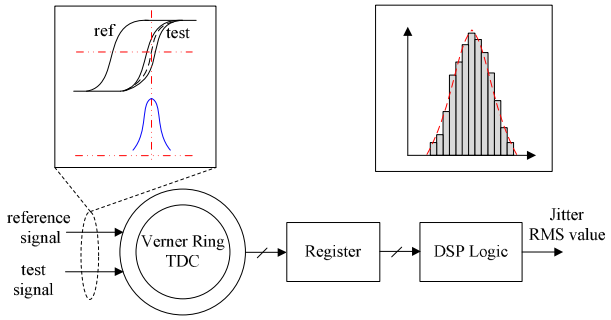



Fig. 3 Block diagram of jitter measurement using Vernier ring TDC.

deviation is $\delta_{ref}$. Thus $\delta_{ref}$ must be much smaller than $\delta_t$. The jitter measurement circuit consists of Vernier ring TDC, register and DSP logic. The reference signal and test signal are input to the Vernier ring TDC and the time interval between these two signals are quantized with a tiny time resolution. The outputs of Vernier TDC are collected in the register where a certain number of the test results are stored and ready for processing by the followed DSP logic. The DSP logic will output the estimated standard derivation and mean value of the measured jitter distribution by calculating the statistics data of the histogram of the collected TDC outputs.

There are many factors that have effects on the accuracy of the jitter measurement. The on-chip jitter measurement using TDC put a stringent requirement on the reference signal. The frequency variation and fluctuation will cause the error in measured jitter. The fixed frequency error, even very small, between reference signal and test signal will generate a ramp of phase error, namely time interval, which will expand the histogram of the collected TDC outputs. The TDC outputs may spread out over a large range of time interval when the accumulated frequency error is larger than the jitter variation range. Moreover, the jitter of reference signal should be negligible compared to the signal under test. The jitter of reference signal is uncorrelated to the test signal therefore this jitter will be added to the measured RMS value of the jitter. The time resolution of the TDC will determine the accuracy of the jitter measurement. The smaller the time resolution is, the more accurate of the measurement can be achieved. The INL and DNL of TDC also affect the measurement accuracy.

## III. ADPLL WITH BULT-IN JITTER MEASUREMENT

As mentioned above, Vernier ring TDC has an important application in all digital phase-locked loop (ADPLL). The VR TDC can be used not only as a phase-frequency comparator, but also as a timing jitter and phase noise detector that can provide tuning controls for a self-healing ADPLL. Fig.4 shows the block diagram of the ADPLL with dynamic loop bandwidth adjustment. This ADPLL consists of a Vernier ring TDC, an IIR low pass filter, a phase noise and jitter detector, an integer-N or a fractional-N frequency divider, a sigma-delta modulator and a DCO.

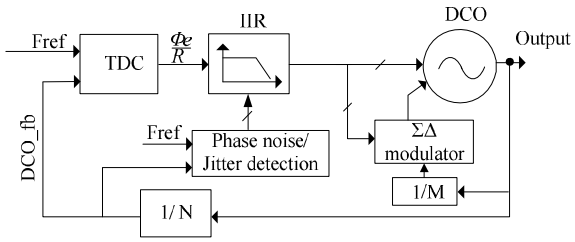



Fig.4 Block diagram of the ADPLL.

PLL loop bandwidth influences the loop settling time, stability, and loop noise performance. A narrow loop bandwidth benefits the in-band noise filtering while a wide loop bandwidth is helpful to remove out-band noise and reduce the loop settling time. In order to minimize the total PLL phase noise, the optimal loop bandwidth should be chosen around the cross point of the in-band and out-band (VCO) phase noise spectral density curves. It's highly desirable that the loop filter bandwidth can be adaptively adjusted during the PLL operation, namely, a wider bandwidth is programmed at the initial stage to allow fast settling of the loop followed by a narrower loop bandwidth that can be chosen by detecting the phase noise or timing jitter of the PLL output and programming the loop filter bandwidth for optimal phase noise and spur rejection, as shown in the proposed ADPLL architecture (Fig. 4). Even if a loop filter can be integrated, a problem associated with integrated analog filters is the cutoff frequency variation due to PVT variations. In a conventional analog PLL, the loop filter is normally placed off-chip due to large component values that are not suitable for integration. For the ADPLL, the digital loop filter can be integrated and programmed on the fly.

The digitized phase error between reference signal and DCO feedback signal can be utilized to characterize the ADPLL output jitter performance when the ADPLL is in locked and the reference jitter is negligible. The ADPLL output jitter is dependent on the loop bandwidth and thus can be optimized through detecting the minimum jitter value when sweeping the loop bandwidth in a reasonable range. As mentioned above, the output jitter can be measured by comparing the DCO feedback signal with the reference signal and the histogram of the phase error can be converted into the RMS value of the jitter. Sweeping the loop bandwidth will generate a curve of the jitter vs. loop bandwidth. A DSP optimization algorism is employed to find the appropriate loop bandwidth where the minimum of RMS jitter of the ADPLL output signal is achieved.

## IV. MEASURED RESULTS

In order to verify the proposed jitter measurement scheme using VR-TDC, a jitter testing set up is illustrated in Fig.5. Two off-chip signal generators are used to generate reference signal and test signal for the jitter measurement. The phase modulation is achieved by adjusting the delay of the test signal with a modulating signal to introduce the jitter. The modulating signal is a random signal (noise) with the tunable amplitude

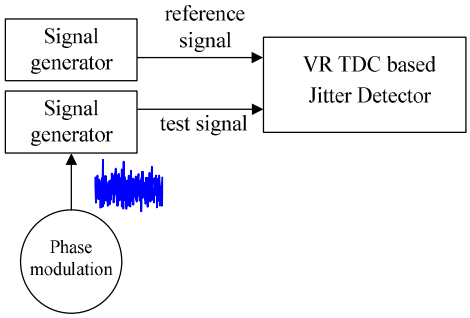
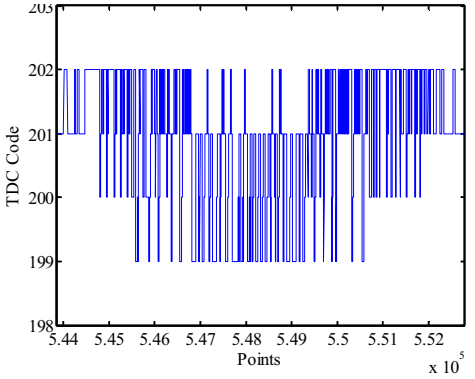
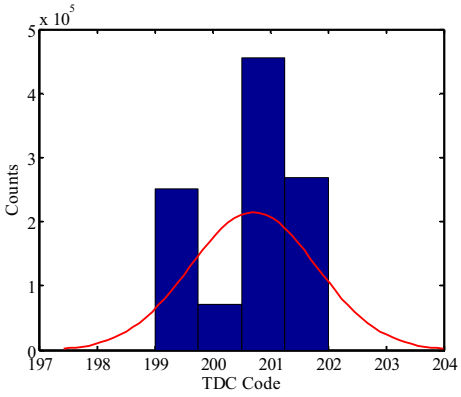



Fig. 5 Block diagram of jitter testing setup.




(a)




(b)

Fig.6 (a)Transient waveform and (b) histogram of TDC output with the estimated μ=200.7LSB and δ=1.09LSB when measuring a pre-defined 20ps peak-to-peak jitter with a DC offset phase error of 2.05ns.

and DC offset. An exemplary test for the proposed VR-TDC jitter measurement was configured as depicted in Fig. 5. A prototype Vernier ring TDC fabricated in 0.13μm CMOS technology was tested using a test signal and reference signal from two channels of the Agilent pulse generator 81134A. A Gaussian noise with the adjustable amplitude and dc offset was generated by an arbitrary waveform generator and then applied to the delay control input of the pulse generator. This voltage input can linearly modulate the delay of the test signal pulses, namely the phase of the pulses. Thus the jitter of the test signal is known since the delay-to-voltage gain is pre-defined in the aforementioned pulse generator.

In this exemplary test, a peak-to-peak 20ps phase variation was modulated to the test signal and the average time interval between two signals is 2.05ns. Vernier ring TDC measured the time-varying jitter in a successive way and the transient measurement results are shown in Fig.6 (a). The TDC output code varies from 199 to 202 when the time resolution is set to 10.2ps. Fig.6 (b) displays the histogram of quantized time intervals and a normal distribution curve drawn in red. The estimated standard derivation and mean value of the histogram are 11.2ps and 2.047ns, respectively. The measurement results are consistent with the jitter of the test signal. The linearity of phase modulation, phase noise of reference signal, TDC quantization noise and noise coupled from PCB and power supply may affect the distribution of TDC output codes.

## V. CONCLUSION

This paper presents an on-chip jitter measurement scheme using Vernier ring TDC. The VR-TDC can achieve a fine resolution and large detectable range simultaneously while the power consumption and area cost are kept at a low level. An exemplary test is given to demonstrate the capability of this on-chip jitter measurement scheme. The proposed on-chip jitter measurement scheme can be used to provide feedback controls for jitter cancellation in RF clock generation circuits with self-healing capability.

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