Chapter 2
Materials and Devices for Nanoelectronic Systems Beyond Ultimately Scaled CMOS

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Introduction

The technological and economic feasibility of high-density, large-scale nanoelectronic systems integration is still being driven by the fundamental paradigms of classical CMOS technology, for which there will be no apparent substitutes in the next 10 to 15 years. However, we cannot expect to continue the lithography scaling of classical CMOS devices and circuits indefinitely, due to fundamental physical limitations such as process variability, excessive leakage, process costs, and very high power densities. This observation calls for radical action on several fronts in order to ensure the continuity of the nanoelectronic systems integration paradigm *until* one or more feasible alternative technologies emerge to replace CMOS within the next 15-year time frame. In particular, we will have to consider the introduction of *new materials and technology steps* to augment and ameliorate the classical CMOS process/devices, explore *new device structures* that can provide reliable performance and sufficiently low power dissipation at high-density integration, and develop new fabrication technology for the CMOS-compatible integration of new materials and nanostructures for new devices in CMOS process flows (approach of stepwise substitution).

In order to keep a strong link to existing CMOS technologies and the ITRS roadmap, compatibility with silicon-based fabrication technologies shall be an important guideline, at least in the near term. On the one hand, this calls for *new materials and fabrication techniques* to further improve the device characteristics and to overcome the limitations of the existing and projected CMOS devices (such as high-k dielectrics, high-mobility substrates, etc.). On the other hand, new nanotechnology components will have to be *hybridized with silicon CMOS* as an add-on approach. Ultimately, the road to developing completely revolutionary nanotechnology platforms (including materials, devices, and integration technologies) should be open – yet the near-term approach will also require a closer link with silicon-based CMOS technologies.

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Clearly, the stated objectives can only be achieved with a strong collaboration and interplay of all disciplines involved in this endeavor to search for new solutions. In particular, the innovations to be explored at the circuit and system levels will have to be inspired by the possibilities offered by new materials and device technologies – while the direction of materials and device research will have to be influenced by the architectural choices made at the system level.

In this chapter, we review some of the most recent results in these areas and put them in a unified context that covers a very wide range, from materials to system design. The first section presents a top-down silicon nanowire fabrication platform for high-mobility gate-all-around (GAA) MOSFETs and impact-ionization devices. Ferroelectric FET with sub-100-nm copolymer P(VDF-TrFE) gate dielectric are examined in the next section for nonvolatile memory applications, which is a very promising direction toward future high-density memory arrays, followed by a discussion of materials for piezoelectric nanodevices in the last section.

Top-Down Silicon Nanowire Fabrication Platform: High-Mobility Gate-All-Around MOSFETs and Impact-Ionization Devices

The main advantage of the top-down technologies are that as they are defined by lithography, the wire placement on the wafer is accurately defined. Top-down silicon nanowire technology fabrication is potentially no more challenging than fabrication of conventional bulk or silicon-on-insulator (SOI) CMOS devices [1, 2]. However, since most nanowires are sublithographic in nature, down-scaling and dimensional control are more challenging than for the bottom-up technologies. Another issue that might be problematic for top-down technologies is doping and the variability of the dopants in small-dimensional structures, especially in cases where the processes defining the nanowires are influenced by the dopants, as is the case in our process. Oxidation rates are highly dependent on the doping concentration and, to a lesser degree, on the etching. However, doping variability is an issue for all nanoscale electronics.

In this work we have developed a versatile top-down silicon nanowire platform that allows for the fabrication of various devices, reported in detail in [3–11]. We have demonstrated enhanced electron mobility due to oxidation-induced tensile strain in GAA bent MOSFETs. We have developed punch-through impact-ionization MOS (PIMOS) devices on body-tied Ω-gate MOS structures. These devices show less than $-10\,\mathrm{mV/dec}$ abrupt switching combined with abrupt switching in both $I_\mathrm{D}(V_\mathrm{DS})$ and $I_\mathrm{D}(V_\mathrm{GS})$. A 1-PIMOS DRAM memory cell has been demonstrated, whereas we have also fabricated an NMOS inverter that maintains an abrupt transition and hysteresis and shows a unique gain of -80.

By combining the resources of technology and device research with that of circuit design, we have demonstrated the ability to create some innovative electronic building blocks that represent the first steps toward logic-on-wire. In the future we would like to extend this work even further and experimentally demonstrate more advanced nanowire architecture such as the addressing scheme of crossbar memories.

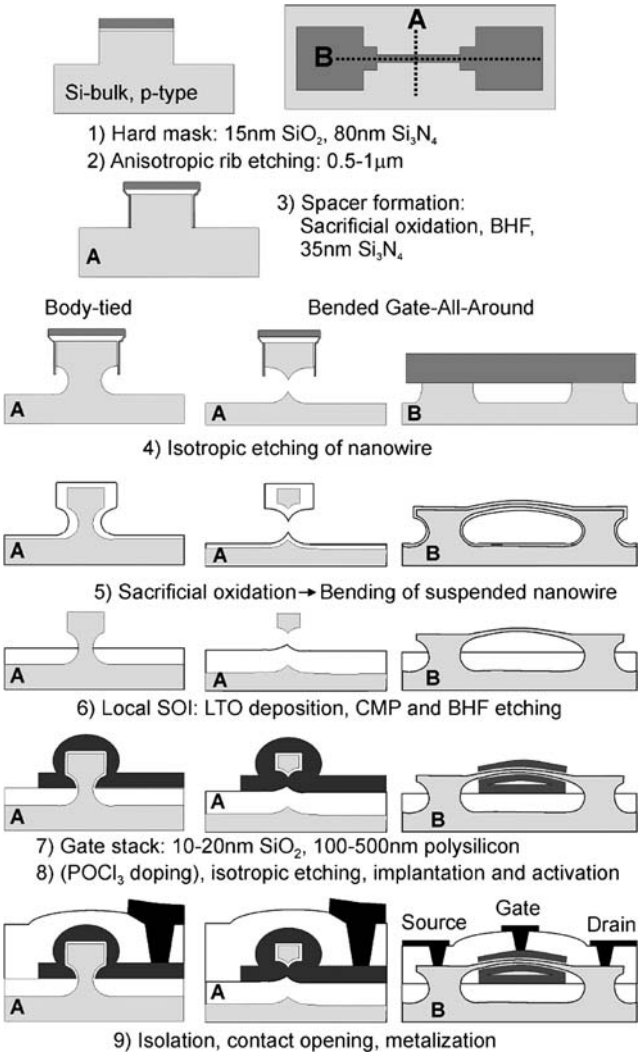

Fig. 2.1 Process flow for top-down fabrication of silicon nanowires with pentagonal cross-section. Cross-section A is shown for both body-tied and suspended (bended GAA) devices, whereas the cross-section B is only shown for the suspended wires

Top-Down Nanowire Fabrication Platform

A schematic of the process flow is shown in Fig. 2.1; it depicts devices of pentagonal cross-section, but a triangular cross-section is obtained by varying the anisotropic rib etching, step 2, and the isotropic etching, step 4. Two different cross-sections are shown for the electronic device. The first one, A, is across the MOSFET channel, and the second, B, runs along the MOSFET channel from the source plot to the drain plot. For the body-tied device, only cross-section A is shown, whereas for the

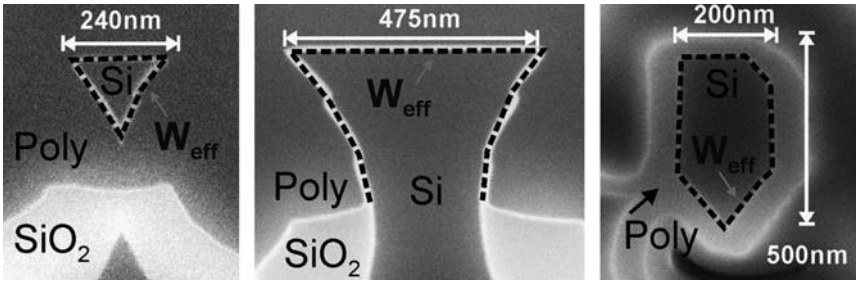

Fig. 2.2 Cross-section SEM/FIB images of triangular and tri-gate fabricated devices. Also illustrated: the definition of effective width, W_{eff}, of three different devices

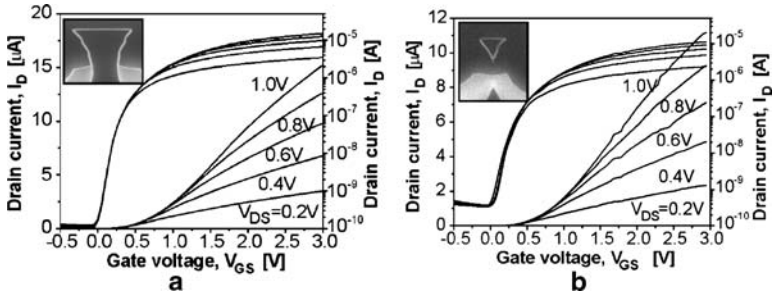

Fig. 2.3 $I_{\text{D}}(V_{\text{GS}})$ characteristics for 10-μm-long devices; *inset* shows a corresponding cross-section. **a** Tri-gate device with $W_{\text{eff}} = 1.12\,\mu\text{m}$. **b** Gate-all-around device with $W_{\text{eff}} = 400\,\text{nm}$

suspended bended GAA device both cross-sections A and B are of interest. The triangular devices are primarily developed for field-effect transistors and fabricated on p-type (boron) (100) wafers of resistivity 0.1 to 0.5 cm, which corresponds to a doping density of $3\times10^{16}\,\Omega\,\text{cm}^{-3}$ to $2\times10^{17}\,\text{cm}^{-3}$. Devices with a pentagonal cross-section, as shown in the process flow in Fig. 2.1, are fabricated on high-resistivity p-type (boron) wafer 15 to 25 Ω cm, $5\times10^{14}\,\text{cm}^{-3}$ to $9\times10^{14}\,\text{cm}^{-3}$, and they serve punch-through impact-ionization (PIMOS) devices. These latter devices are also made with triangular cross-sections. The triangular process flow is simpler; in this case surface roughness on the vertical side walls is not an issue, and the aspect ratio is smaller, which makes the local-SOI fabrication easier. Figure 2.2 shows cross-sections of some of the fabricated devices using the process from Fig. 2.1.

Devices of a wide range of cross-sections have been fabricated and characterized. Device effective widths range from 16 nm, for the smallest circular GAA MOSFET, to 40 μm, for quasi-planar devices, and gate lengths of characterized devices range from 0.9 to 20 μm. Conventional $I_{\text{D}}(V_{\text{G}})$ characteristics of typical $10-\mu\text{m}$-long fabricated devices with two different sections are shown in Figs. 2.3 and 2.4. The I_{on} current measured at $V_{\text{GS}} = V_{\text{DS}} = 2\,\text{V}$ is approximately $22\,\mu\text{A}/\mu\text{m}$ for the GAA MOSFET and about $10\,\mu\text{A}/\mu\text{m}$ for the tri-gate device, in both cases for a 10-μm-long device. The corresponding values for I_{off} measured at $V_{\text{GS}} = 0\,\text{V}$

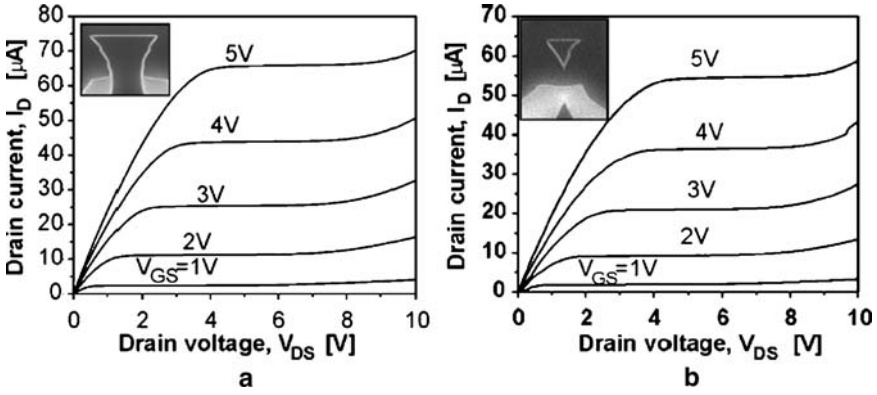

Fig. 2.4 $I_D(V_{DS})$ characteristics for the devices reported in Fig. 2.3

and $V_{DS} = 0.2\,\text{V}$ is around $0.15\,\text{nA}/\mu\text{m}$ for both devices. The reason behind the enhanced current drive of the GAA devices is related to process-induced local tensile strain (bended channel) and mobility enhancement. The flat $I_D(V_{DS})$ characteristics in Fig. 2.4 are also evidence that they do not suffer from self-heating effects because drain and source are connected to the silicon bulk. The absence of any kink in the output characteristics indicates that all devices have a fully depleted body.

Bended Gate-All-Around MOSFET

The bended GAA MOSFET is a new device concept proposed in [7], where the transistor channel is bended by thermal oxidation, introducing the benefits of improved carrier mobility due to the local tensile strain. Figure 2.5 illustrates typical bending as observed in our top-down fabricated nanowire. It is worth noting that bending remains even after fabrication of the gate stack (here 10 nm SiO_2 and 100 nm polysilicon) around the silicon wire.

Micro-Raman spectroscopy has been used for evaluating and confirming tensile strain in our suspended nanowire structures based on a setup adapted for nanoscale measurements developed at the University of Newcastle. Typical measurements showed strain values around 1.5%, which corresponds to approx. 2 GPa, whereas the greatest measured strain is 3.2% ($\sim$4 GPa).

The $I_D(V_{GS})$ characteristics, normalized per effective width, for two bended GAA MOSFETs, compared to that of a nonbended tri-gate device, are shown in Fig. 2.6. The relative current enhancement for device A is a function of gate overdrive varying between 80 and 160% (highest value close to the threshold voltage). Figure 2.7 shows the extracted low field mobility as a function of effective width, W_{eff}, for devices of three different channel lengths. For classical devices there should not be any dependence of the mobility on effective width, which is also what we

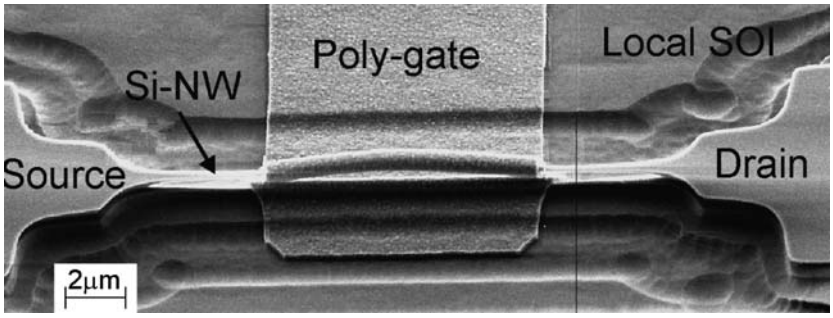

Fig. 2.5 Illustration of bended gate-all-around MOSFET (the poly gate is short-circuited on the two lateral sides to underlying poly line)

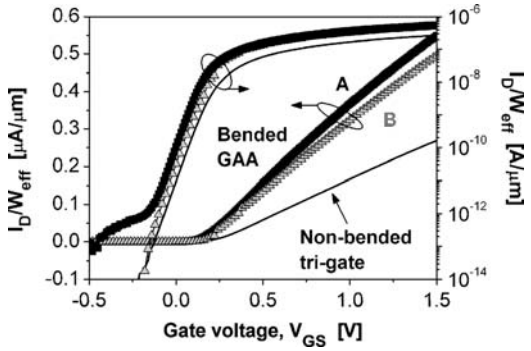

Fig. 2.6 Normalized (per effective width, W_{eff}) drain current, I_{D}, vs. gate voltage, V_{GS}, in bended and nonbended (body-tied tri-gate) nanowire MOSFETs with $L = 5\,\mu\text{m}$, at $V_{\text{DS}} = 20\,\text{mV}$. Effective widths are A: 0.56 μm, B: 0.62 μm and tri-gate: 1.32 μm

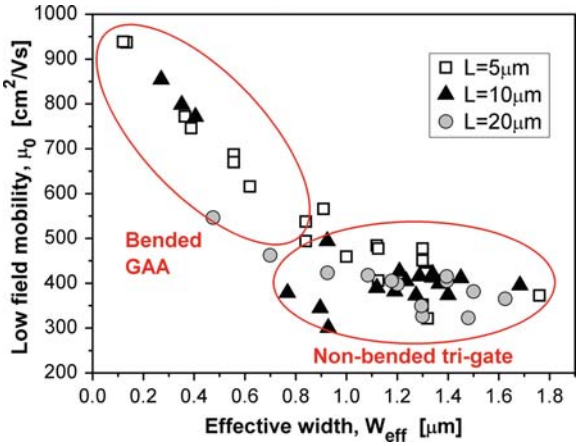

Fig. 2.7 Low-field mobility, μ_0, vs. nanowire cross-section, W_{eff}, highlighting the effect of tensile-strain-induced mobility enhancement in bended structures (for $W_{\text{eff}} < 2\,\mu\text{m}$), at room temperature

can see for the larger nonbended devices. For the smaller bended devices one can observe a rapid increase in the mobility with decreasing dimension. For the smallest devices we see an increase in mobility of around 100%. These findings are well correlated with the Raman strain measurements, where an increase in the tensile strain was observed with decreasing dimension, and tensile strain has been known to cause improvements in the electron mobility of similar magnitude for this amount of strain. This demonstrates that high-mobility channels can be obtained in bended GAA MOSFET.

Impact-Ionization Devices and Inverter on Silicon Rib

The investigated PIMOS device structure is represented in Fig. 2.8a; it is designed as a conventional NMOS, in contrast to a previous I-MOS device [12] that is a reversed biased gated pin structure. PIMOS has a very low-doped body/channel region ($N_A \sim 6 \times 10^{15}\,\mathrm{cm}^{-3}$) and fairly abrupt $N+$ region (arsenic doped, $10^{20}\,\mathrm{cm}^{-3}$). The body of the device is shaped as an X- or tri-gate for small widths, W, and develops gradually into a quasi-planar device for large W. For low drain bias the PIMOS operates as a conventional MOSFET (see $V_{DS} = 0.2\,\mathrm{V}$ in Fig. 2.5b), as V_{DS}'s increased impact ionization will take place at the drain-substrate junction and the drain current will increase rapidly (see $V_{DS} > 8.3\,\mathrm{V}$ in Fig. 2.5b); so far this could resemble the operation of a MOSFET at very high drain bias. However, if at the moment when avalanching sets in the condition of punch-through is met and the device is biased in subthreshold, the particular PIMOS functionality will set in because the electrostatic potential in the channel creates a saddle point in the channel near the drain junction. The electrons generated by impact ionization are swept into the drain junction, whereas the holes can be separated into two fractions. Part of the holes will migrate toward the point of lowest potential, creating a hole pocket at the interface; this also causes a displacement away from the interface of the electron current (Fig. 2.8a). The filling of the hole pocket at the saddle point will result in an increase in the body potential, and thereby a decrease in the local threshold voltage as a function of the drain potential. Another part of the holes constitutes a substrate current, which causes a voltage drop across the substrate resistance that will eventually forward bias the source-substrate junction and turn on the parasitic bipolar structure. The bipolar gain will result in a further amplification of the base (substrate) current, and hence also the channel current. This forms a positive feedback loop on the current, with an abrupt increase in the drain current and thus a steep inverse subthreshold slope.

The hysteresis observed in both the $I_D(V_{GS})$ (Fig. 2.8b) and the $I_D(V_{DS})$ characteristics is due to a combination of the impact ionization under the high drain bias and the positive feedback loop sustained by the BJT action. When the positive feedback loop can no longer be maintained, the drain current will drop suddenly.

Table 2.1 summarizes the main figures of merit of PIMOS compared to the I-MOS (proposed by Stanford University). For this comparison a lateral I-MOS is

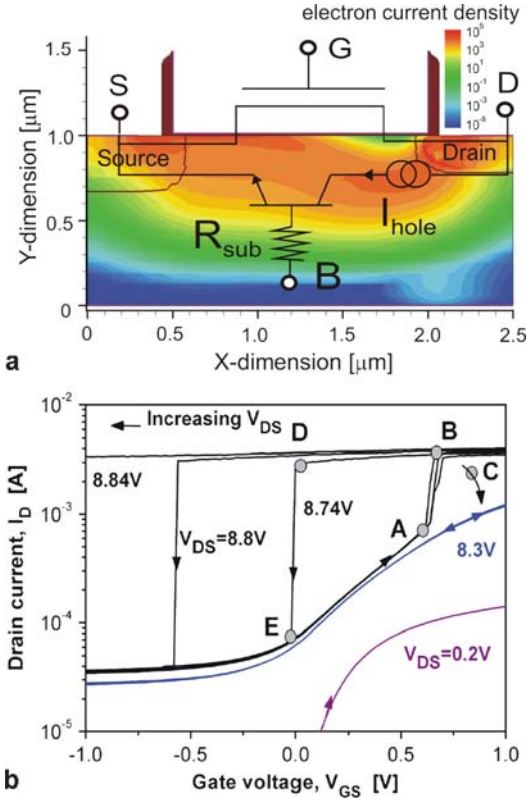

Fig. 2.8 **a** TCAD simulation (DESSIS) showing the electron current distribution at breakdown in a PIMOS device with the schematic of the parasitic bipolar in parallel. The hole pocket at the interface pushes the electron current toward the bulk. **b** Experimental abrupt switching and hysteresis in $I_D(V_{GS})$ for a PIMOS device of $L = 1.4\,\mu m$ and $W = 10\,\mu m$. Increasing V_{DS} widens the hysteresis by displacing the *down* transition $D \rightarrow E$, whereas the *up* transition $A \rightarrow B$ remains more or less fixed. Two curves for normal MOS operation are shown with $V_{DS} = 0.2$ and 8.3 V, respectively

considered, as it is the most closely related in terms of technology and integration with CMOS. The PIMOS fabrication is more closely related to CMOS, and good reliability is also obtained at higher temperatures. The challenges for the PIMOS device are in terms of control of the subthreshold leakage current and the inherent short channel effects. The hysteresis effect can be an advantage for certain applications (memory), but its control, or even elimination, is required for logic applications. The I-MOS, on the other hand, presents a much lower leakage than a corresponding MOSFET, and the scalability in terms of bias voltages is therefore limited by material parameters. The main challenges for the I-MOS are in terms of processing technology and reliability. In planar devices, operation is only assured for a few cycles, but this can be solved by the use of a vertical structure.

Table 2.1 Comparison of main figures of merit of PIMOS and I-MOS

	PIMOS	I-MOS
I_{off}	$I_{\text{leak}} = I_{\text{D0}} e^{-(V_{\text{T}}/S)}$, high	$I_{\text{leak}} = I_{\text{s}} = \left[\frac{eD_{\text{p}}p}{L_{\text{p}}} + \frac{eD_{\text{n}}n}{L_{\text{n}}}\right]$, low
SCE	Inherent	Better than CMOS *off* mode
Slope $I_{\text{off}} \rightarrow I_{\text{on}}$	$<10\,\text{mV/dec}$	$<10\,\text{mV/dec}$
Critical dimension	L_{eff}	$L_{\text{gate}} + L_{\text{I}}$
Processing	Self-aligned	More difficult
Hysteresis	Yes	No
Cycling	$>10^4$ cycles	Few cycles
Substrate	Bulk	SOI
Immunity to I_{sub}	Bad, requires wells	Good, fabricated on SOI
Scalability of V_{BD}	Limited by I_{off}	Limited by material
Ultimate scalability	Limited by I_{off}	Limited by lithography
Temperature stability	Excellent	Unknown

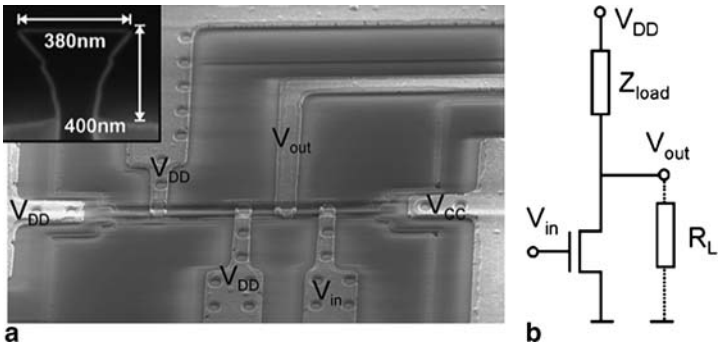

Fig. 2.9 **a** SEM image of NMOS inverter with two-transistor resistive load on a body-tied wire. **b** Equivalent schematic of biasing scheme

We have demonstrated for the first time an N-PIMOS inverter consisting of a PIMOS input device and a pull-up NMOS load (Fig. 2.9), all fabricated on a single etched silicon rib (or body-tied silicon wire with sub-micron cross-section).

The inverter reproduces the abrupt switch and hysteresis from the $I_{\text{D}}(V_{\text{GS}})$ characteristics; the voltage transfer characteristic (VTC) is shown in Fig. 2.10. The PIMOS inverter VTC is different from both that of a conventional CMOS and I-MOS inverters. VTC of PIMOS incorporates three distinct regions of operation: (a) when the input PIMOS device is off, the pull-up network will pass the value of VDD to the output, (b) when $V_{\text{DS}} > V_{\text{DBD}}$ when the input exceeds the gate pull-up voltage, $V_{\text{in}} > V_{\text{GPU}}$, the PIMOS will pull down the output abruptly until it reaches the drain breakdown voltage, and (c) beyond V_{DBD} the device is still on, unlike an I-MOS, it just works as a quasi-conventional short-channel MOSFET at high V_{DS}, after abrupt switching in V_{GS} where the current I_{D} is dictated by both MOSFET and bipolar contributions. So the MOSFET operation will continue to pull down the

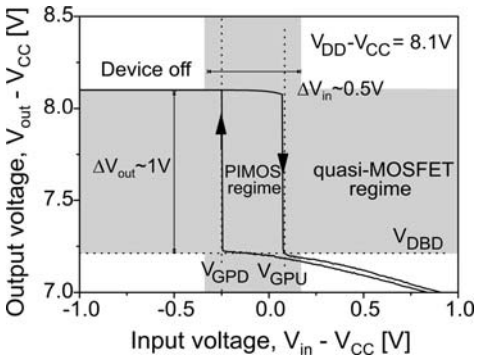

Fig. 2.10 Voltage transfer characteristics of PIMOS inverter reported in Fig. 2.5

output until the point determined by the load network, i.e., a resistive divider in the case of an N-PIMOS.

The hysteretic VTC characteristic in Fig. 2.10 also supports the basic idea of an SRAM cell made of a single inverter (and possible to fabricate on a single etched silicon wire), especially because the hysteresis width can be optimized by the value of applied V_{DS}. However, the main drawback of such a memory cell is the high current consumption. Future prospects should concern the demonstration of a complementary PIMOS inverter to reduce the static power consumption.

Discussion

The work was divided into two distinct topics each dealing with a different issue: (a) mobility enhancement in a GAA architecture and (b) small slope switching based on impact ionization. However, they are united by a common technology platform, which allows for the low-cost fabrication of 3D devices with sublithographic dimensions. Another common feature is that all these devices can be described as true 3D structures, because of their nonplanar geometry and 3D electrostatic effects.

We have addressed the issue of strain-induced mobility enhancement in silicon nanowires. By bending the wire as a result of one or more sacrificial oxidation steps we have demonstrated a bended MOSFET with tensile strain on the order of 1 to 3% and a mobility improvement of up to 100%.

We have proposed a punch-through impact-ionization device (PIMOS) based on a low-doped MOSFET structure operated in subthreshold under punch-through conditions. With this device we obtain abrupt switching transients of less than 10 mV/dec due to the impact-ionization mechanism. In addition, as a result of the inherent parasitic bipolar action, we observe a bias-dependent hysteresis in both the $I_D(V_{DS})$ and $I_D(V_{GS})$ characteristics. We have demonstrated an abrupt hysteretic inverter based on the PIMOS $I_D(V_{GS})$ hysteresis. The N-PIMOS inverter has three operating regions; off, PIMOS mode, and normal MOSFET mode.

Ferroelectric FET with Sub-100-nm Copolymer P(VDF-TrFE) Gate Dielectric for Nonvolatile Memory

The quest for universal memory featuring high density, fast operation, and low power involves a large diversity of memory candidates such as MRAM (Magnetic RAM), PCRAM (Phase Change RAM), Fe-RAM (ferroelectric RAM), and molecular memories. Recently the ferroelectricity of some ultrathin films has been shown to be a good candidate for nonvolatile memory thanks to the bistability of polarization [13–19]. In ferroelectric materials, the electrical dipoles orientate according to an applied external field, and, after reaching a critical electric field, the resulting orientation can be maintained even when the field is switched off. This mechanisms can be used to store charges and therefore to store information for nonvolatile memory applications.

Standard ferroelectric materials like strontium–barium–titanate (SBT) and lead–zirconium–titanate (PZT), employed in some commercial Fe-RAM, still have problems in terms of film quality and retention time [20, 21]. Moreover these perovskite ferroelectrics require high-temperature annealing, which makes them incompatible with CMOS coprocessing. Recently, vinylidene fluoride (VDF) and copolymer with trifluorethylene (Tr-FE) have been attracting growing interest because of their large spontaneous polarization ($\sim 0.1\,\mathrm{C/m^2}$), polarization stability, switch time ($<0.1\,\mu\mathrm{s}$), and suitability for organic devices [17]. Several P(VDF-TrFE) bistable capacitors have been reported with high operating voltages (tens of volts) and good retention times, while the very few low-operating-voltage devices showed reduced low retention ($\sim$15 min). In this work, we concentrate our efforts on the processing and study of the properties of ultrathin P(VDF-TrFE) films when integrated in the gate stack of a MOSFET, which could operate as a one-transistor (1T) memory cell as they would be more scalable than conventional 1T–1C memory architectures using ferroelectric capacitors.

Fe-FET Fabrication

The proposed process targets the use of sub-100-nm ultra-thin-layer PVDF copolymers in the gate stack of n-channel MOSFET on bulk silicon. Device active areas and STI isolation are UV-lithographically defined on p-doped silicon. Two different substrates have been used: a low-resistivity ($N_\mathrm{A} = 4 \times 10^{16}\,\mathrm{cm^{-3}}$) wafer for 40 nm P(VDF-TrFE) and a high-resistivity one for 100 nm P(VDF-TrFE) ($N_\mathrm{A} = 10^{15}\,\mathrm{cm^{-3}}$). Source and drain regions are highly doped ($10^{20}\,\mathrm{cm^{-3}}$) and 10 nm of SiO_2 is thermally grown. The P(VDF-TrFE) (70–30%) is prepared using an original recipe, similar to a recent report [22] based on methyl-ethyl-ketone, optimized to considerably reduce the film thickness (into the sub-100-nm range) and, consequently, the voltage for coercive field. The solution is spin-coated and baked for 5 min at 137°C. Two polymer layer thicknesses, of 100 and 40 nm, are studied.

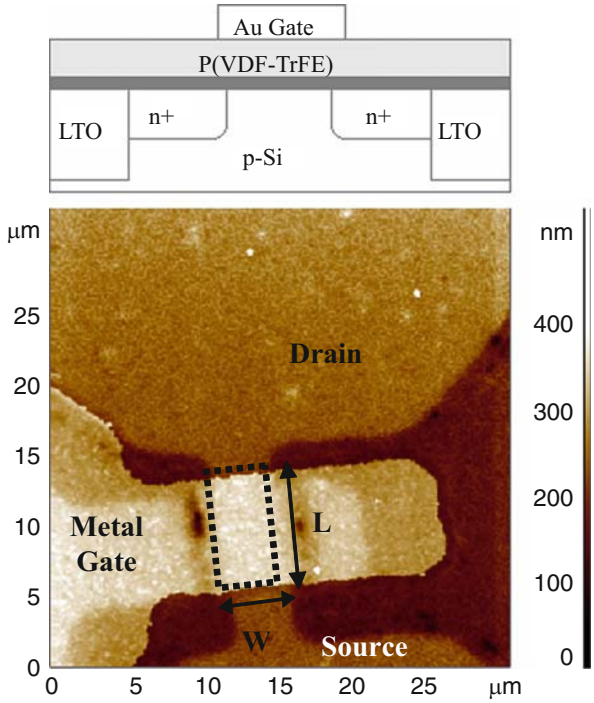

Fig. 2.11 *Top*: Cross-section of fabricated Fe-FEt. *Bottom*: high-resolution AFM image of PVDF-TrFE gate stack of fabricated Fe-FET. The average roughness is 38 nm (which limits the realization of films thinner than 40 nm)

Atomic force microscope (AFM) measurements have been systematically used to evaluate the topography of the copolymer films and optimize their preparation. A thin gold layer (100 nm) defines the gate contact. MOSFET devices with different channel lengths, L, and widths, W, ranging from 2 to 50 µm, have been designed; a fabricated device is shown in Fig. 2.11.

Experimental Results

The measurements of the polarization and of the capacitance on the gate stack of the fabricated Fe-FET prove that the polymer has been successfully integrated onto a silicon substrate. In fact, the hysteretic loop indicates that the ferroelectric properties of the material are preserved following the fabrication process. Figure 2.12 shows the polarization for two different samples: the first with only a P(VDF-TrFE) gate layer and the second with a SiO_2/P(VDF-TrFE) gate stack. Both samples have a ferroelectric layer of 100 nm. The different bending of the curves is due to the drop in voltage on the SiO_2 layer in the second sample. The P(VDF-TrFE) polymer has

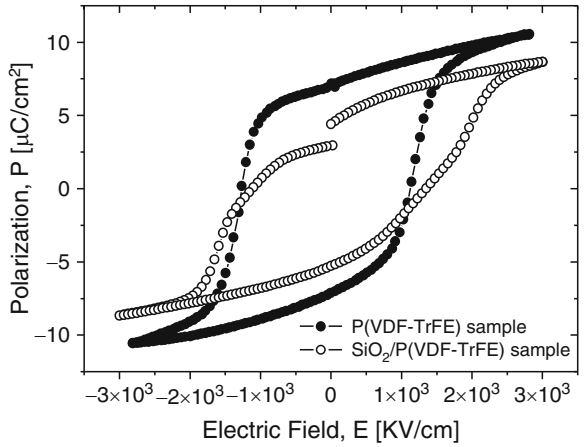

Fig. 2.12 Polarization measurements on two Fe-FET gate stacks: with and without SiO2 layer for a device with $L = W = 50\,\mu\text{m}$

a remanent polarization (Pr) of about $8\,\mu\text{C/cm}^2$ and a coercive field (E_c) of about $1.3\,\text{MV/cm}$.

At first view, the output characteristics, I_D–V_D, of the Fe-FET show linear and saturation regions qualitatively comparable with those of a constant gate oxide capacitance MOSFET (Fig. 2.13). However, there is a combined effect of V_G and V_D on the gate polarization (and consequently on the value of the gate-to-channel capacitance), which influences the buildup of inversion charge and the saturation voltage V_Dsat in a more complex manner than the established equations for a standard MOSFET, which also depend on device size and geometry.

The I_D–V_G electrical characteristics are evaluated for both 100- and 40-nm ferroelectric layers, showing that, like conventional MOSFET, the gate voltage controls the drain current. An equivalent threshold voltage exists, with a very abrupt transition between the off and on states and an associated hysteresis. The memory effect needed for the 1T-cell is clearly demonstrated by the hysteretic loops reported at room temperature in Fig. 2.13a, b. In the case of 40-nm PVDF-TrFE the I_on/I_off is of the order of 10^5 to 10^6 (depending on the applied V_D) and the off-state current is less than 10^{-12} A. We explain the saturation of the drain current by the saturation of the polarization.

The saturation of the drain current is reached at around 10 V for the 40-nm dielectric (Fig. 2.4), less than half of the voltage needed for a thickness of 100 nm. These values are in good agreement with theory relating the voltage to the coercive field (E_c) and ferroelectric dielectric thickness; in fact the saturation voltage V_sat is given by $V_\text{sat} = E_\text{c}d$, where d is the layer thickness and E_c is the coercive field. For the 100-nm thickness we found a V_sat of about 15 V, and for the 40-nm case its value drops to 7 to 8 V, these theoretical values fit well the experimental ones. Moreover, from these results it is observed that the coercive field E_c is almost the same for both 100- and 40-nm thicknesses.

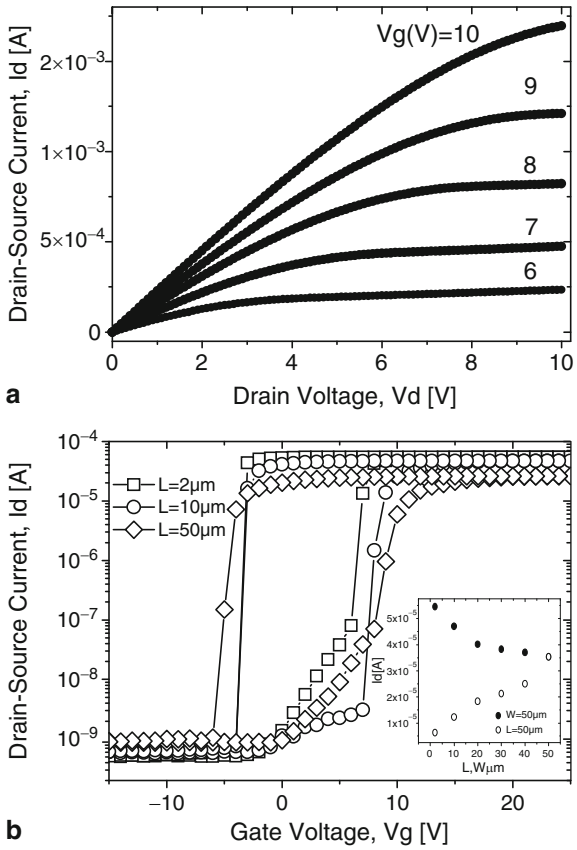

Fig. 2.13 **a** Output characteristics, I_D–V_D. **b** Transfer characteristics, I_D–V_G, for a Fe-FET with 100-nm P(VF-TrFE) in gate stack and $L = W = 50\,\mu m$

The comparison of the I_D–V_G characteristics of 40- and 100-nm PVDF-TrFE transistors, with the same design ($L = W = 10\,\mu m$), demonstrates significant improvement in terms of memory operating voltage (hysteresis) for the 40-nm polymer thickness (Fig. 2.14). While the I_{off} current difference (cf. $I_{off} \sim 10^{-9}$ A, in Fig. 2.13b with $I_{off} \sim 10^{-11}$ A, in Fig. 2.14, for the same device width) is mainly due to the difference in the substrate doping levels; the I_{on} reduction for the 40-nm thickness is explained by a more diluted solution that results in a ferroelectric polymer material with less polarization.

The Fe-FET has also been characterized in terms of memory properties: retention time, endurance, and programming time [23]. The experiments show an $I_D(V_G)$ hysteresis fairly symmetric with respect to 0 V, enabling an efficient read operation. In fact the binary values (0 or 1) stored in the 1T Fe-FET cell can be read out at $V_G = 0$ V (Fig. 2.15). Retention analysis has been performed by applying to the gate a 20-V pulse signal with a width of 30 s and measuring the drain current. Figure 2.15

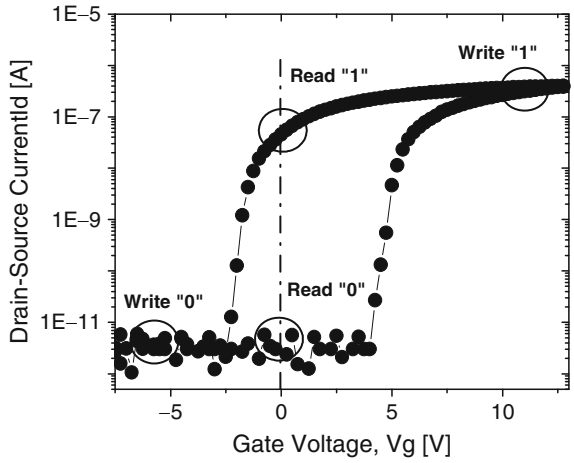

Fig. 2.14 I_D–V_G characteristics and programming regions for a Fe-FET device operated as 1T memory cell

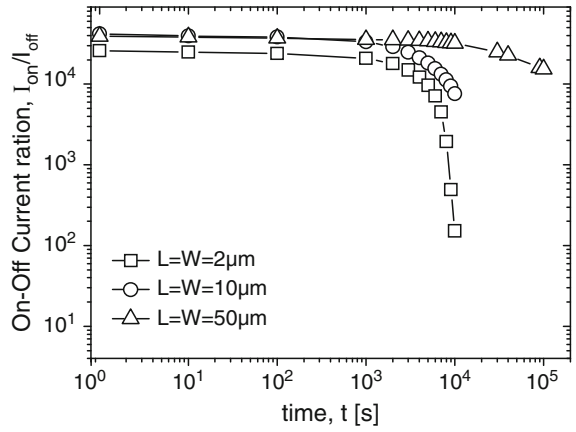

Fig. 2.15 Retention time of 1T Fe-FET memory cell with 100-nm polymer thickness, after writing the high state "1" with $V_g = 20$ V for 30 s, at room temperature

shows the change in the I_{on}/I_{off} ratio as a function of time. The largest Fe-FET ($L = W = 50\,\mu$m) has a retention time of about 2 d, while the smallest one ($L = W = 2\,\mu$m) of about 3 h; retention time dependence on device size is under investigation. This dependence has already been observed in PZT/SBT ferroelectric capacitors. In a number of publications, the switching polarization loss was attributed to the lateral damage provoked by etching [18] or electric field nonuniformity at the Fe-CAP edges [24]. A preferential polarization state observed in very small Fe-CAPs was explained by the accumulation of defects at the lateral surface [25]. In most recent works it was demonstrated that the size effects consist not only of a

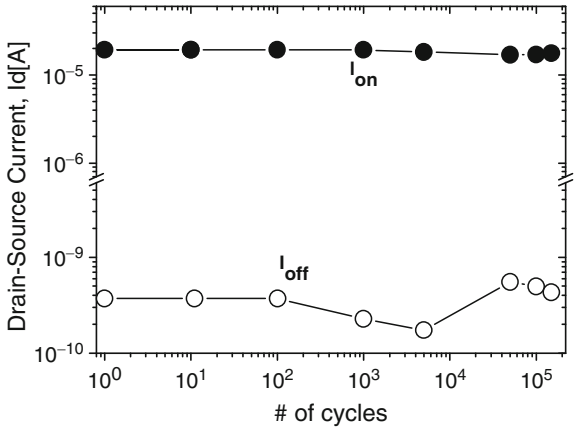

Fig. 2.16 Experimental endurance of 1T Fe-FET memory cell with 100-nm polymer thickness; the gate is cycled with 20Vpp square signal, and I_{on} and I_{off} are evaluated after each decade of cycles

decrease but also of a redistribution and even inversion of the original spontaneous polarization [26].

Finally, typical 1T memory endurance experimental analysis has been performed and is reported in Fig. 2.16; after 10^5 cycles, both I_{on} and I_{off} current levels are well preserved, suggesting the suitability of the investigated new material for nonvolatile memory cells.

Discussion

We have integrated for the first time a P(VDF-TrFE) copolymer into the gate stack of a standard MOSFET structure and demonstrated a fully operational 1T nonvolatile memory cell. Devices with two different copolymer thicknesses (40 and 100 nm) have been characterized and a memory window of 6 V has been found for the thinner dielectric. The I_{on}/I_{off} ratio of fabricated Fe-FETs is in the order of 10^5, with I_{off} currents ranging from 10^{-11} to 10^{-9} A. The Fe-FET memory cell has a retention time of about a few days, a good endurance (10^5 cycles demonstrated), and a programming time on the order of milliseconds (due to the micrometer size of the fabricated devices). These performances make the 1T Fe-FET memory cell suitable for any nonvolatile memory application requiring a storage time of some days, with an associated low cost. Future work is foreseen to improve the retention characteristics of the reported memory cell and to develop accurate modeling for the Fe-FET electrical operation.

Materials for Piezoelectric Nanodevices

Recent examples of piezoelectric materials in polymer matrix show that sensors have established a solid presence in our daily lives from ultrasound applications in medicine, to underwater ultrasound in military and civilian applications, to smart sensor systems in automobiles, or to nondestructive testing in industry. Since the 1950s, lead titanate ($PbTiO_3$) compounds have been the leading materials for piezoelectric applications due to their excellent dielectric and piezoelectric properties. The rugged solid-state construction of industrial piezoelectric ceramic sensors enables them to operate under most harsh environmental conditions. However, the production of piezoelectric nanowires and their applications are still very challenging.

With the increasing public awareness of health concerns associated with lead and the recent changes in environmental policies, we have focused our research on $KNbO_3$-based nanowires. Alkali niobate materials with a perovskite-type structure are believed to be the best candidates to replace piezoelectric lead-containing materials. On the other hand, $KNbO_3$ is a photocatalyst with E_g of about 3.3 eV. $KNbO_3$ nanowire arrays could be suitable materials to compete with TiO_2 for the production of H_2 by water splitting in a new generation of photocatalytic cells.

Composite $KNbO_3$ *Nanowires: Epoxy Resin for Piezoelectric Devices*

Single-crystal $KNbO_3$ nanowires are grown by hydrothermal treatment from a mixture of Nb_2O_5 and highly concentrated KOH solution [27]. After optimizing the growth conditions [27] and studying the kinetics of the chemical reactions [28], we have modified the method to produce a 1×1 cm carpet of $KNbO_3$ nanowires epitaxially grown on a [001] $SrTiO_3$ substrate [29] (Fig. 2.17). As previously reported (see 2007 CCMX interim report), the morphological characteristics (length, diameter, etc.) and density of nanowires strongly depend on the roughness of the $SrTiO_3$ substrates. It is believed that structural defects induced by the polishing process on the substrate surface act as nucleation sites for the crystallization of the $KNbO_3$ nanowires.

The nanowire arrays are subsequently embedded in a polymer matrix by immersion in an epoxy resin and the composite is easily peeled off from the $SrTiO_3$ substrate. Excess polymer is removed by gentle polishing. Gold is subsequently evaporated on both sides of the composites. Innumerous samples, with approximate dimensions of $500 \times 500\,\mu$m and 50μm thickness, were prepared and the piezoactivity was measured by placing the sample inside a pressure cell that was connected to an electrometer measuring charge, and hydrostatic pressure up to 3.5 kbar was applied. The signal of a strain gauge measuring the applied force and

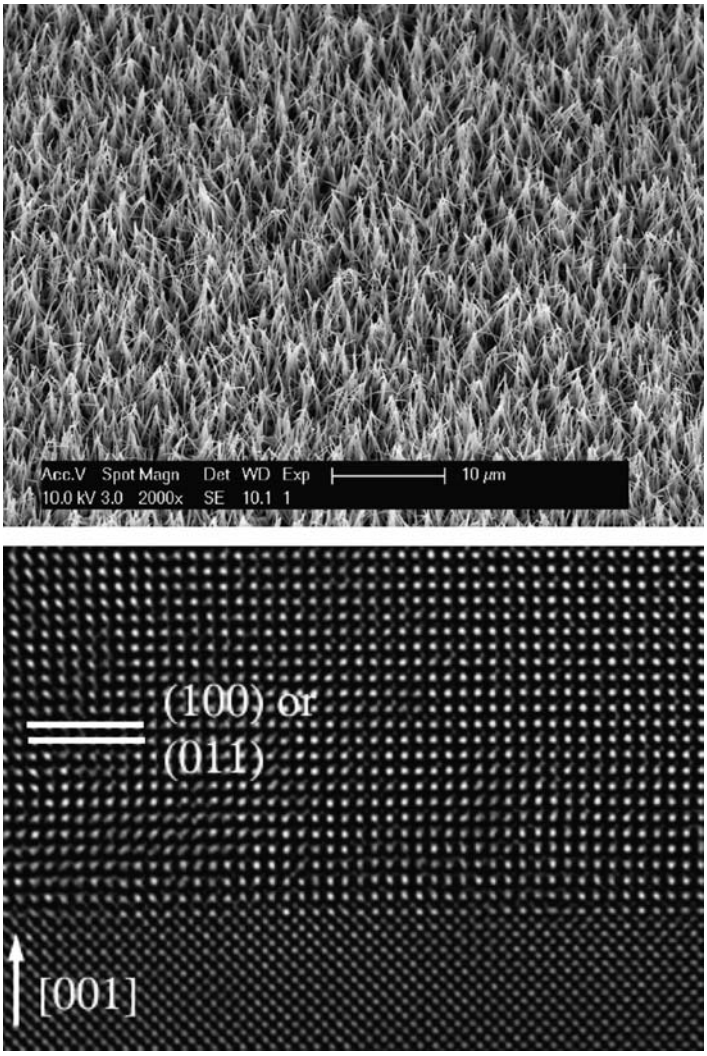

Fig. 2.17 SEM images of $KNbO_3$ nanowires carpet grown on $SrTiO_3$ substrates and HRTEM of the $SrTiO_3$–$KNbO_3$ interface

the analog output of the electrometer were recorded with an oscilloscope. Several charge-discharge curves were measured (Fig. 2.18).

Although these results are very encouraging, the measured piezoactivity of the composite differs significantly from the value calculated from the bulk $KNbO_3$ piezoelectric coefficient, which is on the order of 10 pC/N [30]. Actually, the $KNbO_3$ nanowires are multidomain with a random polarization direction. Additional investigations are being carried out while applying an electric field to polarize entirely the nanowire along their axis prior to the application of pressure.

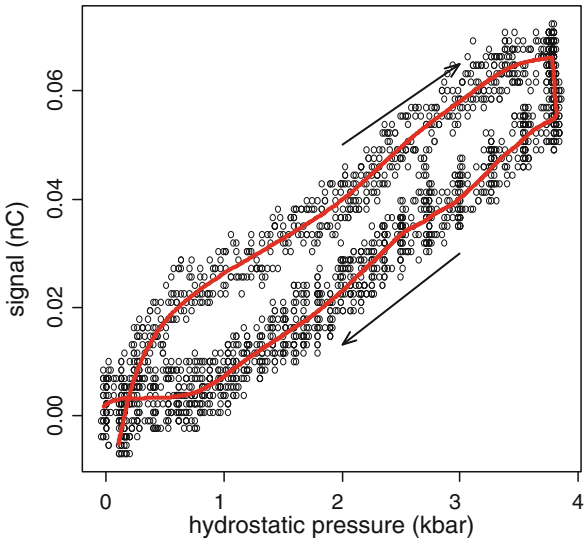

Fig. 2.18 Piezoelectric hysteresis loop obtained from $KNbO_3$ nanowires – epoxy composites. *Arrows* indicate direction of scan. Original data points are indicated by *symbols*, *solid line* is a guide for the eye

Water Splitting Photocatalyzed by $KNbO_3$ Nanowires: Discussion

In order to investigate the photocatalytic activity of $KNbO_3$ nanowires, we have implemented an electron spin resonance (ESR) technique to detect and quantify singlet-oxygen generation. Regarding the photosynthesis process, H_2 is formed via light-stimulated exciton generation in the bulk of the $KNbO_3$ nanowires. Excitons can be understood as *e–h* pairs. The extra, light-induced electrons in the conduction band are needed to initiate the H_2 formation process at the particle surface. Therefore, the evidence of singlet-oxygen generation will be closely related to the effective exciton formation under stimulation with UVA. Thus, it gives a good prognostic for H_2 formation.

The preliminary results of our ESR investigations are plotted in Fig. 2.19. The linear evolution of the ESR signal intensity vs. time shows the ability of $KNbO_3$ nanowires to generate singlet oxygen. However, this production is still reduced compared to TiO_2 films.

As perspectives, the photocatalytic activity will be tentatively enhanced by decorating the $KNbO_3$ nanowire surface with cocatalyst Ni/NiO particles, which are known to work as an H_2 evolution site. In addition, the ESR analysis will be combined with mass spectrometry to substantiate the correlation between singlet-oxygen generation and H_2 evolution.

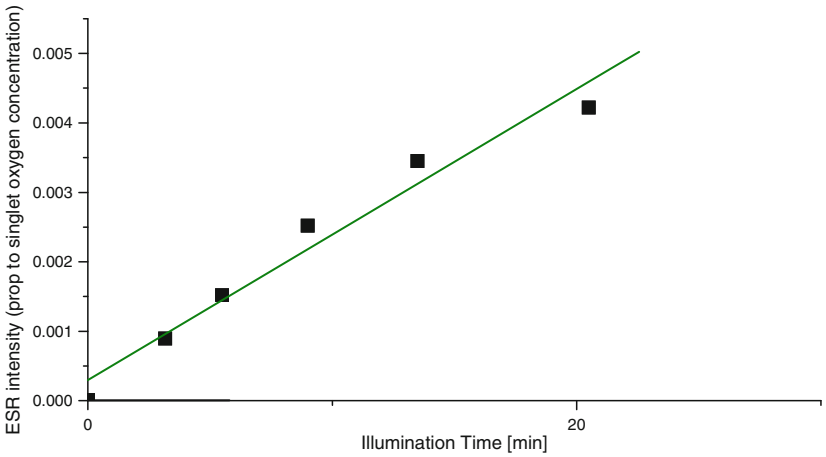

Fig. 2.19 Evolution of ESR signal intensity, proportional to the singlet oxygen concentration generated by illumination of the $KNbO_3$ nanowires with UVA

Conclusions

Various materials have been shown to be very relevant for the construction of nanoelectronic circuits. The synergy between material choice and electronic design is extremely important especially in view of achieving the desirable electrical and mechanical properties. To date, a large number of materials have been used in micro- and nanoelectronics, but a broad range of opportunities remain untapped.

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