CMOS Neurotransmitter Microarray: 96-Channel Integrated Potentiostat With On-Die Microsensors

Meisam Honarvar Nazari, *Student Member, IEEE*, Hamed Mazhab-Jafari, *Student Member, IEEE*, Lian Leng, Axel Guenther, and Roman Genov, *Senior Member, IEEE*

***Abstract*—A 8×12 array of integrated potentiostats for on-CMOS neurotransmitter imaging is presented. Each potentiostat channel measures bidirectional redox currents proportional to the concentration of a neurochemical. By combining the current-to-frequency and the single-slope analog-to-digital converter (ADC) architectures a total linear dynamic range of 95 dB is achieved. A 3.8 mm $\times$ 3.1 mm prototype fabricated in a 0.35 μm standard CMOS technology was integrated with flat and 3D on-die gold microelectrodes and an on-chip microfluidic network. It is experimentally validated in in-situ recording of neurotransmitter dopamine.**

***Index Terms*—Dopamine, gold microelectrode, microfludic network, neurochemical imaging, potentiostat.**

I. Introduction

In brain neurochemistry, dysfunctions of neurotransmitters such as dopamine, glutamine and serotonine have been linked to neurological disorders such as stroke, Parkinson's and Alzheimer's diseases. Neurotransmitters play a key role in neural communication. When an action potential in a pre-synaptic neuron arrives to a synapse, neurotransmitters are released into the synaptic cleft. The neurotransmitters diffuse to the post-synaptic neuron and bind to its receptors. This triggers an electrical signal in the post-synaptic neuron, thus enabling neuron-to-neuron messaging.

Measuring neurotransmitter concentration in vivo facilitates studies of various neurological disorders in order to identify new treatments but may be prohibitively slow and risky [1]. Imaging neurotransmitters in vitro, such as in cell cultures and brain slices, yields a fast and low-risk platform for early-stage high-throughput drug screening and drug discovery. Currently available techniques for neurotransmitter imaging such as chemiluminescent imaging, liquid chromatography, and PET and SPECT imaging are expensive and utilize bulky equipment.

Manuscript received December 10, 2011; revised March 08, 2012; accepted May 07, 2012. Date of publication August 10, 2012; date of current version May 22, 2013. This work was supported by National Sciences and Engineering Research Council of Canada (NSERC). This paper was recommended by Associate Editor T. Constandinou.

M. H. Nazari was with Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada. He is now with the California Institute of Technology, Pasadena, CA 91125 USA.

H. Mazhab-Jafari and R. Genov are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: roman@eecg.utoronto.ca).

L. Leng and A. Guenther are with the Department of Mechanical and Industrial Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2012.2203597

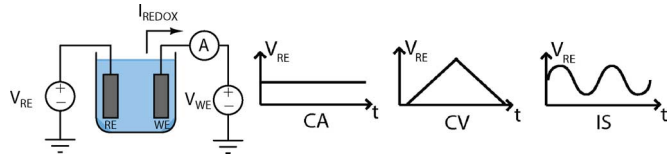


Fig. 1. Potentiostat circuit principle of operation in three sensory methods: constant potential amperometry (CA), cyclic voltammetry (CV) and impedance spectroscopy (IS).

In recent years amperometric integrated circuits [2]–[4] have been gaining popularity in monitoring the neurotransmitter activity [5], [6] due to their low cost and small form factor.

In electrochemical amperometric microsystems, the concentration of a neurochemical can be measured by a potentiostat circuit, as shown in Fig. 1. The potentiostat measures the current through the working electrode (WE) held at a fixed potential. The reference electrode (RE) is set to a constant voltage for constant-potential amperometry (CA), a bidirectional ramp voltage for cyclic voltammetry (CV), or a small-amplitude sinusoid for impedance spectroscopy (IS). CA can yield high sensitivity at the cost of poor selectivity, CV can be highly selective but with lower temporal resolution, and IS is suitable for applications where chemical reactions result in unique changes in the impedance spectrum of the working electrode but requires long time for the spectral analysis.

Low concentrations of neurochemicals result in pA-level input currents. The direction of the current is determined by the type of the chemical reaction, reduction or oxidation. An offset current arising from the chemical reactions at the electrode surface can be as high as a few hundred nanoamperes. As a result a potentiostat has to cover over 80 dB dynamic range of a current-mode input while maintaining the accuracy at the picoampere level. Another requirement in designing an integrated potentiostat is the high sampling rate. In cyclic voltammetry, due to the varying potential applied to the reference electrode, the redox current changes fast during the recording period. For instance, the reference potential required to detect dopamine (an important neurotransmitter in the brain) changes with a sweep rate of 300 V/s which corresponds to a sampling rate of a few hundreds of Hz, considered high for a potentiostat. Power dissipation is another important design constraint. When sensors are fabricated on a die, heat dissipation should be such that a sample analyte is not heated by more than a few degrees Celsius, necessitating a mW-level power budget [8].

A number of integrated potentiostats for single-chip amperometry have been reported. Earlier implementations [9]–[11] have one recording channel. The design in [9] measures redox

currents in a narrow 0.1 μA to 3.5 μA range. The potentiostat presented in [10] resolves currents as small as 100 fA at the cost of consuming 5 mW of power. The potentiostat in [11] records a bidirectional input current in the range of 0.1 nA to 0.5 μA corresponding to 74 dB input dynamic range. A wireless potentiostat with programmable sensitivity which trades with the sampling rate of up to 100 Hz is reported in [12]. The potentiostat in [13] is employed as a patch-clamp amplifier with a pulse modulated output ranging from 3 Hz to 10 MHz for detecting input currents as small as 1 pA while consuming more than 5.5 mW of power.

Multi-channel potentiostats enable recording chemicals at different locations and provide a much needed neurochemical imaging functionality. Channel compactness is critical here as a higher channel count translates into higher neurochemical image spatial resolution. A 9-channel integrated potentiostat with on-chip electrodes in [14] occupies 9 mm^2 of silicon area and measures redox currents down to 10 pA. In [5], [15], [16] three integrated potentiostat designs with 16 channels are presented. These potentiostats use an array of off-chip electrodes for chemical recording and support a low sampling rate. A 42-channel integrated potentiostat in [17] has 50 fA sensitivity at the cost of a sampling rate in the range of a few Hz. The design in [18] is comprised of 128 channels for DNA detection which measure input redox currents as small as 1 pA with a conversion time of several seconds. The reported potentiostats have typically been demostrated in one of the sensory methods depicted in Fig. 1.

We present a 96-channel single-ended integrated potentiostat array fabricated in a 0.35μm standard CMOS technology that implements all three sensory methods to simultaneously measure concentrations of multiple neurochemicals, as many as one per channel, directly on the die. This paper extends on an earlier report of the principle and demonstration in [19], and offers a more detailed analysis and expanded experimental results. Each channel is comprised of a low-noise current conveyor followed by an analog-to-digital converter (ADC). Both a wide dynamic range (95 dB) and a high sampling rate (up to 1 ksps) are achieved by combining the current-to-frequency and the single-slope analog-to-digital conversion architectures. They reuse the same circuit components, which results in a compact and low-power implementation.

This work targets two main applications: neurotransmitter imaging in cell cultures and in brain slices. On-chip microelectrodes organized in a 200 μm-pitch array allow for electrochemical imaging directly on the CMOS die. For the cell culture imaging application, bio-compatible on-die flat microelectrodes have been fabricated as shown in Fig. 2(a). In brain slice studies, a region of the brain is extracted and sliced. As a result, the slices have a layer of dead tissue which needs to be penetrated by recording microelectrodes. For this purpose 3D gold microelectrodes have also been fabricated on the CMOS die as depicted in Fig. 2(b). On-die gold micro-sensors yield high sensitivity and selectivity, eliminate the need for costly excessive wiring and minimize the interference noise. A low-cost microfluidic network integrated with the CMOS potentiostat array allows for per-channel pharmacological agent sample delivery, provides for faster analysis and response times and a better overall process control. The rest of the paper is organized as follows. Section II presents the top-level VLSI architecture of the 96-channel integrated potentiostat. Section III details the circuit implementation of the VLSI architecture. Section IV demonstrates the electrical experimental results obtained from a 0.35 μm CMOS prototype of the integrated potentiostat. In Section V results of chemical sensing experiments in neurophysiology applications are presented.

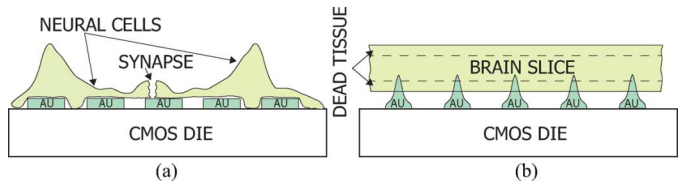


Fig. 2. Cross-section of a microsystem for mapping concentration of neurotransmitters in-vitro in (a) cell cultures and (b) brain slices.

II. Channel VLSI Architecture

The top-level VLSI architecture and the timing diagram of one channel of the integrated potentiostat are shown in Fig. 3(a) and (b) respectively. A current conveyor at the front end of each channel maintains the working electrode at a fixed potential, V_{WE}, as needed to induce a redox reaction. An integrating ADC quantizes the resulting voltage and outputs a corresponding digital word, D_{OUT}.

The in-channel ADC architecture combines two analog-to-digital conversion techniques, the current-to-frequency ADC and the single-slope ADC, which share and reuse the same circuit components. Given the sensory signal specifications as well as the power and area requirements described in Section I, this dual-mode ADC architecture is well suited for this application as it yields both a wide dynamic range and short conversion time as well as a compact and low-power circuit implementation.

The proposed ADC architecture has been inspired by wide-dynamic-range CMOS image sensors VLSI architectures [20], [21]. In this work the circuit implementation is optimized for chemical sensing applications. A current conveyor at the front end keeps the working electrode at the redox voltage. Additionally pulse-shaping circuit has been introduced to fully discharge the integrating capacitor since the size of the integrating capacitor is much larger than the size of the capacitors in image sensors.

The analog-to-digital conversion is performed in two phases as detailed in Fig. 3(c) and (d). In the first, current-to-frequency analog-to-digital conversion phase shown in Fig. 3(c) the input current charges the integrating capacitor, C_{INT}. When the voltage on the capacitor reaches the max voltage, V_{REF}, the comparator generates a pulse that discharges the capacitor through the reset switch. This process is repeated. The input current relates to the number of pulses at the output of the comparator as

$$I_{IN} = \frac{N_{MSB}\, C_{INT}\, V_{REF}}{T_{phase1}} + \Delta I \tag{1}$$

where I_{IN} is the input redox current, ΔI is the residue current which is resolved in the second phase, T_{phase1} is the duration

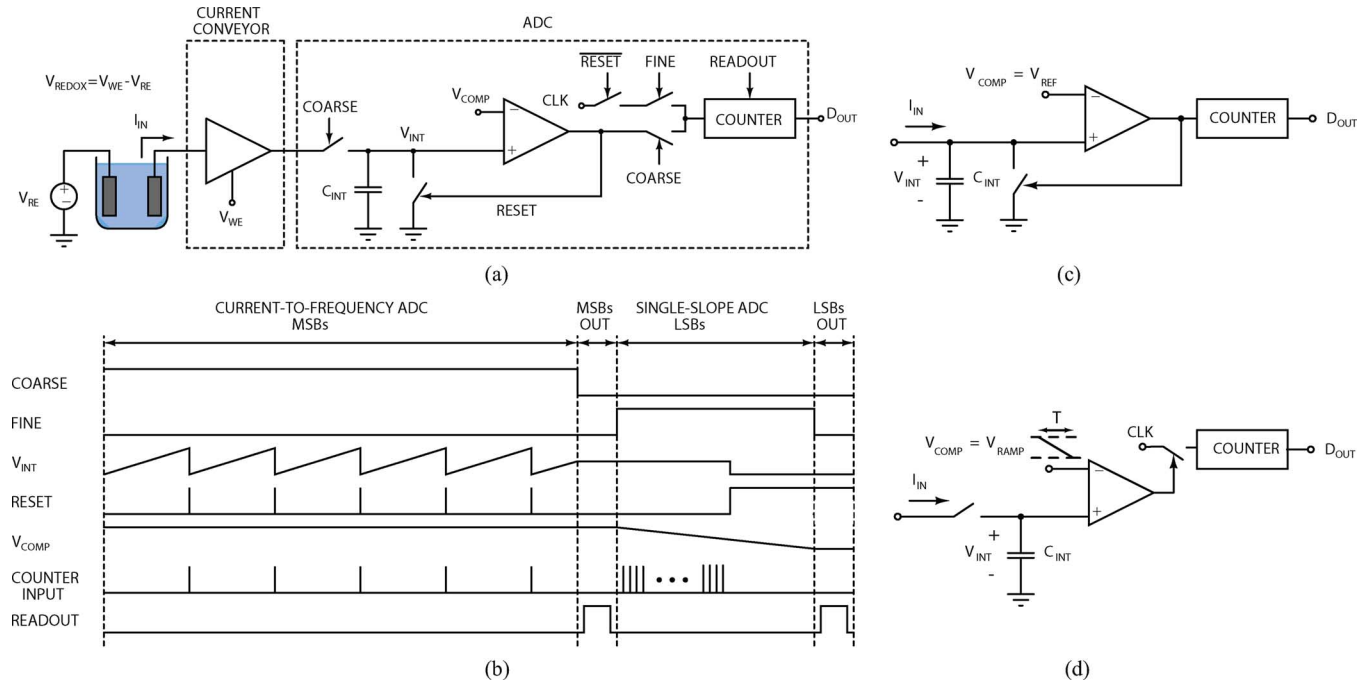


Fig. 3. (a) Top-level VLSI architecture of one channel of the integrated potentiostat, and (b) timing diagram of the dual-mode ADC. (c) VLSI architectures of the current-to-frequency analog-to-digital conversion phase, and (d) of the single-slope analog-to-digital conversion phase.

of phase one, N_{MSB} is the number of pulses at the input of the comparator during the first phase, C_{INT} is the integrating capacitance, and V_{REF} is the comparator reference voltage. A wide input dynamic range is achieved as data conversion is performed in the time domain. This comes at a cost of a longer conversion time, as for a low input current, a long time is needed to charge the integrating capacitor.

To eliminate this trade-off, the single-slope ADC architecture [18] is employed in the second phase of the data conversion, as shown in Fig. 3(d). The single-slope ADC has a higher sampling rate for small input currents than that of the current-to-frequency ADC. At the beginning of the second phase, the voltage across the capacitor is the residue voltage of the first phase. It is compared with a ramp reference voltage (generated using an on-chip in-channel DAC), V_{RAMP}. Once the reference voltage reaches the capacitor voltage, the counter stops counting. The voltage across the capacitor at that instance is calculated as

$$V_{INT} = N_{LSB}\left(\frac{T_{CLK}}{T_{phase2}}\right)V_{REF} \tag{2}$$

where T_{CLK} is the clock period, N_{LSB} is the output of the counter at the end of the second phase, and T_{phase2} is the duration of the second phase. Solving (1) and (2) together results in

$$\begin{aligned} I_{IN} &= C_{INT}\frac{N_{MSB}V_{REF}+V_{INT}}{T_{phase1}} \\ &= \frac{C_{INT}N_{MSB}V_{REF}}{T_{phase1}} + \frac{C_{INT}}{T_{phase1}}V_{INT} \end{aligned} \tag{3}$$

where the residual current is given by

$$\Delta I = \frac{C_{INT}}{T_{phase1}}V_{INT}. \tag{4}$$

T_{phase2} can be expressed in terms of the number of bits generated in the second phase, M, as

$$T_{phase2} = 2^M \times T_{CLK} \tag{5}$$

resulting in the following expression for the input residual current:

$$\Delta I = \left(\frac{C_{INT}}{T_{phase1}}\right)\left(\frac{N_{LSB}}{2^M}\right)V_{REF}. \tag{6}$$

The single-slope ADC architecture achieves high accuracy but does not support a wide range of input currents because for high currents the capacitor voltage goes beyond the reference voltage. The two architectures, the current-to-frequency ADC and the single-slope ADC, are combined to break the dynamic range and sampling rate trade-off. The current-to-frequency conversion performed in phase one covers a wide dynamic range of input currents. If the input current is low, it may not generate an output pulse in phase one given a limited conversion time. Such a low current results in the MSBs equal to zero. In the second phase the capacitor voltage corresponding to the low-level current is accurately resolved by the single-slope ADC. As a result, both a wide dynamic range and a high sampling rate are achieved. The outputs of the two phases are related to the input current as

$$I_{IN} = \frac{C_{INT}V_{REF}}{T_{phase1}}\left[N_{MSB} + \frac{N_{LSB}}{2^M}\right]. \tag{7}$$

III. Circuit Implementation

This section describes the circuit implementation of the VLSI architecture of the potentiostat described in Section II. Fig. 4(a) depicts the schematic diagram of one channel of the integrated potentiostat. Each channel is comprised of a current conveyor

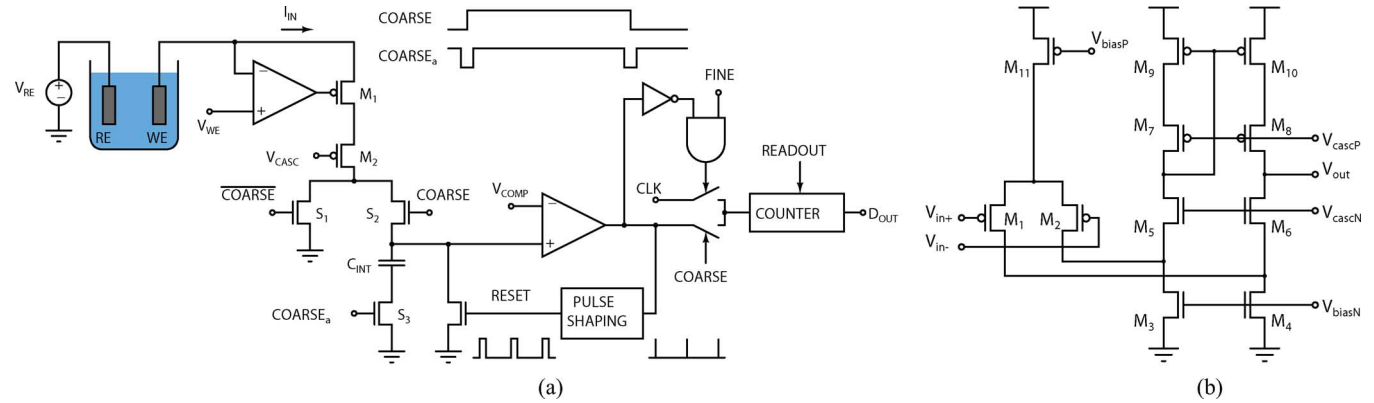


Fig. 4. (a) Circuit diagram of one channel of the integrated potentiostat. (b) Folded-cascode OTA in the current conveyor.

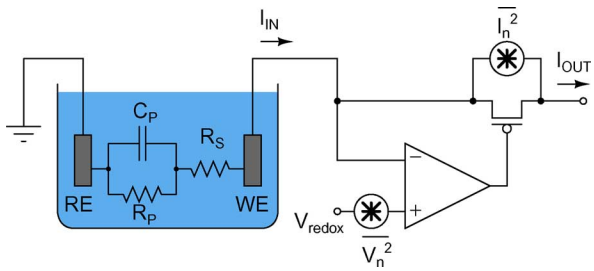


Fig. 5. Simplified noise model of the potentiostat front-end.

and a dual-mode ADC. Next, each of these circuits is described in detail.

A. Current Conveyor

The current conveyor is comprised of a PMOS transistor connected in the feedback of an OTA, as shown in Fig. 4(a). The negative feedback ensures a known potential at the working electrode as set by the voltage at the non-inverting input of the OTA. The cascode transistor M_2 boosts the output impedance.

The current conveyor OTA shown in Fig. 4(b) employs a folded-cascode topology for a wide-swing output. The main consideration in the design of the current conveyor is its noise. This noise limits the sensitivity of the potentiostat. It originates from the OTA and the PMOS transistor in the current conveyor as shown in Fig. 5.

The input-referred noise of the OTA is due to the thermal and flicker noise. The impedance between the reference and the working electrodes is modeled as a leakage resistance, R_P, in parallel with the double layer capacitor, C_P, both in series with the electrode resistance, R_S [22]. According to the simplified model given in Fig. 5, the output noise power of the first stage is

$$\overline{I_{n,OUT}^2} = \left|\frac{g_m A}{1+g_m AZ}\right|^2 \overline{V_n^2} + \left|\frac{1}{1+g_m AZ}\right|^2 \overline{I_n^2} \qquad (8)$$

where $\overline{V_n^2}$ is the OTA input-referred noise, $\overline{I_n^2}$ is the noise due to the feedback transistor, g_m is the transconductance of the PMOS feedback transistor, A is the open-loop gain of the OTA, and Z is the equivalent impedance of the electrode. For practical values of g_m, A and Z, the contribution of I_n^2 in (8) is negligible, resulting in the total output current noise

$$\overline{I_{n,OUT}^2} = \frac{V_n^2}{|Z|^2}. \qquad (9)$$

Since the leakage resistance, R_P, is typically very large, and the electrode resistance, R_S, is small, the electrode equivalent impedance is approximately capacitive

$$Z \approx \frac{1}{j\omega C_P}. \qquad (10)$$

Substituting (10) into (9) results in

$$\overline{I_{n,OUT}^2} = (2\pi f C_P)^2 V_n^2. \qquad (11)$$

According to (11), the output noise root mean square (RMS) value is directly proportional to the input-referred noise of the OTA and the electrode capacitance. The effective area of the electrode determines its capacitance. On the other hand a larger area of the electrode causes more biomolecules to undergo a redox reaction and accordingly results in a larger input signal. As a result, the electrode capacitance does not affect the signal-to-noise ratio (SNR).

The input-referred noise of the OTA consists of two components, the thermal noise and the $1/f$ noise. The thermal noise component can be expressed [23] as

$$\frac{\overline{V_{n,thermal}^2}}{\Delta f} = \frac{4kT}{g_{m1}}\left(\frac{4}{3}\right)\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m9}}{g_{m1}}\right). \qquad (12)$$

By biasing $M_{1,2,3,4,9,10}$ such that $g_{m3,4,9,10} \ll g_{m1,2}$, the noise contribution of $M_{3,4,9,10}$ is minimized. The key to minimize the g_m ratios is to bias the input differential pair transistors in the weak inversion region, where the transconductance efficiency, g_m/I_D, is maximized, and to bias $M_{3,4,9,10}$ in the strong inversion region to minimize their g_m.

The input-referred $1/f$ noise power can be expressed [23] as

$$\frac{\overline{V_{n,1/f}^2}}{\Delta f} = \frac{2K_P}{C_{ox}W_1L_1 f} + \frac{2K_N}{C_{ox}W_3L_3 f}\left(\frac{g_{m3}}{g_{m1}}\right)^2 + \frac{2K_P}{C_{ox}W_9L_9 f}\left(\frac{g_{m9}}{g_{m1}}\right)^2. \qquad (13)$$

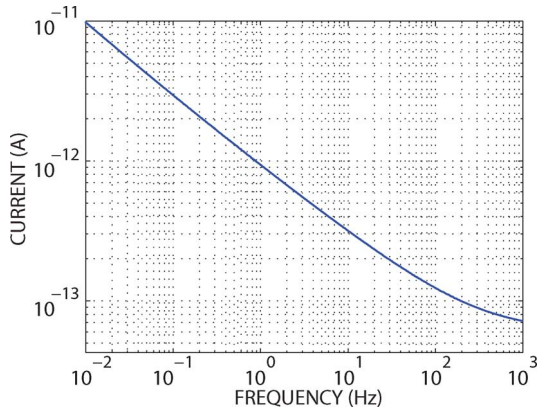


Fig. 6. Simulated input-referred current noise of the current conveyor.

TABLE I
CURRENT CONVEYOR NOISE SUMMARY

OTA Transistor	Noise Type	Noise Contribution, %
$M_{1,2}$	Flicker	25.26
$M_{3,4}$	Flicker	23.4
$M_{1,2}$	Thermal	21
$M_{3,4}$	Thermal	18.5
$M_{10,9}$	Flicker	6.25
$M_{10,9}$	Thermal	3.22

Given the minimized transconductance ratios, the $1/f$ noise contribution of $M_{3,4,9,10}$ is negligible compared to that of $M_{1,2}$. In order to minimize the $1/f$ noise, large PMOS transistors are employed for the input differential pair of the OTA.

The simulated input-referred noise of the current conveyor plotted in Fig. 6 is consistent with the theoretical analysis. The integrated input-referred noise over 1 kHz bandwidth is 3.1 pA. The main contributors to the input-referred noise are the flicker noise of the OTA input pair $M_{1,2}$ and of the tail current transistors $M_{3,4}$. The contribution of each transistor to the total input-referred noise is shown Table I. The cascode transistors in the OTA and the feedback transistors M_1 and M_2 in Fig. 4(a) contribute less than one percent to the total input-referred noise.

Other sources of error in low-level current recording systems are the junction and subthreshold leakage currents. The junction leakage current is proportional to the source/drain junction area. Minimum-area diffusion regions in the layout of all transistors in the signal path are utilized, such as a non-contacted diffusion between transistors M_1 and M_2 in Fig. 4(a). The subthreshold leakage current increases with the device width. Minimum-size transistors are employed in the current path in Fig. 4(a). The subthreshold leakage current also increases with the drain-to-source voltage for V_{ds} values below 100 mV. For transistors M_1, M_2 and S_2 this current gets added to the signal. In some cases, the values of voltages V_{WE} and V_{COMP} can be chosen such that the drain-to-source voltage on these transistors is significantly higher than the thermal voltage (e.g., 100 mV or higher). In these cases the leakage current contributes only a DC offset (time and signal independent) to the signal and can be subtracted out by offset calibration. Tables II and III summarize the OTA electrical characteristics and its transistor sizing respectively.

TABLE II
OTA SIMULATED ELECTRICAL CHARACTERISTICS

DC gain	84dB
Unity Gain Frequency (0.5pF load)	16MHz
Slew Rate	13V/μs
Output Voltage Swing	$2V_{pp}$
Total Bias Current	$16\mu A$
Supply Voltage	3.3V

TABLE III
OTA AND COMPARATOR TRANSISTOR SIZING

OTA		Comparator	
Transistor	W/L (μm)	Transistor	W/L (μm)
$M_{1,2}$	$8 \times 3/1$	$M_{1,2}$	$8 \times 1/1$
$M_{3,4}$	$2 \times 1/4$	$M_{3,4}$	$2 \times 1/0.5$
$M_{5,6}$	$4 \times 1/1$	$M_{5,6}$	$1 \times 0.8/0.35$
$M_{7,8}$	$8 \times 1/1$	$M_{7,8}$	$2 \times 1/0.35$
$M_{9,10}$	$4 \times 1/4$	$M_{9,10}$	$1 \times 1/0.35$
M_{11}	$8 \times 1/2$	M_{11}	$8 \times 1/2$
—	—	M_{12}	$2 \times 1/2$
—	—	M_{13}	$1 \times 1/2$
—	—	$M_{14,15}$	$1 \times 1/0.35$
—	—	M_{16}	$4 \times 1/0.35$

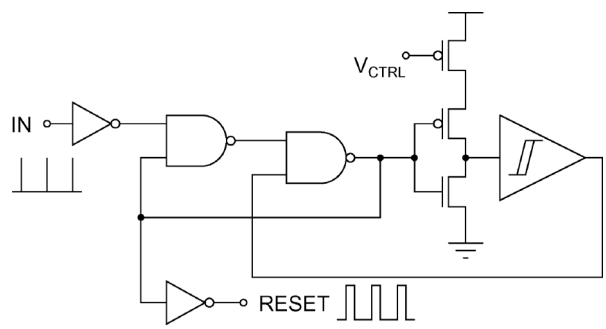


Fig. 7. A simple logic circuit, known as pulse-shaping block, for widening the $RESET$ signal.

B. Dual-Mode ADC

As described in Section II, the proposed ADC operates in two phases. In the first, coarse conversion phase, the current-to-frequency ADC generates the MSBs. In the second, fine conversion phase, the LSBs are extracted by the single-slope ADC. Both ADCs reuse most of the same circuit components.

The current steering switches $S_{1,2}$ in Fig. 4(a) select the path through which the redox current flows. During the coarse conversion phase the current continuously charges the integrating capacitor. The comparator generates a reset pulse when the voltage across the capacitor reaches V_{REF} as needed to discharge the integrating capacitor. The comparator output pulse is not wide enough to fully discharge the capacitor. Fig. 7 shows the circuit that widens the $RESET$ pulse [24]. The duration of the $RESET$ pulse is controlled by the gate voltage of the current-starved inverter current source. The number of the ADC output pulses is directly proportional to the input current. A counter counts the number of pulses generated during this phase and produces the MSBs. Upon completion of the first phase, the voltage across the integrating capacitor is held and the single-slope ADC extracts the LSBs. The voltage across the capacitor remains between ground and V_{REF}. The reference voltage applied to the comparator starts ramping down and the

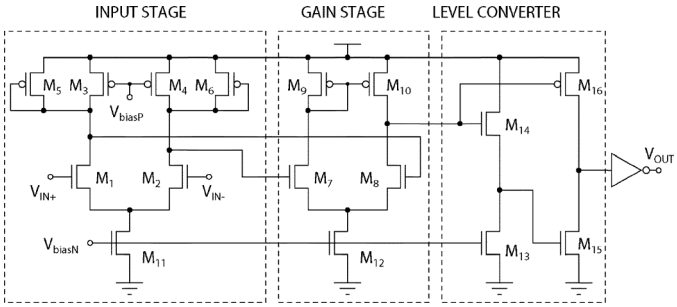


Fig. 8. The multi-stage comparator circuit diagram.

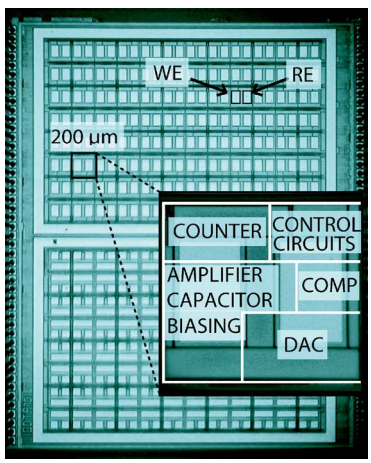


Fig. 9. Die micrograph of the 96-channel integrated potentiostat fabricated in a 0.35 μm CMOS technology. The die size is 3.8×3.1 mm^2.

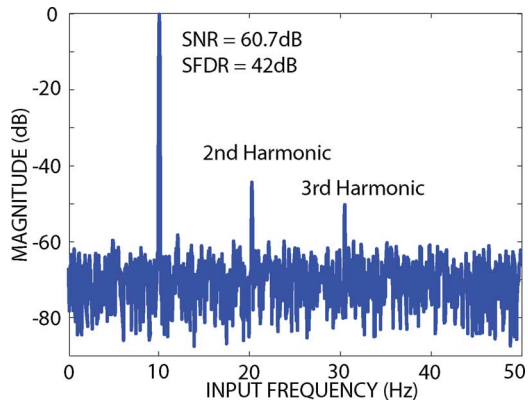


Fig. 10. Experimentally measured output spectrum of the ADC for a 20 nA peak-to-peak 10 Hz sinusoidal input for 0.1 kHz sampling rate.

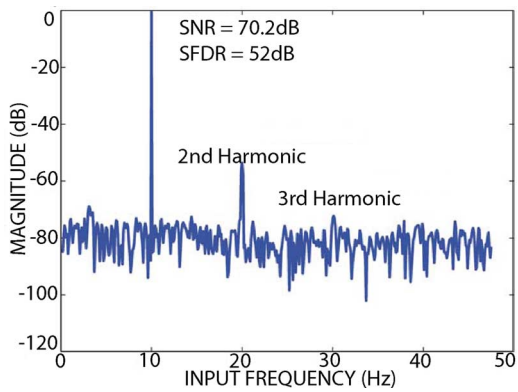


Fig. 11. Experimentally measured output spectrum of the full channel for a 350 nA peak-to-peak 10 Hz sinusoidal input for 1 kHz sampling rate.

input of the counter is switched to a clock signal. The counter counts the number of clock cycles that the ramp reference voltage requires to reach the capacitor voltage.

The input-dependent charge injection due to the switches may limit the accuracy of the ADC. To minimize this effect, switch S_3 turns off slightly before S_2 turns off, leaving no path through C_{INT} for the channel charge of S_2 to flow and introduce an error. The input-dependent charge injection is not fully removed because of the parasitic capacitors, but becomes negligibly small. A multi-stage comparator shown in Fig. 8 is employed in the ADC. The first stage is a high-speed amplifier with diode-connected load transistors. The second stage has a high gain in order to increase the overall gain of the comparator. Level converters are employed to make the output signal compatible to CMOS logic levels. Transistor sizes are given in Table II.

To save silicon area, both the counter and the shift register are implemented as a 15-bit linear feedback shift register (LFSR). The same circuit is reused as a counter and shift register. During the analog-to-digital conversion period it operates as a counter. During the readout it shifts out one-bit digital outputs [18].

IV. Experimental Results

An array of integrated potentiostats was fabricated in a 0.35 μm double-poly four-metal standard CMOS process. The die micrograph is shown in Fig. 9. The microchip consists of two 8×12 sub-arrays, one for single-ended (upper) and one for differential amperometry (lower)[25]. The two sub-arrays have been fully experimentally characterized and can run simultaneously within a single 192-channel system. The focus of this paper is on the 96-channel single-ended implementation only. Each channel of the potentiostat records a redox current generated at an on-chip working electrode and converts it into the digital domain. Four different external voltages drive the four adjacent on-chip reference electrodes in every 2×2 adjacent channels in a mosaicing fashion. This allows for simultaneous detection of four different biochemical groups each reduced/oxidized at a different voltage, as the voltage difference between the working and reference electrodes can be set independently for each of the four sets of 24 channels.

Dynamic performance of an entire channel was characterized by applying 20 nA and 350 nA peak-to-peak sinusoidal input currents generated with a Stanford Research System (DS360) function generator connected to the potentiostat input through a 2 MΩ and 20 MΩ resistor, respectively. Fig. 10 (20 nA) and Fig. 11 (350 nA) show the power spectral density of the quantized output. The minimum dynamic current level (LSB) of the potentiostat for sampling frequencies of 0.1 ksps and 1 ksps are 24 pA and 135 pA respectively. The LSBs are calculated based on the SNR for a given sampling frequency. The corresponding linear input dynamic range is 95 dB cumulatively for the two sampling frequency settings (24 pA to 350 nA).

The output SFDR is limited by the non-linearity of the current conveyor, not the ADC. Fig. 12 depicts the linearity of the

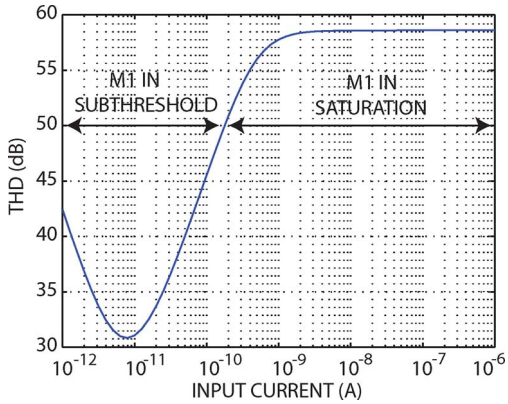


Fig. 12. Total harmonic distortion of the current conveyor versus input current.

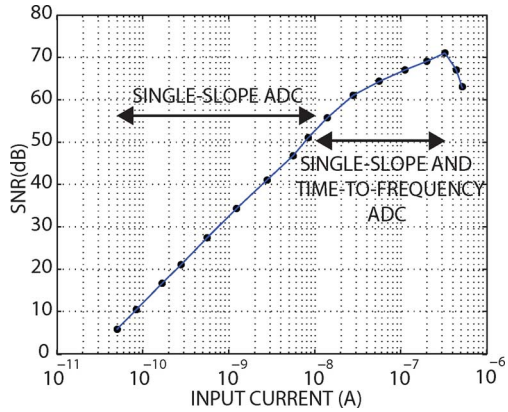


Fig. 14. Experimentally measured channel SNR versus input current at 0.1 and 1 ksps sampling frequency.

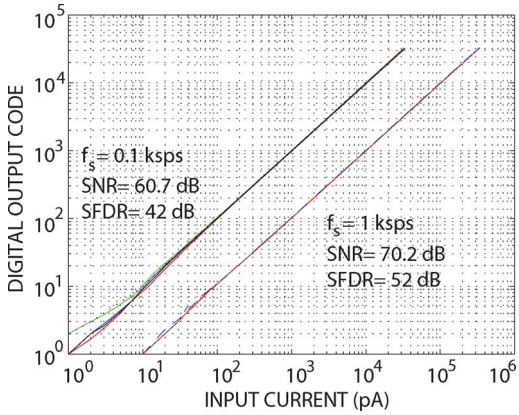


Fig. 13. Experimentally measured transfer characteristics of four adjacent channels in one column of the potentiostat array for two sampling frequencies.

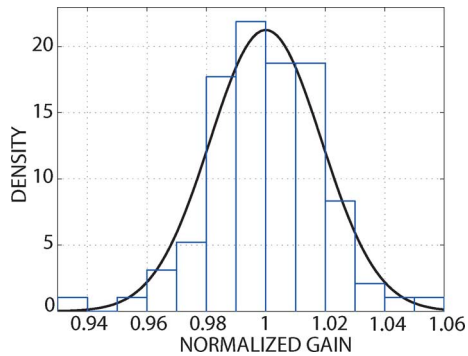


Fig. 15. Gain mismatch distribution of 96 single-ended potentiostat channels and its Gaussian best fit.

current conveyor versus the input current. Due to the finite gain of the transconductance amplifier and the non-linearity of the feedback transistor (subthreshold biasing) the overall linearity of the current conveyor is limited to a maximum of 58 dB as shown in Fig. 12. At low current levels the feedback transistor M_1 is operating in the subthreshold region resulting in a sub-optimal linearity of the current conveyor limiting the effective number of bits (ENOB) of the whole channel to 8.3. The static performance of the channel is characterized by sweeping the input current between 1 pA and 350 nA as shown in Fig. 13.

The peak channel SNR versus the input current for the sampling frequency of 1 ksps is shown in Fig. 14. At low currents, only the single-slope ADC is operating, achieving a maximum SNR of 56 dB at 10 nA. At higher currents, both modes of the ADC are engaged thus improving the channel peak SNR by 14 dB to 70.2 dB at 300 nA.

Fig. 15 shows the normalized gain distribution of all channels in the array where a 1 nA current is applied to each channel. Due to the mismatch between the integrating capacitors and other active components it follows a gaussian distribution with a 3-sigma standard deviation of 1.9 percent. At very low currents the leakage current affects recording channels by introducing an offset but has a negligible effect on the channel gain. Table IV summarizes the experimentally measured characteristics of the integrated potentiostat.

TABLE IV
EXPERIMENTALLY MEASURED CHARACTERISTICS

Technology	0.35μm CMOS
Supply Voltage	3.3V
Die Area	3.8mm×3.1mm
Array Dimensions	16×12 channels
Channel Size	200μm×200μm
Maximum Sampling Rate	1ksps
Sensitivity	24pA
Channel SNR (fs=1ksps)	11.32 bits
Channel SFDR (fs=1ksps)	8.3 bits
Channel Power Consumption	
Current Conveyor	80μW
Comparator	63μW
Biasing	23μW
Digital	22μW
Total	188μW

V. VALIDATION IN APPLICATION

The integrated prototype has been experimentally validated in chemical sensing of neurotransmitters for neurophysiological applications.

Neurotransmitters are a class of biomolecules that carry signals across the synaptic gap between neurons in the nervous systems. One of these biomolecules which has been extensively studied is dopamine. Dopamine is a neurotransmitter in the human brain that plays a key role in diseases such as Alzheimer's and Parkinson's. In this section the utility of the integrated potentiostat was validated by measuring dopamine

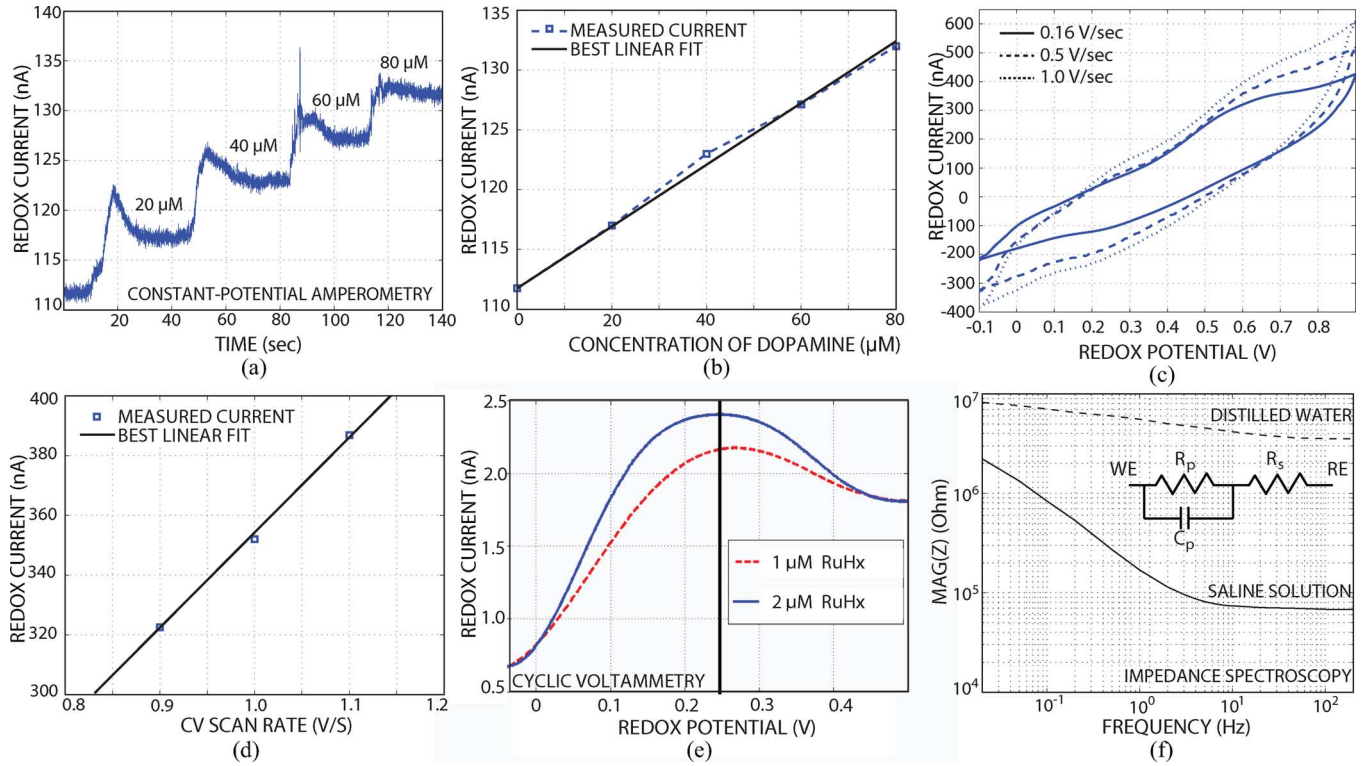


Fig. 16. Experimentally measured results of: (a) dopamine constant-potential amperometry with (b) the corresponding potentiostat calibration plot, (c) 0.01 M phosphate buffered saline solution cyclic voltammetry at three different scan rates with (d) the corresponding calibration plot, (e) RuHx cyclic voltammetry, and (f) impedance spectroscopy.

concentration. Dopamine constant-potential amperometric detection was first performed on a single channel with an off-chip working electrode and a gold quasi/pseudo reference electrode. The working electrode potential was held at 1.8 V, 300 mV above that of the reference electrode to induce a dopamine redox reaction. Controlled amounts of dopamine (2 mM dopamine solution in perchloric acid, $HClO_4$) were added to the 0.1 mM phosphate buffered saline solution. This resulted in steps in the current measured by the potentiostat, as shown in Fig. 16(a). Clinically relevant chemical concentrations are used in this experiment. Phosphate buffered saline is employed as the bulk solution for dopamine concentration measurements. As seen, there is a large, 112 nA, offset current due to the redox potential applied between the working and reference electrodes. The transient part of the response is mainly due to the manual stirring of the solution. The calibration curve for the sensor-potentiostat system is shown in Fig. 16(b). This curve demonstrates the linear relationship between the concentration of dopamine and the output redox current.

A cyclic voltammetry experiment was also performed to demonstrate recording of redox currents at high sampling rates. Fig. 16(c) shows the cyclic voltammograms recorded by one channel on a 0.01 M phosphate buffered saline solution at three different scan rates. As expected, the current generated by the buffer (the background current) increases as the scan rate increases. The corresponding calibration curve for the potentiostat is shown in Fig. 16(d). This curve demonstrates the linear relationship between the scan rate and the background current.

A 100 mV/s cyclic voltammetry with a 30 second resting period between each cycle was performed on RuHx solution, a standard solution used to calibrate microelectrodes utilized in redox electrochemical sensing. The resulting background-subtracted cyclic voltammetry curve (forward scan) for two concentrations of RuHx solution is shown in Fig. 16(e). There is a distinguishable peak at 250 mV, the oxidization voltage of RuHx. In order to avoid a large background current, low sweep rates were utilized.

An impedance spectroscopy experiment was also performed by applying a small-amplitude sinusoidal potential to an off-chip reference electrode placed first in distilled water and then phosphate buffered saline solution. The correct frequency-domain representation of the impedance between electrodes was generated by sweeping the frequency of the sinusoidal potential as shown in Fig. 16(f).

The top metal in the integrated CMOS potentiostat, when coated with a noble metal such as gold, can serve directly as the on-die electrode. The integration of the electrodes with the potentiostat minimizes the interference noise, eliminates the excessive wiring and yields a compact low-cost sensory microsystem. Aluminum, a standard CMOS interconnect metal, has poor bio-compatibility. Also, because of the native oxide layer, it is not directly suitable for the amperometric sensing. A post-fabrication process is required to coat the electrode surface with an inert biocompatible metal such as gold.

Both 2D and 3D biocompatible microelectrodes have been fabricated on the surface of the potentiostat die for on-chip spatial biochemical sensing. An array of 192 2D gold microelec-

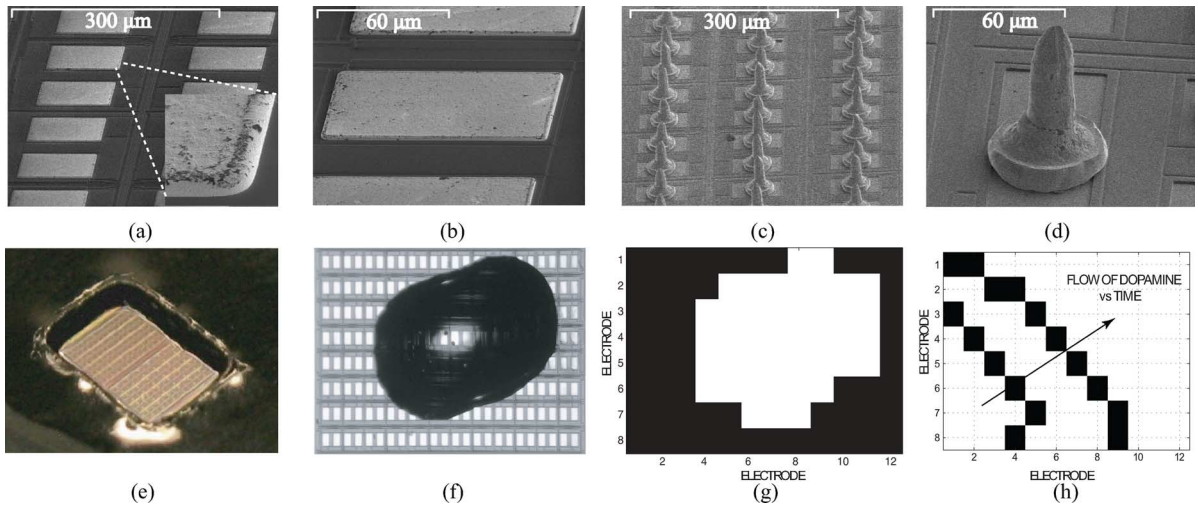


Fig. 17. SEM images of (a, b) on-die 2D gold electrodes and (c, d) on-die 3D gold electrodes. (e) Encapsulated die photograph. (f) Micrograph of the phosphate buffered saline solution drop placed on the single-ended sub-array on the die and (g) the corresponding experimentally recorded impedance spectroscopy results (thresholded at 2 nA). (h) Experimental impedance spectroscopy results of on-die imaging of dopamine solution flow front.

trodes (on both single-ended and differential arrays) were electrolessly plated with a 2 μm-thick Ni base and 0.75 μm-thick gold as shown in Fig. 17(a) and (b). The 3D microelectrodes are 100 μm-long gold bumps [26] bonded to the die as depicted in Fig. 17(c) and (d). They can also be used for neurochemical activity monitoring in acute brain slices in in-vitro animal studies, as the pointed shape allows for penetrating a thin ($\sim$ 50 μm) layer of dead tissue caused by tissue slicing. After the electrode fabrication, the die is wire-bonded and the bonding wires are insulated with a biocompatible epoxy as depicted in Fig. 17(e).

In order to demonstrate the on-chip spatial recording functionality of the potentiostat, a drop of the 0.01 M phosphate buffered saline solution was placed on the electrode array while the reference electrode was driven by a sinusoidal (low-pass filtered saw-tooth) waveform. Fig. 17(f) depicts a micrograph of the drop. The result of the on-chip spatial impedance specroscopy recording at a single frequency (thresholded) is shown in Fig. 17(g).

Dopamine constant-potential amperometry was performed on the array of on-chip 3D gold electrodes. A drop of dopamine in the phosphate buffered saline solution was placed in the corner of electrode array. Fig. 17(h) depicts two images recorded by impedance spectroscopy (thresholded at 2 nA) capturing the front of the flow of dopamine on the surface of the die.

For rapid nerouchemical sensing on a low-cost miniature platform, the potentiostat die was integrated with a simple two-layer PDMS microfluidic chamber as depicted in Fig. 18(a). An example of the bottom layer fluidic chamber is shown in Fig. 18(b). Fig. 18(c) depicts a micrograph of the fluidic chamber in Fig. 18(b) compression-sealed against the surface of the potentiostat die. Fig. 18(d) shows the impedance spectroscopy results (thresholded) measured by the potentiostat when dopamine was flowing through the chamber over one sub-array on the die. In future we envision culturing dissociated cells and brain slices within a microfluidic chamber.

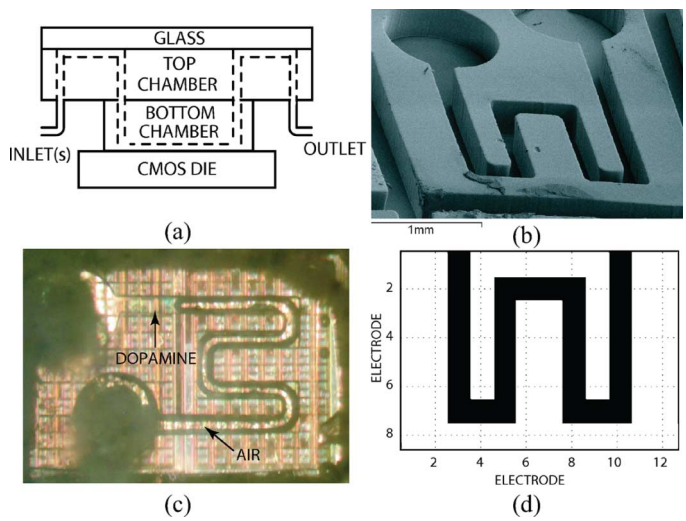


Fig. 18. (a) Cross-sectional view of the on-chip two-layer PDMS microfluidic chamber. (b) Bottom chamber microfluidic network example. (c) Fluidic chamber compression-sealed against the surface of the potentiostat die. (d) Experimentally measured results of on-chip impedance spectroscopy of dopamine.

Table V provides a comparative analysis of the presented design and existing amperometric biochemical sensory microsystems. The presented design offers an unmatched combination of conversion rate, channel power and integration area. The compactness of the design yields a high channel count of 192 on a small 3.15×1.9 mm^2 area in a 0.35 μm CMOS technology. The prototype has been demonstrated in all three biochemical sensory methods: constant-potential amperometry, cyclic voltammetry and impedance spectroscopy.

VI. Conclusions

A 96-channel integrated potentiostat microarray with on-die microelectrodes for neurochemical imaging has been presented. A 95 dB linear dynamic range and 1 ksps maximum sampling

TABLE V
COMPARATIVE ANALYSIS OF AMPEROMETRIC SENSORY MICROSYSTEMS

	Tech (μm)	Channel Count	Max Conversion Rate (Hz)	Channel Power (μW)	Channel Area (mm^2)	Min Current (1LSB from SNR, pA)	Max Current	On-chip Electrodes 2D/3D	On-chip Microfluidics	Sensory Methods CA/CV/IS
ISSCC 94 [10]	2	1	2500	5000	4.84	–	40mA	-/-	-	-/Yes/-
JSSC 04 [18]	0.5	128	10	N/A	0.1	–	100nA	Yes/-	-	Yes/-/-
TCAS-I 06 [4]	1.2	42	3	11.5	0.086	–	100nA	-/-	-	Yes/-/-
TCAS-I 06 [13]	0.5	1	3	5500	0.7	–	10uA	-/-	-	-/Yes/-
ISSCC 08 [7]	0.6	24	10	N/A	N/A	97	100nA	Yes/-	-	-/Yes/-
JSSC 08 [1]	0.25	16	2500	N/A	0.12	240	250nA	Yes/-	-	-/Yes/-
JSSC 09 [5]	0.5	4	5000	76	N/A	98	750nA	-/-	-	-/Yes/-
This Work	**0.35**	**192**	**1000**	**188**	**0.04**	**24 (at 100Hz)**	**350nA**	**Yes/Yes**	**Yes**	**Yes/Yes/Yes**

rate are achieved by combining the current-to-frequency and the single-slope ADC architectures with a low circuit overhead. Electrical experimental measurements verify the specifications of the potentiostat. Neurochemical detection experiments validate the utility of the potentiostat in neurophysiological sensory applications. On-chip 3D gold electrodes are a promising sensor modality for future tissue-penetrating and implantable brain neurochemistry analysis applications.

ACKNOWLEDGMENT

The authors would like to thank Canadian Microelectronics Corporation (CMC) for providing the fabrication services and microsystem integration services.

REFERENCES

[1] M. Roham, M. P. Garris, and P. Mohseni, "A wireless IC for time-share chemical and electrical neural recording," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3645–3658, 2009.

[2] P. M. Levine, P. Gong, R. Levicky, and K. L. Shepard, "Active CMOS sensor array for electrochemical biomolecular detection," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1859–1871, 2008.

[3] M. Ahmadi and G. Jullien, "Current-mirror-based potentiostats for three-electrode amperometric electrochemical sensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, pp. 1339–1348, 2009.

[4] C. Yang, Y. Huang, B. L. Hassler, R. M. Worden, and A. J. Mason, "Amperometric electrochemical microsystem for a miniaturized protein biosensor array," *IEEE Trans. Biomed. Circuits Syst*, vol. 3, no. 3, pp. 160–168, 2009.

[5] R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, and N. Thakor, "16-channel integrated potentiostat for distributed neurochemical sensing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 11, pp. 2371–2376, Nov. 2006.

[6] A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, and A. Hassibi, "A CMOS electrochemical impedance spectroscopy (EIS) biosensor array," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 379–390, 2010.

[7] F. Heer, M. Keller, G. Yu, J. Janata, M. Josowicz, and A. Hierlemann, "CMOS electro-chemical DNA-detection array with on-chip ADC," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2008, pp. 168–169.

[8] T. M. Seese, H. Harasaki, G. M. Saidel, and C. R. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating," *Lab. Invest.*, vol. 78, no. 12, pp. 1553–1562, Dec. 1998.

[9] R. F. B. Turner, D. J. Harrison, and H. P. Baltes, "A CMOS potentiostat for amperometric chemical sensors," *IEEE J. Solid-State Circuits*, vol. 22, pp. 473–478, 1987.

[10] R. J. Reay, S. P. Kounaves, and G. T. A. Kovacs, "An integrated CMOS potentiostat for miniaturized electroanalytical instrumentation," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1994, pp. 162–163.

[11] R. G. Kakerow, H. Kappert, E. Spiegel, and Y. Manoli, "Low-power single-chip CMOS potentiostat," in *Proc. IEEE Int. Conf. Solid-State Sensors and Actuators*, 1995, vol. 1, pp. 142–145.

[12] M. Roham and P. Mohseni, "A wireless IC for wide-range neurochemical monitoring using amperometry and fast-scan cyclic voltammetry," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 27–30, 2007, pp. 3131–3134.

[13] F. Laiwalla, K. G. Klemic, F. J. Sigworth, and E. Culurciello, "An integrated patch-clamp amplifier in silicon-on-saphire CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 11, pp. 2364–2370, Nov. 2006.

[14] J. Zhang, Y. Huang, N. Trombly, C. Yang, and A. Mason, "Electrochemical array microsystem with integrated potentiostat," *IEEE Sensors*, pp. 385–388, 2005.

[15] M. Stanacevic, K. Murari, G. Cauwenberghs, and N. Thakor, "16-channel wide-range VLSI potentiostat array," in *Proc. IEEE Int. Workshop Biomedical Circuits and Systems*, 2004, pp. 17–21.

[16] A. Bandyopadhyay, G. Mulliken, G. Cauwenberghs, and N. Thakor, "VLSI potentiostat array for distributed electrochemical neural recording," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 26–29, 2002, vol. 2, pp. 740–743.

[17] A. Gore, S. Chakrabartty, S. Pal, and E. C. Alocilja, "A multichannel femtoampere-sensitivity potentiostat array for biosensing applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 11, pp. 2357–2363, 2006.

[18] M. Schienle, C. Paulus, A. Frey, F. Hofmann, B. Holzapfl, P. Schindler-Bauer, and R. Thewes, "A fully electronic DNA sensor with 128 positions and in-pixel A/D conversion," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2438–2445, 2004.

[19] M. Nazari, H. M. Jafari, and R. Genov, "192-Channel CMOS neurochemical microarray," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2010, pp. 121–125.

[20] J. Rhee and Y. Joo, "Wide dynamic range CMOS image sensor with pixel level ADC," *IEEE Electron. Lett.*, vol. 39, pp. 360–361, 2003.

[21] D. Park, J. Rhee, and Y. Joo, "A wide dynamic-range CMOS image sensor using self-reset technique," *IEEE Electron Device Lett.*, vol. 28, no. 10, pp. 890–892, 2007.

[22] D. Burns, "Detection of transmitter release with carbon fiber electrodes," *J. Neurosci. Methods*, vol. 33, pp. 312–321, 2004.

[23] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[24] S. K. Islam, R. Vijayaraghavan, M. Zhang, S. Ripp, S. D. Caylor, B. Weathers, S. Moser, S. Terry, B. J. Blalock, and G. S. Sayler, "Integrated circuit biosensor using living whole-cell bioreporters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 89–98, Jan. 2007.

[25] M. Nazari and R. Genov, "A Fully differential CMOS potentiostat," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2009, vol. 2, pp. 2177–2180.

[26] J. Aziz, R. Genov, M. Derchansky, B. Bardakjian, and P. Carlen, "256-channel neural recording microsystem with on-chip 3D electrodes," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2007, pp. 160–161.

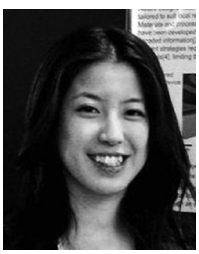
Meisam Honarvar Nazari (S'09) received the B.Sc. degree from the University of Tehran, Tehran, Iran, in 2005, the M.A.Sc. degree from the University of Toronto, Toronto, ON, Canada, in 2008, and the M.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2009.

He is currently working toward the Ph.D. degree at the California Institute of Technology. The focus of his current research is high-performance mixed-signal integrated circuits, with the focus on high-speed and low-power optical and electrical interconnects. He spent the summer of 2011 at Rambus Inc. working on new equalization techniques for high data rate communication links.

Mr. Nazari received the University of Toronto Fellowship for Fall 2006 and an Atwood Fellowship for Fall 2008. He is the corecipient of 2008 Brian L. Barge Award for excellence in microsystems integration, 2010 AMD/CICC Student Scholarship Award, and the 2012 Solid-State Circuits Society Award. He is also an NVIDIA 2012 Graduate Fellowship finalist.

Hamed Mazhab-Jafari (S'11) received the B.Eng. and M.A.Sc. degrees in electrical engineering from McMaster University, Hamilton, ON, Canada, in 2004 and 2006, respectively.

He is currently working toward the Ph.D. degree in electrical and computer engineering at the University of Toronto, Toronto, ON, Canada. His M.A.Sc. thesis focused on low-power ultra-wideband CMOS front end and ultra-widebands antennas. His Ph.D dissertation focus is on CMOS DNA analysis SoC. He has held internship positions at Kapik Integration, where he worked on low-power mixed signal circuits. Since 2011, he has been with Snowbush IP, Toronto, ON, Canada, where he focuses on research and development of next-generation high-speed wireline communication systems.



Lian Leng received the B.A.Sc. degree in mechanical engineering from McGill University, Montreal, QC, Canada, in 2007 and the M.A.Sc. degree from the University of Toronto, Toronto, ON, Canada, in 2010.

She is currently working toward the Ph.D. degree at the Guenther Laboratory, University of Toronto. Her research interests are in the development of microfluidic systems for the high throughput generation of organized multidimensional materials for regenerative medicine.

Axel Guenther received the Ph.D. degree from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, and conducted postdoctoral research at the Massachusetts Institute of Technology, Cambridge.

He is an Assistant Professor in the Department of Mechanical and Industrial Engineering with cross-appointment to the Institute of Biomaterials and Biomedical Engineering, University of Toronto, Toronto, ON, Canada. He has authored more than 30 scientific papers and invented three licensed technologies.

Dr. Guenther was the recipient of the ETH silver medal (2002), the Ontario Early Researcher Award (2009), the I.W. Smith Award of the Canadian Society of Mechanical Engineers (2010) and currently holds the Wallace G. Chalmers Chair of Engineering Design. He co-organizes "Ontario-on-a-Chip", the annual event on microfluidics, microreactors and labs-on-a-chip, which facilitates contact between university researchers and chemical, pharma, biotech, advanced materials and analytical device companies and is the Scientific Director of a new Centre for Microfluidic Systems in Chemistry and Biology in Toronto.

Roman Genov (S'96–M'02–SM'11) received the B.S. degree (first rank) in electrical engineering from the Rochester Institute of Technology, Rochester, NY, in 1996, and the M.S. and Ph.D. degrees in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, in 1998 and 2002, respectively.

He held engineering positions at Atmel Corporation, Columbia, MD, in 1995 and Xerox Corporation, Rochester, NY, in 1996. He was a Visiting Researcher in the Laboratory of Intelligent Systems at the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1998 and in the Center for Biological and Computational Learning at the Massachusetts Institute of Technology, Cambridge, in 1999. He is currently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Toronto, Toronto, ON, Canada. His research interests include analog and digital VLSI circuits, systems and algorithms for energy-efficient signal processing with applications to electrical, chemical and photonic sensory information acquisition, biosensor arrays, brain-silicon interfaces, parallel signal processing, adaptive computing for pattern recognition, and implantable and wearable biomedical electronics.

Dr. Genov received the Canadian Institutes of Health Research (CIHR) Next Generation Award in 2005, the Brian L. Barge Award for excellence in microsystems integration in 2008, the DALSA Corporation Award for excellence in microsystems innovation in 2006 and 2009, and the Best Paper Award on sensors and the Best Student Paper Award, both at the IEEE International Symposium on Circuits and Systems in 2009. He is an Associate Editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, and IEEE SIGNAL PROCESSING LETTERS.