Feature

Power-Aware Multimedia:
Concepts and Design Perspectives

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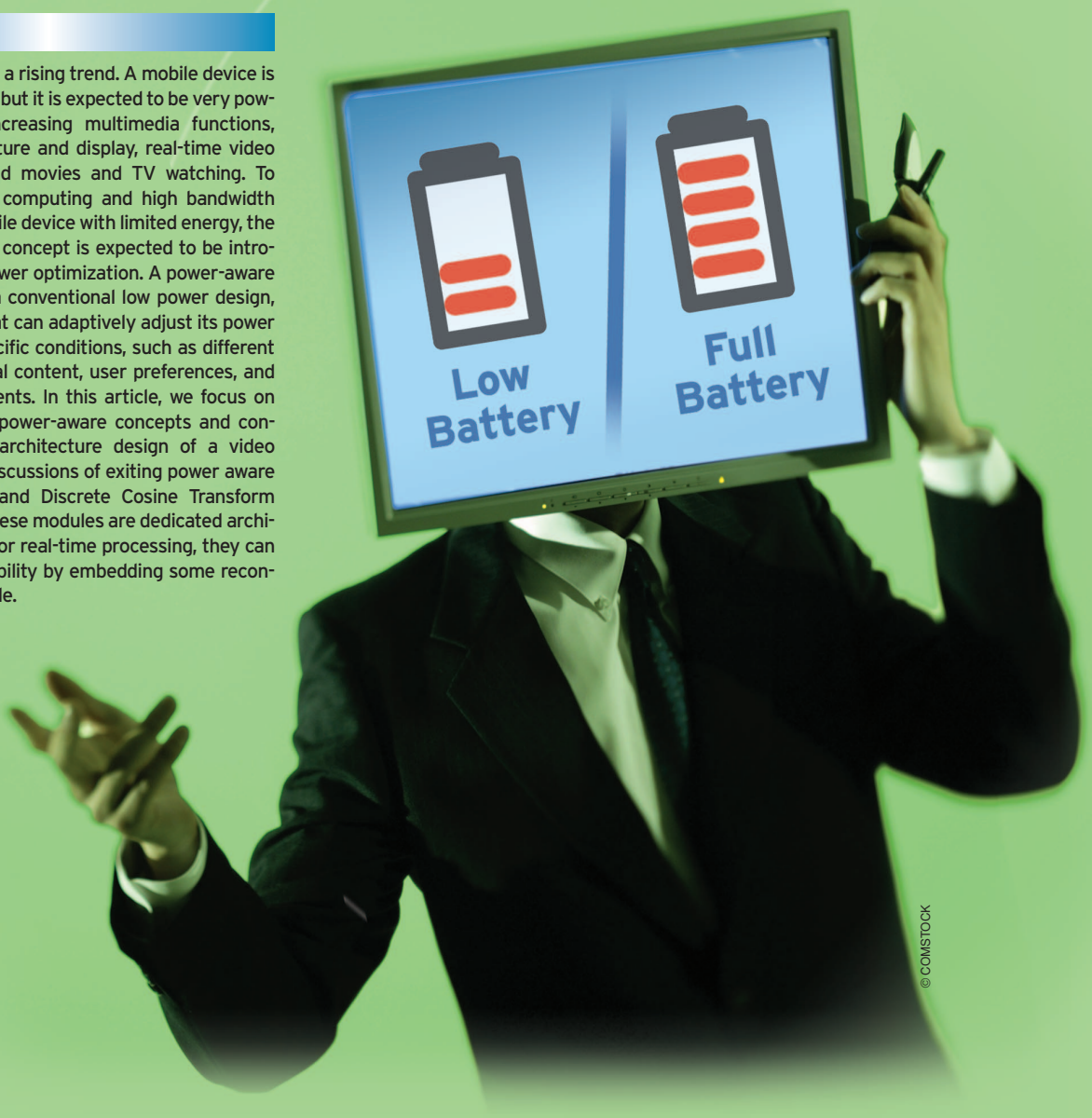
Abstract

Mobile multimedia is a rising trend. A mobile device is light, thin, and small, but it is expected to be very powerful to support increasing multimedia functions, such as photos capture and display, real-time video communications, and movies and TV watching. To support these high computing and high bandwidth operations on a mobile device with limited energy, the power-aware design concept is expected to be introduced for further power optimization. A power-aware system is not only a conventional low power design, but also a design that can adaptively adjust its power consumption to specific conditions, such as different battery status, signal content, user preferences, and operating environments. In this article, we focus on the introduction of power-aware concepts and considerations to the architecture design of a video coder, followed by discussions of exiting power aware Motion Estimation and Discrete Cosine Transform designs. Although these modules are dedicated architectures optimized for real-time processing, they can provide power scalability by embedding some reconfigurable points inside.



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1. Introduction

Mobile multimedia becomes feasible with the rapid advances of semiconductor and communication technologies. Mobile multimedia is so popular since people wish to enjoy joyful music, beautiful images, and wonderful videos anywhere and anytime. From voice and text only service to music, image and video applications, a mobile device now integrates more multimedia functions, and, therefore, requires more and more computing power. With the rapid advances of semiconductor technology, putting billions or even trillions of transistors on a chip is possible. While the computing power of IC chips keeps increasing, it is not a big problem to have a high performance multimedia processor, and there have been chips that can handle real-time encoding of HDTV or even higher resolution videos. It will be a big problem, however, if we do not offer enough energy for a power-hungry battery-operated multimedia processor.

A powerful processor does not work without power. Different from a non-mobile device with a power line, a mobile appliance relies on batteries with limited energy. While more and more multimedia functions are integrated into a portable device, the growth of power capacity still falls behind the hungry requirements. Besides the continuing explorations of higher capacity or brand new battery technologies, what we designers can do is to keep lowering the power consumption. Designers have tried to lower the power consumption by carefully examining factors contributing to power reduction at each abstraction level, such as system, algorithm, architecture, and circuit levels, and proposing many low power design techniques. The combinations of these techniques help extend the battery lifetime significantly. That is why we can actually enjoy more of our music or movies with even less power. However, these improvements are never satisfactory since people always ask for more.

Beyond the conventional low power thinking, the power-aware design concept [1]–[3] is introduced to mobile multimedia. Here in this paper, a power-aware design means that it has multiple power modes of operation, and can adapt its operating configurations based on the awareness of environmental conditions, such as energy constraint (battery status) or user preferences. The power control process is like a marathon athlete who adjusts his running speed to complete the race. The introduction of power awareness opens another dimension for further power optimization. This article provides an overview of power aware video codec design concepts and approaches. The focus will be more, from an ASIC design's perspective, on how a dedicated architecture can provide the functionality of power awareness. A function-dedicated but parameter-reconfigurable architecture is a promising approach as it can meet the hard real-time processing requirement and also enable the power awareness. Design perspectives and examples on power aware Motion Estimation (ME) and Discrete Cosine Transform (DCT) will be discussed in this paper followed by discussions and conclusions.

2. Beyond Low Power: Power Aware Concepts

No power means not every function is available, let alone multimedia. As the power problems become the obstacle to the feasibility and popularity of mobile multimedia, how to economize the use of energy is a critical design issue of portable devices. A portable device, of course, should be a low power design. However, beyond that, it should also be a power-aware design. Simply speaking, a power-aware device is a smart design that is aware of the limiting power, and it can utilize the available energy in a smart and efficient way by dynamically adjusting the power consumption. The idea behind the power-aware concept is analogous to our daily life behaviors. With limited time and energy, we have to prioritize the jobs at hand, and give more efforts to important things, while skipping less important ones or just finishing these things "roughly".

Consider a scenario that a portable device estimates by itself that the battery can only afford 30 more minutes while operating at current configurations, but the user cannot charge the device until one hour later when he arrives home. In this case, a smart device should accept the request to sustain the operations for at least one hour, and try to adapt the system to a configuration that consumes less power to last longer.

A power aware device, therefore, should have multiple power modes, and it could choose a suitable mode by accepting a user's direct command, predicting a user's preferences from history, or sensing current operating environment automatically, such as network conditions, data characteristics and battery status, etc. The design idea is to provide more operating points between the binary on and off states. When battery power is almost exhausted or under certain level, the computing engine can switch to a lower power mode at the cost of certain quality loss or functions not being supported. In this case, the service, although not as perfect as it is in a power-rich state, can sustain for a longer time instead of completely off.

Even when the battery power is still enough, a power aware design should be able to execute the computations

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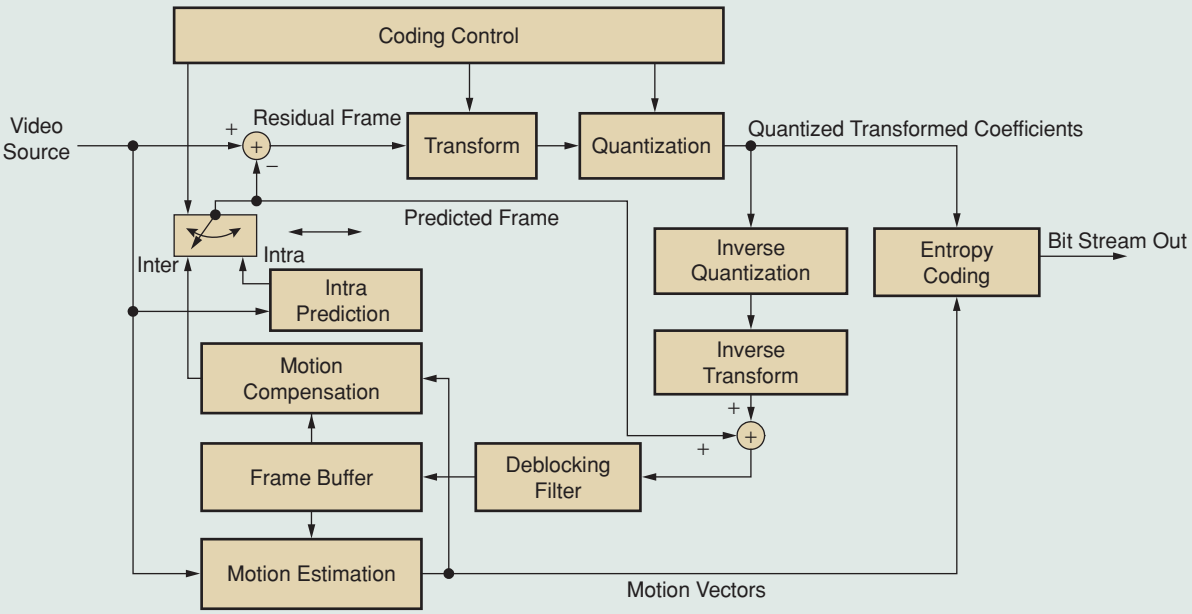


Figure 1. General functional block diagram of a video coder.

with just-enough energy. Conventional content-blind processing is designed for worst case, and therefore always uses full energy no matter whether the job is easy or difficult. A power aware design is, on the contrary, aware of the content variations. The goal is to have a design that can scale down its power consumption as the job complexity is decreasing. That is, the design should be content aware and adaptive, and waste no energy on easy jobs.

3. Power-Aware Video Codec Design

Video coding (compression) is a core technology that enables the storage and transmission of a large amount of digital video data. Figure 1 shows a typical video coding framework. It is a hybrid coding architecture based on Discrete Cosine Transform (DCT) and Motion Estimation/Motion Compensation (ME/MC). The technique of ME/MC is to remove the temporal redundancy between frames, while DCT followed by entropy coding is to remove the spatial and statistical redundancy of video data. Many widely used video coding standards, such as MPEG-1/-2/-4, H.26x, and H.264/AVC, are mainly based on this framework.

The design of a power-aware video codec extends the original rate-distortion (R-D) optimization problem to a three-dimensional power-rate-distortion or complexity-rate- distortion optimization problem [4], [5] (Figure 2). In a situation where power is very critical, video quality can be sacrificed to some extent to lower the power consumption and to sustain longer the encoding or decoding of a video. In a video codec, there are various parameters that can be adjusted to lower the power consumption. The goal is to find a good configuration that has optimal visual quality under the rate and power constraints. Figure 3 shows a conceptual example that illustrates the power-aware video coding.

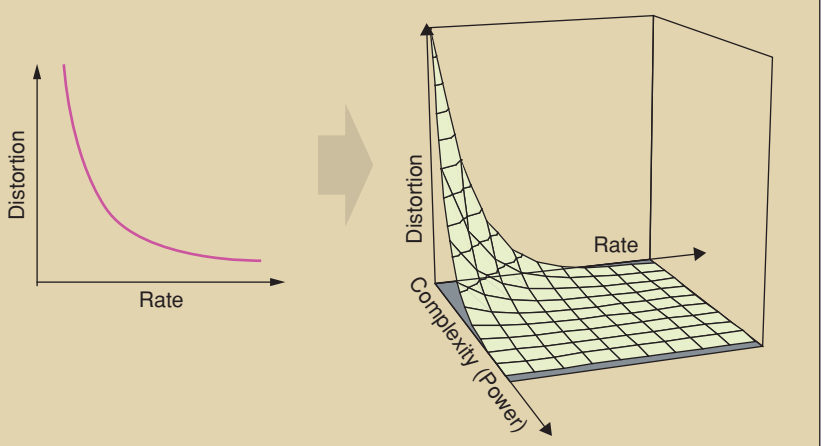


Figure 2. From a two-dimensional Rate-Distortion to a three-dimensional Complexity/Power-Rate-Distortion optimization.

To master the domain knowledge of video coding is the key to the design of a power-aware video codec. We need insightful analysis and understanding of the characteristics of video data and compression algorithms. There are various types of video content and their characteristics can be very diverse sequence-by-sequence, and even frame-by-frame. The sources of videos can be home videos, or professional videos, such as movies, advertisements, and news. The video content may be a slow motion one, such as head-and-shoulder view, a fast motion one, such as sports video, or a view with global motion. Furthermore, a frame can be composed of complex or simple scene, and with few or many object motions. A video sequence with simple content and slow motion is easier to be compressed. In this case, a video coding processor should theoretically be able to finish this simpler work with less power.

As for the video compression algorithm side, there are good characteristics that can be utilized. Figure 4 shows a performance (Video Quality) versus power consumption diagram. First, lossless fast algorithms can be developed to reduce the power consumption. By these fast algorithms, the computational process is different, but the results are the same. The optimization in this stage is a general consideration for a low power design. One step further, the characteristics of video data and the intermediate data during compression can be carefully exploited to reduce the power. That is, the design is now content-aware so that it can adjust the computing power according to the data complexity. For example, the design can detect zero coefficients or all-zero-coefficient blocks in advance, and ignore executions such as multiplying by zero to save energy. So far, the video quality is the same as the situation without applying these techniques. From this point on, the power is reduced at the cost of quality degradation. A direct thinking consists in trading some losses of computation precision for the power reduction in order to have other lower power modes.

Researches and applications of the power-aware design attract a lot of attention today. In the field of modern microprocessor designs, dynamically adjusting the operating frequency and supplying voltage to deliver the performance on demand have realized the power-aware concept. In [5], the rate-distortion behavior of the

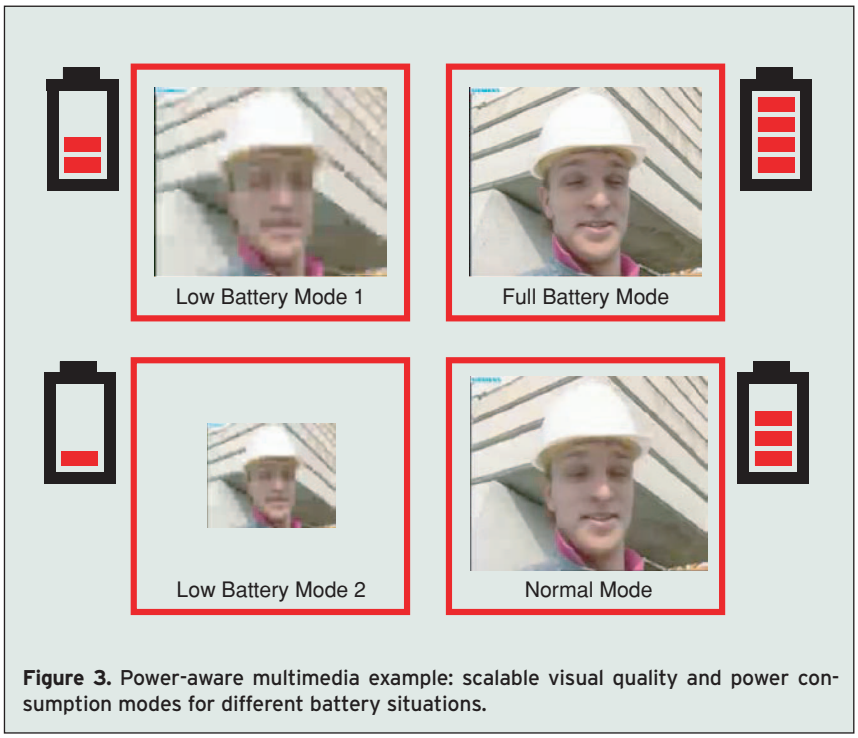


Figure 3. Power-aware multimedia example: scalable visual quality and power consumption modes for different battery situations.

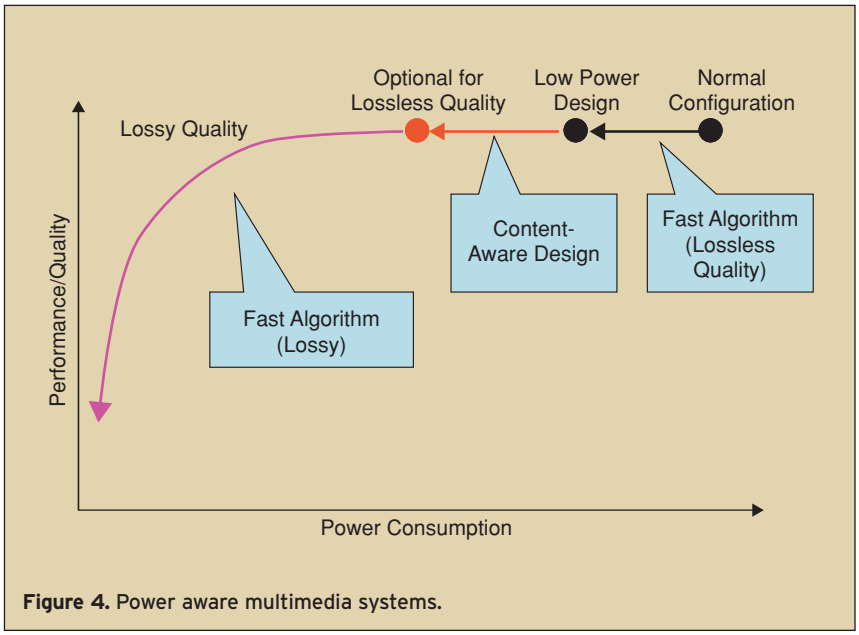
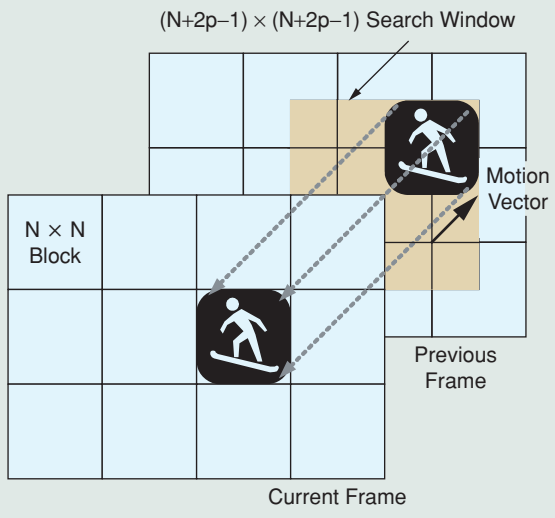


Figure 4. Power aware multimedia systems.

complexity control parameters is investigated, and an analytic power-rate-distortion model is built. In [6], a configurable video coding system is proposed. An exhaustive search and the Lagrangian multiplier method are used to optimize the performance and computational complexity of this coder. In [7], dynamically parameterized algorithms and architectures for the ME, DCT, Lempel-Ziv coding, 3D graphics, and Viterbi decoding are discussed. In the following subsections, we will look into the design considerations of power-aware ME and DCT. These two modules are the key to a power-aware video codec.

3.1 Power-Aware ME

Motion estimation is an effective but high-complexity technique to remove the temporal redundancy for video compression. For inter-frame prediction, a current frame is first partitioned into Macro Blocks (MBs), where each MB is a 16 × 16 block. To code an MB, the process is to search for the most similar MB (best matched MB) in previously coded frames, code the motion vector, which points to the previous coded MB, and then code the difference (residue) of the two MBs. Figure 5 illustrates the block matching ME.



$$SAD(m, n) = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} |c(i, j) - s(i + m, j + n)|$$

Figure 5. Block Matching Motion Estimation. An image is partitioned into 16 × 16 Macro Blocks (MBs). For each MB, the best-matched MB is searched in a [−p, (p − 1)] search range. Sum of Absolute Difference (SAD) is adopted as the criterion for the matching.

The computational complexity of ME [8] is very high. It is seen from the run time profiling of a processor-based implementation of a video codec that ME always occupies over half of the computing time. As for ASIC implementations of a video codec, the ME module always needs most of the gate count, memory and bandwidth. The ME is, therefore, the most critical module in a video codec not only because of the real-time performance requirements but also because of the power issue considerations.

Block based ME technique is adopted in video coding standard, but how to search for a motion vector is beyond the scope of the standardization. Therefore, there are great possibilities for research and design trade-offs on the ME algorithm. The impact of the ME performance is that when a more similar MB is found, the residue (difference between the two MBs) is smaller, and then the compression performance can be better. If we ask for better ME search quality, we need to spend more power. To search for the best matched MB, Full Search (FS) ME, which search for all possible candidates in a search range, can guarantee the smallest SAD value, but the complexity of exhausted search is the highest.

Full Search ME is not always necessary. There is a saturation point of quality improvement. After that point, you pay significant effort, but get little performance improvement. It is similar to the experience of exam preparation in our daily life. The effort spent to get more scores from 80 to 100 (full marks) is greater than from, say, 40 to 60. When the time and energy are limited, a smart strategy is not to pursue the full marks so that you can do more things.

Various searching tricks are, therefore, proposed to reduce the complexity of ME. These tricks form large sets of fast algorithms, such as three-step search (3SS), four-step search (4SS), hierarchical search, and diamond search, etc. Basically, the idea is to skip some candidates skillfully so that the computational complexity is lower but the search result is still close to the best-matched one. Another well-known skill is pixel truncation scheme, which truncates some lower bits of a coefficient during ME search, and sub-sampling scheme, which sub-sample the image to a smaller one for ME search. These methods can be combined with those fast ME algorithms to further reduce the computing precision and the number of data to be processed.

A power-aware ME can, therefore, be achieved by implementing different searching algorithms with variable search range, and pre-constrained searching candidate numbers, etc. Figure 6 shows a reconfigurable ME design proposed in [9]. Three ME algorithms, Full Search (FS), Three-Step Search (3SS), and Enhanced Four-Step Search (E4SS), can

be executed on this reconfigurable hardware. Different algorithms have different search patterns and flows, but they can share the same processing unit of parallel tree to accumulate the Sum of Absolute Differences (SADs). Four quality modes, the ultrahigh quality, high quality, normal, and low battery modes, are selectable by adaptively adopting different combinations of ME algorithms.

The proposed content-aware ME algorithm is based on two criteria, the variance of neighboring blocks' motion vectors and the accuracy of predictive motion vectors [9], to adaptively select the searching algorithm in a quality mode. In ultrahigh quality mode, Full Search ME provides the highest quality but consumes most power. In high quality mode, the Full Search ME is still adopted but the search range is adaptively changed from [-16, 15] to [-8, 7]. When the variance of neighboring blocks' motion vectors is small and the accuracy of predictive motion vectors is high, a smaller search range is selected. To further lower the power consumption, fast searching algorithms are adopted. The Full Search and Enhanced 4SS (E4SS) [9] are adaptively adopted in the normal mode. When the variance of neighboring blocks' motion vectors is small and the accuracy of predictive motion vectors is smaller than a predefined SAD threshold, the E4SS ME is performed; otherwise, Full Search ME is performed. For the low battery mode, two fast ME algorithms, E4SS and 3SS are the choices. Similar to the selection criterion in previous mode, the 3SS is selected when the variance of neighboring blocks is large or the accuracy of predictive MV is not good enough. The adaptive E4SS/3SS mode is suitable for strict power constraint.

Figure 7 shows the result of the power awareness. From the simulation results, the cost of adaptive search range scheme is about 40% of the complete Full Search mode, and the PSNR drop is only 0.036dB in average. As for lower complexity modes of normal and low-battery modes, the cost is about 21% and 3.73%, respectively, and the average quality drop is about 0.01dB and 0.16dB, respectively. The idea behind this architecture is simple, and it demonstrated the feasibility and effectiveness of power-aware consideration.

3.2 Power-Aware DCT

DCT and inverse DCT (IDCT) are also computationally intensive modules in a video codec. For an MPEG-4 Simple Profile encoder with full search ME, the DCT, Quantization (Q), Inverse Quantization (IQ), and IDCT occupies about 16% of overall complexity. As for an encoder with

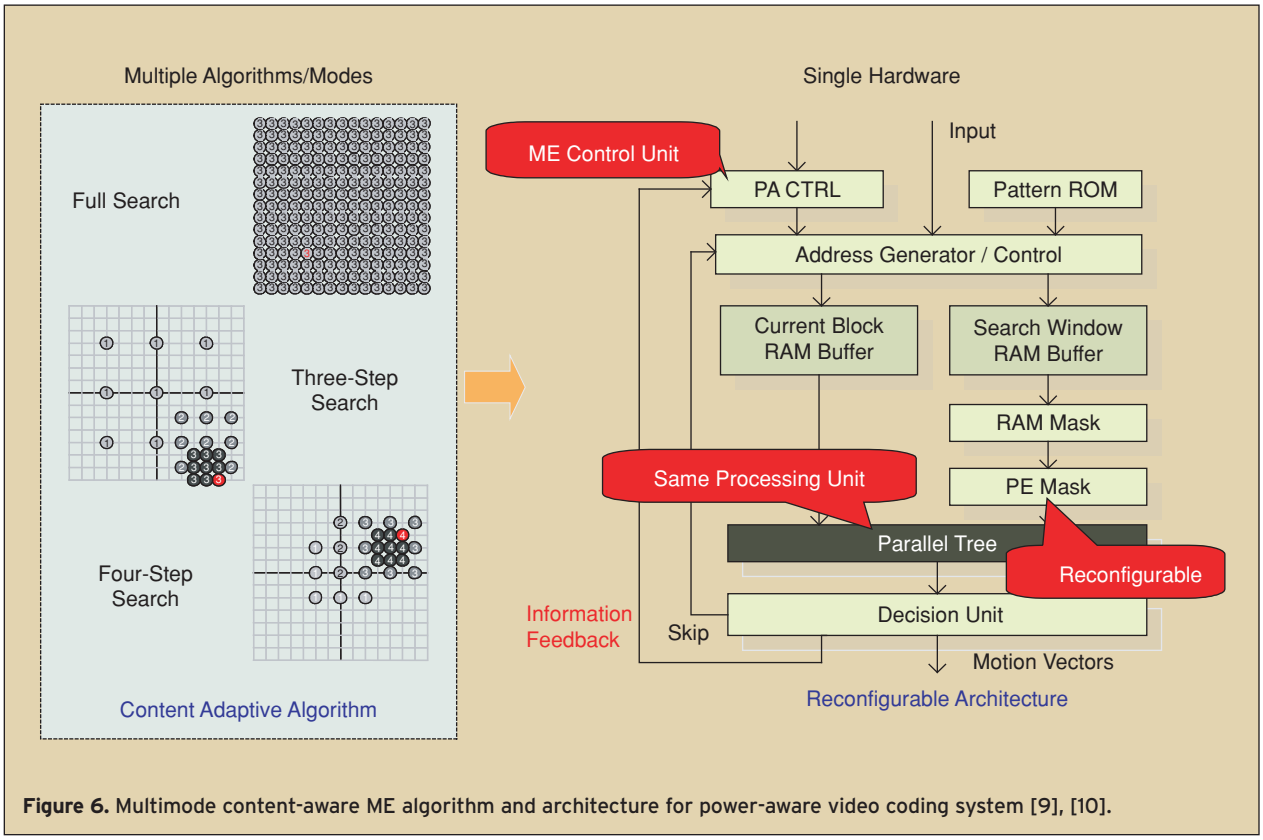


Figure 6. Multimode content-aware ME algorithm and architecture for power-aware video coding system [9], [10].

fast ME algorithm, DCT/Q/IQ/IDCT can occupy up to 29% of overall complexity.

For a module that is mainly composed of arithmetic computations, such as additions, subtractions and multiplications, there are basically two ways for the considerations of power-awareness. One is to reduce the number of data that has to be processed, and the other is to reduce the bit-width (precision) of the data path. The idea is to approximate the original computing results by sacrificing some precision at the less significant or less visible part.

When the data signals have large content variations, these data are potential to be utilized for low power and power aware design. The data signals in the DCT, Q, IQ, and IDCT modules in a video codec are one of the good examples to show the power awareness through content-aware detection. For the coding of natural images, after the 8×8 2D DCT, the magnitudes of lower-frequency DCT coefficients in a block are usually larger than those of higher-frequency ones. Since the human visual system is less sensitive to higher frequency signals, high frequency components are usually quantized more. As we increase the compression ratio by raising the quantization steps, more and more high frequency coefficients are quantized to zero. Besides a single 8×8 block, the percentage of non-zero occurrence of quantized DCT coefficients between frames and sequences also has large variations, depending on the complexity of the scene.

For the IDCT, the computational precision has to meet the IEEE Standard 1180–1990 so that the drift error in the video coding loop can be controlled to some extent. As for the DCT, there are no constraints on it, since it is an encoder issue and the scope of a video standard is only the decoding part. Therefore, the precision of DCT implementation is a better candidate for power-aware design. Feasible methods are to jointly consider the quantization effect and the DCT, to design a content-aware DCT module by exploiting the video data characteristics, or to directly reduce the precision or operations at some cost of quality.

In the literature, there have been a number of researches devoted to the algorithms for content-dependent DCT [11]–[15] and IDCT [16], [17]. By the exploitation of the signal variations, these algorithms apply content-dependent variable workload processing for the reduction of computational complexity.

There have also been several dedicated architectures proposed for content-dependent DCT and IDCT. The Distributed Arithmetic (DA) [18] based architecture proposed by [19] can deal with the approximation of zero or low-precision output data as well as the

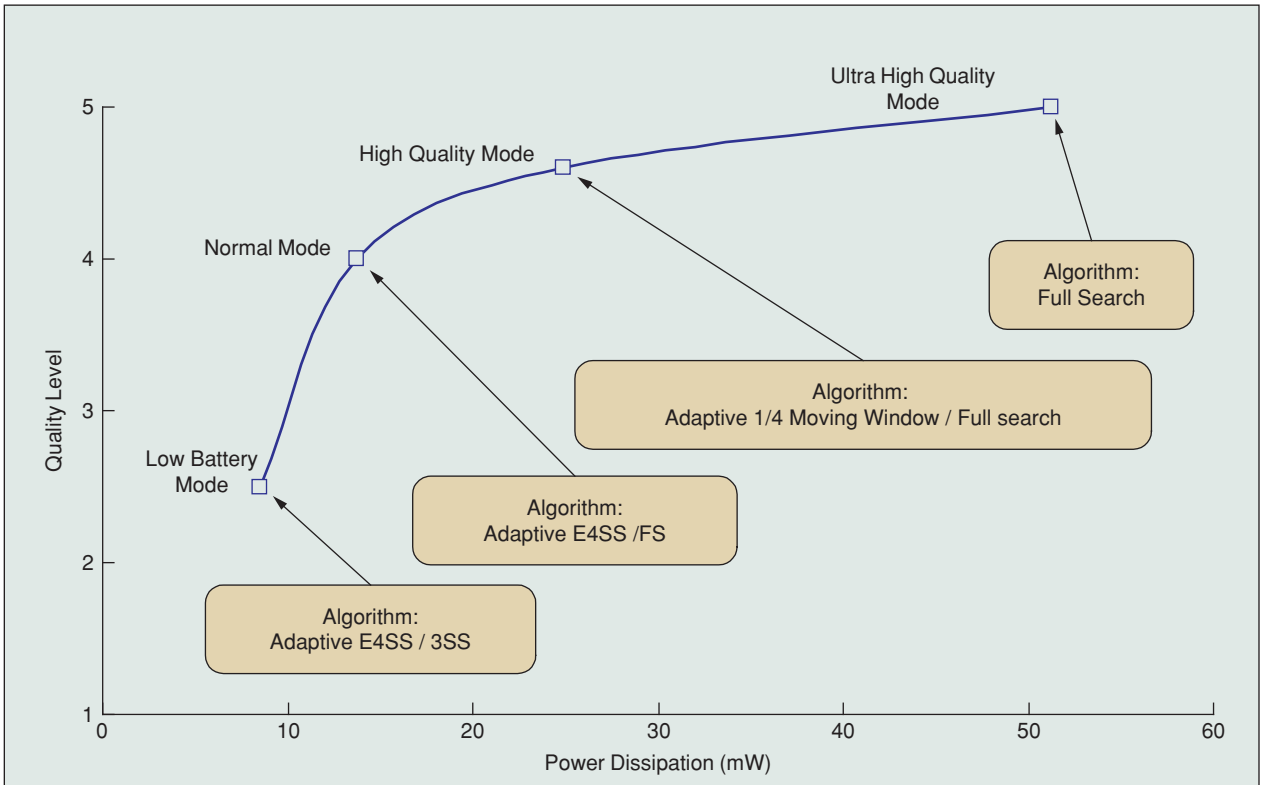


Figure 7. Power-aware reconfigurable ME experimental results.

estimation of low-precision input data. Another DA-based architecture in [21] can handle the estimation of zero or low-precision input data, and it extends the support of DCT and IDCT in a single architecture. DA-based realization of the processing elements is intuitive since DA does the calculation bit by bit so that the precision can be easily controlled at bit-level. As for Flow-Graph-based architectures, the one proposed in [21] is a content-dependent IDCT, which processes the estimation of zero input data. The later FG-based architecture proposed in [22] extends the support of DCT and IDCT in a single architecture that can cope with the approximation of zero output data as well as the estimation of zero input data.

4. Discussions

A power-aware system is composed of the low-level reconfigurable modules for power scalability and the system-level power-aware control and optimization. Not only processor based designs but also ASIC style codecs can provide the power awareness through power-scalability oriented reconfigurable architecture. Modules such as the above-mentioned dedicated ME and DCT architectures provide various configuration modes, and each consumes different power levels. The system then controls the configuration to adjust the power consumption efficiently.

In addition to power aware module design of conventional non-scalable video coding standard, the emerging scalable video coding provides more features for power awareness. The emerging MPEG Scalable Video Coding (SVC) supports spatial, temporal, and PSNR scalabilities by inter-layer prediction, Motion Compensation Temporal Filtering, and Fine Granularity Scalability based techniques. The SVC algorithm is inherently complexity scalable. An SVC decoder can therefore decode the bitstream considering its computing capability and energy status. For example, spatial resolution, frame rate, or SNR/fidelity can be reduced to save more power when applicable and necessary.

5. Conclusions

It has been a dream that a machine can think itself as human beings. Though it seems still a long way to go, electronic devices are more and more intelligent through various awareness schemes, such as content-aware, computing resource-aware, and temperature-aware designs, etc. For mobile multimedia, power awareness is the most important technique. A power-aware design goes one step further for intelligent mobile multimedia beyond the original low power design concept. For real time video coding, dedicated architectures with power-aware reconfigurability are a promising solution. Existing power-aware architecture designs show the feasibility and capability of power scalability. The design of reconfigurable architecture for power awareness and the power-rate-distortion optimized system control will be the key to power-aware multimedia.

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References

[1] T. Sakurai, "Perspectives on power-aware electronics," *Digest of Technical Papers, IEEE Int. Solid-State Circuits Conf. 2003 (ISSCC 2003)*, vol. 1, pp. 26–29.

[2] L.-G. Chen, "Power-aware multimedia," *SE2 Power-Aware Signal Processing, Evening Session, Digest of Technical Papers, IEEE International Solid-State Circuits Conference 2006 (ISSCC 2006)*, p. 17.

[3] M. Bhardwaj, R. Min, and A.P. Chandrakasan, "Quantifying and enhancing power awareness of VLSI systems," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 9, no. 6, pp. 757–772, Dec. 2001.

[4] Z. He, S.K. Mitra, "From rate-distortion analysis to resource-distortion analysis," *IEEE Circuits and Systems Magazine*, vol. 5, no. 3, pp. 6–18, 2005.

[5] Z. He, Y. Liang, L. Chen, I. Ahmad, and D. Wu, "Power-rate-distortion analysis for wireless video communication under energy constraints," *IEEE Trans. on Circuits and Systems for Video Technology*, vol. 15, no. 5, pp. 645–658, May 2005.

[6] D.N. Kwon, P.F. Driessen, A. Basso, and P. Agathoklis, "Performance and computational complexity optimization in configurable hybrid video coding system," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 16, no. 1, pp. 31–42, Jan. 2006.

[7] P. Jain, A. Laffely, W. Burleson, R. Tessier, and D. Goeckel, "Dynamically parameterized algorithms and architectures to exploit signal variations," *Journal of VLSI Signal Processing Systems*, vol. 36, no. 1, pp. 27–40, Jan. 2004.

[8] Y.-W. Huang, C.-Y. Chen, C.-H. Tsai, C.-F. Shen, and L.-G. Chen, "Survey on block matching motion estimation algorithms and architectures with new results," to appear, *Journal of VLSI Signal Processing Systems*.

[9] P.-C. Tseng, "Design and Implementation of Power-Aware Video Codec Systems," Ph.D. Dissertation, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan. Jan. 2005.

[10] S.-S. Lin, P.-C. Tseng, C.-P. Lin, and L.-G. Chen, "Multi-mode content-aware motion estimation algorithm for power-aware video coding systems," in *Proc. IEEE Workshop on Signal Processing Systems (SIPS 2004)*, pp. 239–244, 2004.

[11] B. Girod and K.W. Stuhlmuller, "A content-dependent fast DCT for low bit-rate video coding," in *Proc. of IEEE Int. Conf. on Image Processing*, pp. 80–84, 1998.

[12] I.M. Pao and M.T. Sun, "Modeling DCT coefficients for fast video encoding," *IEEE Trans. on Circuits and Systems for Video Technology*, vol. 9, no. 4, pp. 608–616, Jun. 1999.

[13] K. Lengwehasatit and A. Ortega, "DCT computation based on variable complexity fast approximations," in *Proc. of IEEE Int. Conf. on Image Processing*, pp. 95–99, 1998.

[14] A. Docef, F. Kossentini, K. Nguuyen-Phi, and I.R. Ismaeil, "The quantized DCT and its application to DCT-based video coding," *IEEE Trans. on Image Processing*, vol. 11, no. 3, pp. 177–187, Mar. 2002.

[15] K. Lengwehasatit and A. Ortega, "Scalable variable complexity approximate forward DCT," *IEEE Trans. on Circuits and Systems for Video Technology*, vol. 14, no. 11, pp. 1236–1248, Nov. 2004.

[16] L. McMillan and L. Westover, "A forward-mapping realization for the inverse discrete cosine transform," in *Proc. IEEE Data Compression Conf.*, pp. 219–228, 1992.

[17] J.F. Yang, S.C. Shaih, and B.L. Bai, "An efficient two-dimensional inverse discrete cosine transform algorithm for HDTV receivers," *IEEE*

Trans. on Circuits and Systems for Video Technology, vol. 5, no. 1, pp. 25–30, Feb. 1995.
[18] S.A. White, "Applications of distributed arithmetic to digital signal processing: a tutorial review," *IEEE ASSP Magazine*, vol. 6, no. 3, pp. 4–19, Jul. 1989.
[19] T. Xanthopoulos, A.P. Chandrakasan, "A low-power DCT core using adaptive bitwidth and arithmetic activity exploiting signal correlations and quantization," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 740–750, May 2000.
[20] L. Fanucci and S. Saponara, "Data driven VLSI computation for low-power DCT-based video coding," in *Proc. Int. Conf. on Electronics, Circuits, and Systems*, pp. 541–544, 2002.
[21] T. Xanthopoulos, A.P. Chandrakasan, "A Low-Power IDCT macrocell for MPEG-2 MP@ML exploiting data distribution properties for minimal activity," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 693–703, May 1999.
[22] N.J. August and D.S. Ha, "Low power design of DCT and IDCT for low bit rate video codecs," *IEEE Trans. on Multimedia*, vol. 6, no. 3, pp. 414–422, June 2004.

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