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Fundamental Circuit Topology of Duo-Active-Neutral-Point-Clamped, Duo-Neutral-Point-Clamped, and Duo-Neutral-Point-Piloted Multilevel Converters

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Abstract

Multilevel voltage-source converters are well-suited for power conversion applications demanding higher power density, reliability, efficiency, and power quality. An unremitting and persistent research for developing advanced multilevel converter topologies with improved characteristics, performance, modulation techniques, and control methods continues. This paper proposes duo-neutral-point-clamped (D-NPC), duo-active-neutral-point-clamped (D-ANPC), and duo-neutral-point-piloted (D-NPP) multilevel voltage-sourced converter topologies. The D-NPC, D-ANPC, and D-NPP converters phase-leg is realized by adding low-frequency semiconductor power switches to their structures. This results in a substantial reduction in the number of the high-frequency pulse-width-modulation (PWM) insulated-gate bipolar transistors (IGBTs) and clamping passive devices including diodes as well as flying-capacitors (FCs). Moreover, a drastic abatement in the total voltage rating and total stored energy of the FCs within the D-ANPC topology is achieved compared to the classic ANPC configuration. The experimental results are provided for D-NPC, D-ANPC, and D-NPP converters to validate the feasibility of their topology and modulation method for control of the multilevel converters.

tilevel converters.

Index Terms- D-ANPC converter, D-NPC converter, D-NPP converter, Diode abatement, FC energy reduction, FC voltage decrease, IGBT abatement.

1 Introduction

Multilevel converters have been the focus of an intense attention from academia and industry since their emergence in 1980s, and have made their way into medium-voltage (MV) energy management and power conversion market [1]. Researchers across the globe are making great efforts to improve the topology and enhance the performance of these configurations [2]. Multilevel voltage-source topologies comprising of low-voltage (LV)/MV semiconductor power switches such as the LV/MV-insulated-gate bipolar transistors (MV-IGBTs) are considered as competitive solutions for the MV high-power (MV-HP) energy conversion market, compared to their alternative two-level counterparts based on the developing technology of the high-voltage (HV)-IGBTs, the integrated gate-commutated thyristors (IGCTs), or the gate turn-off thyristor (GTOs) [3]. The main converter topologies which have been commercialized by major manufactur-

ers are the neutral-point-clamped (NPC) converters, the cascaded multicell (CM) converters, the flying-capacitor (FC) multicell (FCM) converters, and the modular multilevel converters (MMCs) [4–8].

In 1979, A. Nabae, I. Takahashi, and H. Akagi invented the first pulse-width-modulation (PWM) NPC converter to drive a three-phase 200 V 2.2 kW 60 Hz squirrel-cage induction motor [9]. The three-level NPC configuration has now become an accepted and standard topology in industry for adjustable-speed drive (ASD) applications. For instance, the GE Power Conversion's MV-7000 ASD series are realized based on the three-level NPC topology, and provide a wide power range from 3 up to 101 MVA at output voltage from 3.3 kV up to 10 kV employing the IGCT or MV/HV-IGBT technology. The multiple clamping points, voltage imbalance, asymmetrical power loss distribution among semiconductor devices, and unimodular clamping diodes have restricted the NPC topology to the three-level configuration [10]. Complementing the passive neutral-point (NP) diodes by adding antiparallel active switches such as IGBTs, IGCTs, and GTOs provide a controllable path for neutral-point current to flow and overcomes the drawback of the uneven power loss distribution among semiconductor devices. The resultant topology is referred to as the active-neutral-point-clamped (ANPC) converter [11–13]. The PCS 8000 ASD series manufactured by ABB generates voltages from 6 kV up to 220 kV with a wide power range from 6 up to 100 MVA utilizing IGCT technology [1].

In 1977, J. Holtz invented a converter topology for HV and high-frequency applications which was built and tested using Thyristors for its phase-leg [14]. Later in 2009, this topology was named as the neutral-point-piloted (NPP) converter that is a suitable configuration for ASD applications [15]. The NPP converter uses bidirectional IGBTs to connect the phase output to the dc-link midpoint (*i.e.* NP) to generate the additional zero voltage-level and control the NP current. This topology is also referred to as the transistor-clamped converter (TCC) [4, 16] or the T-Type topology [17–21]. The NPP converter requires a HV-IGBTs or series connected MV-IGBTs for its upper and lower switches compared to its intermediate MV-IGBT switches. This impedes the topology's extension to higher voltage-levels and limits the converter structure to the three-level configuration.

The FC-based multilevel converter family including the FCM and stacked multicell (SM) converters were invented in 1990s by T. Meynard and H. Foch [22, 23]. The FCM and SM converter topologies employ imbricated cells comprising IGBTs and FCs in the form of a tandem/ladder or stack arrangements to realize the converter's phase-leg [24]. The redundant switching states are used in the FCM converters to achieve the proper voltage balance across FCs and clamp the voltage across the MV-IGBTs. The proper switching states for this multilevel topol-

ogy provides a correct commutation between adjacent cells to chop the dc-link voltage employing semiconductor devices and FCs. This makes it possible to regulate the FC voltages and synthesize different voltage-levels at the output nodes of the FCM converters without a need for an NP. The FCs might impose some practical limitations such as the excessive cost and accommodation space on the FCM converters. The FCM converters made their first appearance in MV-ASD market through ALSPA VDM6000 drive series by ALSTOM in the mid 1990's. The 3.3 kV 4.6 MVA ASD was built using a three-cell four-level IGBT-based FCM converter for pumps and train traction applications [25].

The extension of the three-level ANPC topology which is realized by combination of the NPC and FCM converters forms a new multilevel configuration which is referred to as the FC-based ANPC topology [26–28]. The FC-based ANPC converter is a promising multilevel topology for ASD applications which benefits from the robustness of the NPC along with the flexibility of the FCM converters [29, 30]. For example, ABB's ACS-2000 drive series employs the five-level FC-based ANPC converters at the heart of the ASD to generate the 4 kV, 4.16 kV, 6 kV, and 6.9 kV output voltages within a power range up to 3 MVA. Some new FC-based ANPC converter topologies are reported in [31, 32]. Improved modulation techniques for control of the ANPC converters to achieve a better performance have been implemented in [33–40]. In general, the stored energy, number, voltage and current ratings of the FCs are the limiting factors for FC-based multilevel converters. Thus, the optimization of the converter topology from the FCs point of view by reducing their voltage rating, stored energy, number, and modularization is of utmost importance. This brings the power converter and overall system's costs down and makes converter more practical for industrial and ASD applications.

Therefore, this paper proposes three topologies of duo-neutral-point-clamped (D-NPC), duo-active-neutral-point-clamped (D-ANPC), and duo-neutral-point-piloted (D-NPP) converters. The substantial reduction in the number of the HF-PWM MV-IGBTs, clamping diodes, and FCs, as well as a drastic abatement in the total voltage rating and total stored energy of the FCs are the most noteworthy advantages that these topologies offer over their classic counterparts. The circuit configurations and modulation techniques are verified through the experimental results which have been provided for all three D-ANPC, D-NPC, and D-NPP topologies.

2 Proposed Topologies

2.1 Duo-Active-Neutral-Point-Clamped (D-ANPC) Converter

The proposed D-ANPC converter's phase-leg is realized by adding the LF HV-IGBTs to the topology of a classic ANPC inverter. This results in a 50% reduction in the number of the HF MV-IGBTs and FCs [33]. To demonstrate the offered advantages, the 17-level classic FC-based topologies including the FCM, SM, and ANPC converters and the proposed 17-level D-ANPC converters are illustrated in Figs. 1-4 to provide a detailed topological comparison in the case of generating a 17-level 16 p.u. peak-to-peak voltage at the converters output nodes.

To generate a 17-level single-phase voltage with a peak-to-peak value of 16 p.u., the FCM converter would require a 16 p.u. DC-bus voltage, 16 HF-switching-cells, 32 HF MV-IGBTs with 1 p.u. voltage rating, 15 FCs with voltage ratings ranging from 1 p.u. to 15 p.u., and two DC-bus capacitors with voltage ratings of 8 p.u.. Thus, the total voltage rating and stored energy of the all DC-capacitors would be 136 p.u. and 684C J, respectively. The SM converter would require a 16 p.u. DC-bus voltage, 16 HF-switching-cells, 16 HF MV-IGBTs with 1 p.u. voltage rating, 16 HF MV-IGBTs with 2 p.u. voltage rating, two set of FCs wherein each set comprises 7 FCs with voltage ratings ranging from 1 p.u. to 7 p.u., and two DC-bus capacitors with voltage ratings of 8 p.u.. Therefore, the total voltage rating and stored energy of the all DC-capacitors would be 72 p.u. and 204C J, respectively. The ANPC converter would require a 16 p.u. DC-bus voltage, 8 HF-switching-cells, 16 HF MV-IGBTs with 1 p.u. voltage rating, 4 LF HV-IGBTs with 8 p.u. voltage rating, 7 FCs with voltage ratings ranging from 1 p.u. to 7 p.u., and two DC-bus capacitors with voltage ratings of 8 p.u.. So, the total voltage rating and stored energy of the all DC-capacitors would be 44 p.u. and 134C J, respectively. The D-ANPC converter would require a 8 p.u. DC-bus voltage, 4 HF-switching-cells, 8 HF MV-IGBTs with 1 p.u. voltage rating, 4 LF HV-IGBTs with 4 p.u. voltage rating, 2 LF HV-IGBTs with 8 p.u. voltage rating, 3 FCs with voltage ratings ranging from 1 p.u. to 3 p.u., and two DC-bus capacitors with voltage ratings of 4 p.u.. Therefore, the total voltage rating and stored energy of the all DC-capacitors would be 14 p.u. and 23C J, respectively.

Thus, the DC-capacitors' total voltage rating and stored energy in the 17-level D-ANPC converter are 10.2941% and 3.3626% of those values in the 17-level FCM converter, respectively. Accordingly, the DC-capacitors' total voltage rating and stored energy in the 17-level D-ANPC converter are 19.4444% and 11.2745% of those values in the 17-level SM converter, respectively. Ultimately, the DC-capacitors' total voltage rating and stored

energy in the 17-level D-ANPC converter are 31.8182% and 17.1642% of those values in the 17-level ANPC converter, respectively. It is worth pointing out that for sufficiently large number of voltage levels, these ratios tend to converge to the 6.25% and 1.5625%, respectively as compared to the FCM, 12.5% and 6.25%, respectively as compared to the SM, 25% and 12.5%, respectively as compared to the ANPC converter. This comparison is illustrated in Table. I for 17-level 16 p.u. peak-to-peak case. The same comparison is conducted for generalized cases and the results are depicted in Figs. 5-6 for voltage-levels from 5 up to 69. Therefore, the substantial reduction in number of the HF MV-IGBTs by 50% in comparison with classic ANPC converter, along with a drastic decrease in the total voltage rating and stored energy of the capacitors are the major advantages offered by the proposed D-ANPC topology over the FC-based multilevel converters. The derived equations for calculation of the total voltage ratings ($\mathcal{V}(n)$) and the stored energy ($\mathcal{E}(n)$) of the DC-link capacitors and FCs in the FCM, SM, ANPC, and the D-ANPC converters are given in the Appendix.

2.1.1 Proposed Modulation Technique

The proposed control technique employs phase-shifted carrier PWM (PSC-PWM) strategy wherein the triangular carriers are interleaved, phase shifted by $\frac{2\pi}{n}$, to achieve superior harmonic characteristics. The sinusoidal reference waveform ($\Psi(t)$) is represented in Eq. 1. The proposed switching technique is divided into two cases. The modulation index for the first case is considered $0.5 \leq M \leq 1$ while it is assumed $0 \leq M < 0.5$ in the second case. In the proposed control method, the PSC-PWM carriers band falls between 0.5 and 1, ($0.5 \leq \Omega(t) \leq 1$) and ($0.5 \leq \kappa_i(t) \leq 1$), as it is expressed in Eqs. 2-3. The intersection angle of the sinusoidal reference waveform with the constant value of $d(t) = 0.5$ is determined through Eq. 4. Using the zero-crossing angle of the $\Psi(t)$ and the intersection angle of ϑ , four pulses of $\Gamma(t)$, $\gamma_1(t)$, $\gamma_2(t)$, and $\gamma_3(t)$ are generated to be added to the $\Psi(t)$ to form a reference waveform which is bounded between 0.5 and 1 for PWM comparison with $\kappa_i(t)$ carriers. This bounded reference waveform is called $\chi(t)$ and is represented in Eq. 9. The $\chi(t)$ derivation method is illustrated in Fig. 7 for the first case wherein $M = 1$ and $\vartheta = \frac{\pi}{6}$. The LF HV-IGBT of S_T is modulated using $\Gamma(t)$, the LF HV-IGBT of S_J is controlled using PWM comparison of $(\Psi(t) + \Gamma(t))$ and a constant value of $d(t) = 0.5$, and the HF MV-IGBTs of $S_{(n-i+1)}$ are switched ON and OFF through the PWM comparison of $\chi(t)$ and the carrier of $\kappa_i(t)$. This is expressed in Eqs. 10-12 and illustrated in Fig. 8 for the first case wherein $M = 1$ and $\vartheta = \frac{\pi}{6}$. It is worth pointing out that

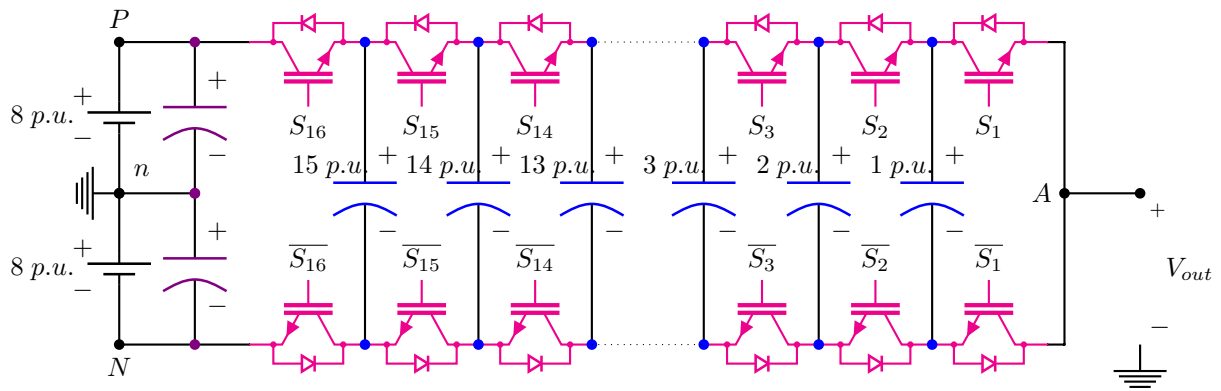


Figure 1: A 16-cell 17-level 16 p.u. peak-to-peak FCM converter.

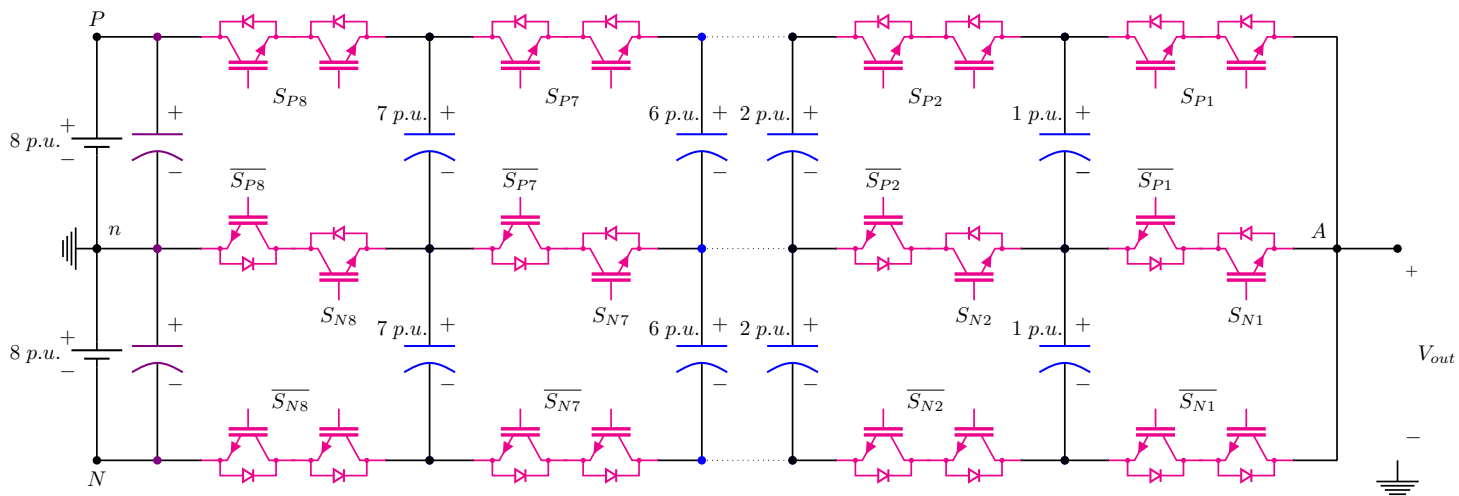


Figure 2: A 16-cell 17-level 16 p.u. peak-to-peak SM converter.

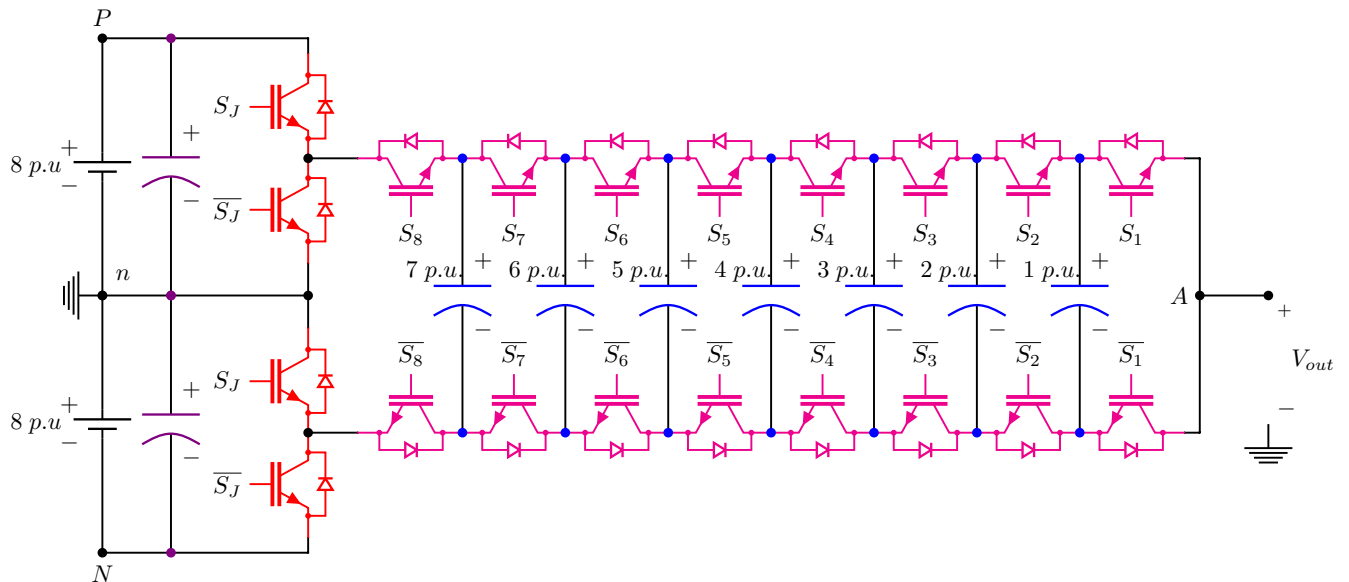


Figure 3: An 8-cell 17-level 16 p.u. peak-to-peak ANPC converter.

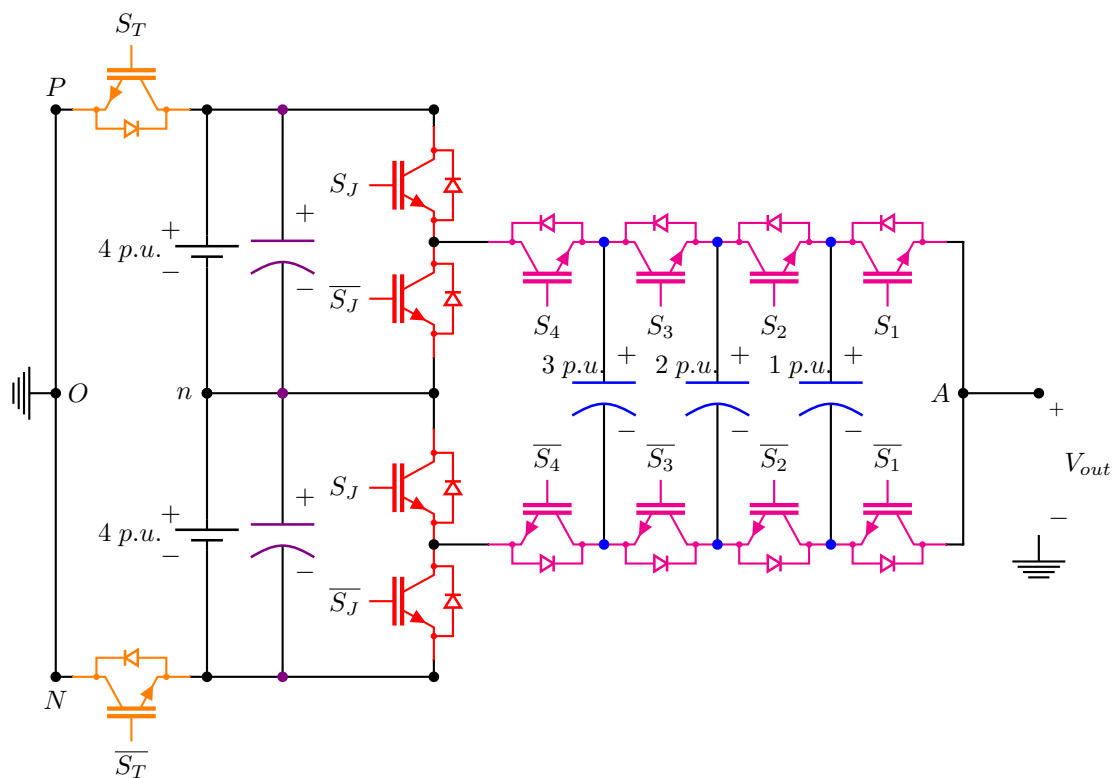


Figure 4: A 4-cell 17-level 16 p.u. peak-to-peak proposed D-ANPC converter.

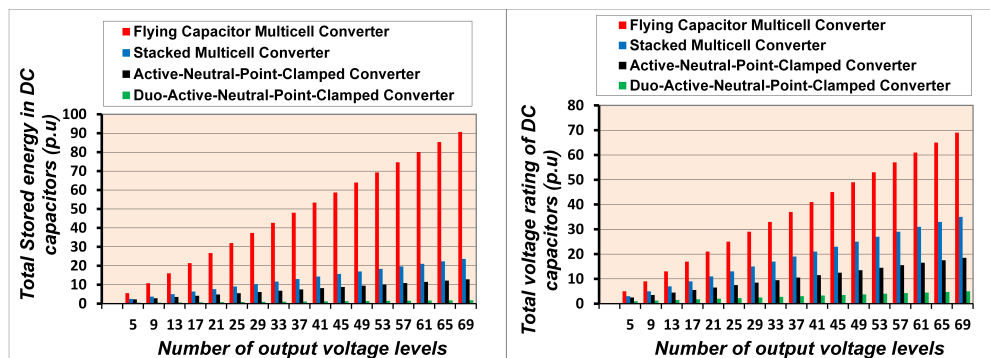


Figure 5: Capacitors total stored energy and voltage rating comparison in FCM, SM, ANPC, and D-ANPC converters [33].

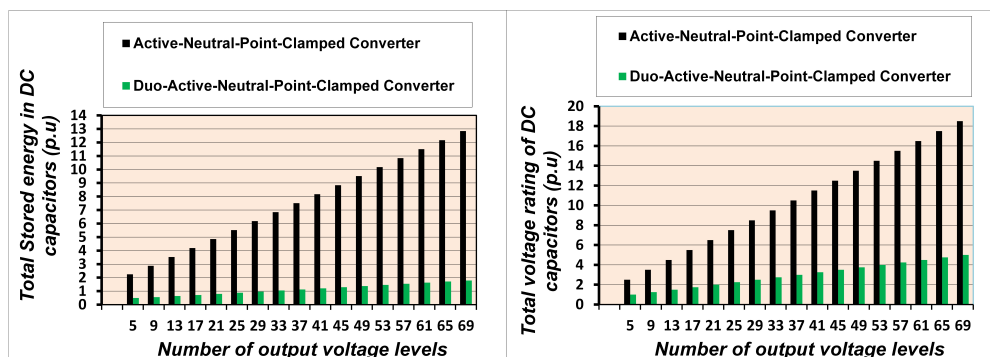


Figure 6: Capacitors total stored energy and voltage rating comparison in ANPC and D-ANPC converters [33].

Table 1: Comparison among the conventional multilevel topologies and the proposed D-ANPC converter for generating an identical output voltage (i.e., 17-level, 16 p.u. peak-to-peak.)

Type of multilevel converter	No. of cells	No. of HF switches (α)	No. of LF switches (β)	No. of DC capacitors (DC link and FCs)	Voltage rating of HF switches (p.u)(γ)	Voltage rating of LF switches (p.u)(λ)	Voltage rating of DC sources (p.u)	Voltage rating of capacitors (DC link and FCs) (p.u)	No. of HF modular switches ($\alpha \times \gamma$)	No. of LF modular switches ($\beta \times \lambda$)
FCM	16	32	0	17	1	0	16	First type: 1 to 15 p.u. Second type: Two 8 p.u.: (2× 8 p.u.)	32	0
SM	2×8	32	0	16	16 switches: are 1 p.u. 16 switches: are 2 p.u.	0	16	Two series: 1 to 8 p.u.	48	0
ANPC	8	16	4	9	1	8	16	First Type: 1 to 7 p.u. Second type: Two 8 p.u.: (2× 8 p.u.)	16	32
D-ANPC	4	8	6	5	1	4 switches: are 4 p.u. 2 switches: are 8 p.u.	8	First Type: 1 to 3 Second type: Two 4 p.u.: (2× 4 p.u.)	8	32

M is the modulation index, f_r is the reference frequency, f_c and T_c are the triangular carrier waveform frequency (f_{sw}) and period, respectively, and E_c is the carrier amplitude. Moreover, $\omega_r = 2\pi f_r$, $\omega_c = 2\pi f_c$, $f_c = 1/T_c$, $i = 1, 2, 3, \dots, n$, and $q \in \mathbb{Z}^+$. $\alpha_i(t)$ is the control pulse for $S_{(n-i+1)}$ within $(n-i+1)^{th}$ -HF cells of the D-ANPC converter.

$$\Gamma(t) = \begin{cases} 0 & -\varphi \leq \omega_r t < \pi - \varphi \\ 1 & \pi - \varphi \leq \omega_r t < 2\pi - \varphi \end{cases} \quad (4)$$

$$\gamma_1(t) = \begin{cases} 0.5 & -\varphi \leq \omega_r t < \vartheta - \varphi \\ 0 & \vartheta - \varphi \leq \omega_r t < 2\pi - \varphi \end{cases} \quad (5)$$

$$\gamma_2(t) = \begin{cases} 0 & -\varphi \leq \omega_r t < \pi - \vartheta - \varphi \\ 0.5 & \pi - \vartheta - \varphi \leq \omega_r t < \pi - \varphi \\ 0 & \pi - \varphi \leq \omega_r t < 2\pi - \varphi \end{cases} \quad (6)$$

$$\Psi(t) = M \sin(\omega_r t + \varphi) \quad -\varphi \leq \omega_r t < 2\pi - \varphi \quad (1)$$

$$\gamma_3(t) = \begin{cases} 0 & -\varphi \leq \omega_r t < \pi + \vartheta - \varphi \\ 0.5 & \pi + \vartheta - \varphi \leq \omega_r t < 2\pi - \vartheta - \varphi \\ 0 & 2\pi - \vartheta - \varphi \leq \omega_r t < 2\pi - \varphi \end{cases} \quad (7)$$

$$\Omega(t) = \begin{cases} (2E_c - 1) \times \left(\frac{t}{T_c} - q \right) + 0.5 & qT_c \leq t \leq qT_c + \frac{T_c}{2} \\ -(2E_c - 1) \times \left(\frac{t}{T_c} - q - 1 \right) + 0.5 & qT_c + \frac{T_c}{2} \leq t \leq (q+1)T_c \end{cases}$$

$$\chi(t) = \Psi(t) + \Gamma(t) + \gamma_1(t) + \gamma_2(t) + \gamma_3(t) \quad 0.5 \leq M \leq 1 \quad (8)$$

$$\kappa_i(t) = \Omega\left(t + \frac{(i-1)T_c}{n}\right) \quad (2)$$

$$S_T(t) = \Gamma(t) \quad (9)$$

$$\vartheta = \sin^{-1}\left(\frac{1}{2M}\right) \quad 0.5 \leq M \leq 1 \quad (3)$$

$$S_J(t) = \begin{cases} 1 & 0.5 \leq (\Psi(t) + \Gamma(t)) \\ 0 & 0.5 > (\Psi(t) + \Gamma(t)) \end{cases} \quad (10)$$

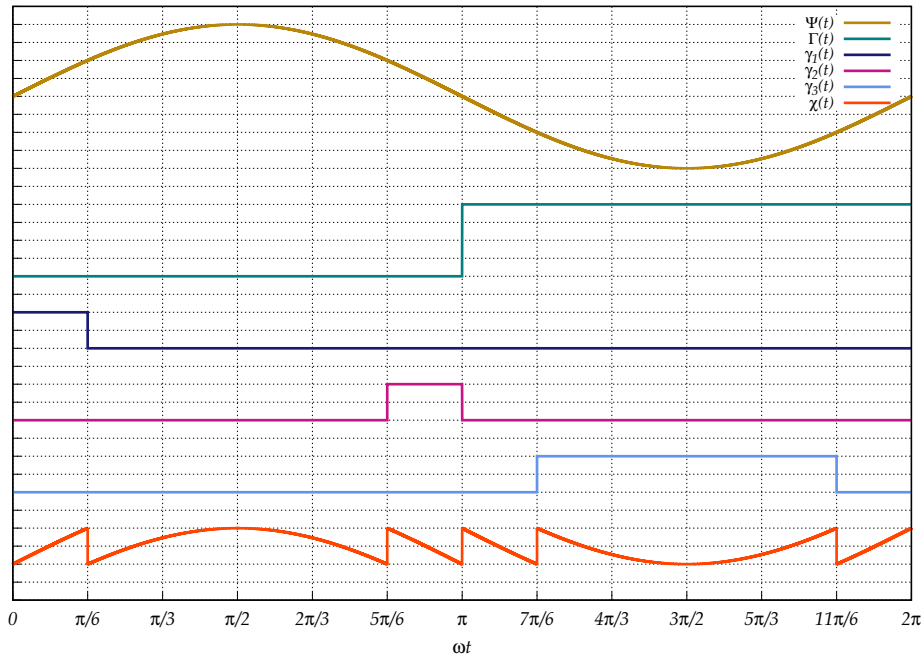


Figure 7: Derivation of the bounded reference waveform $\chi(t)$ for the first case of the $0.5 \leq M \leq 1$ using four pulses of $\Gamma(t) + \gamma_1(t) + \gamma_2(t) + \gamma_3(t)$: $M = 1$ and $\vartheta = \frac{\pi}{6}$.

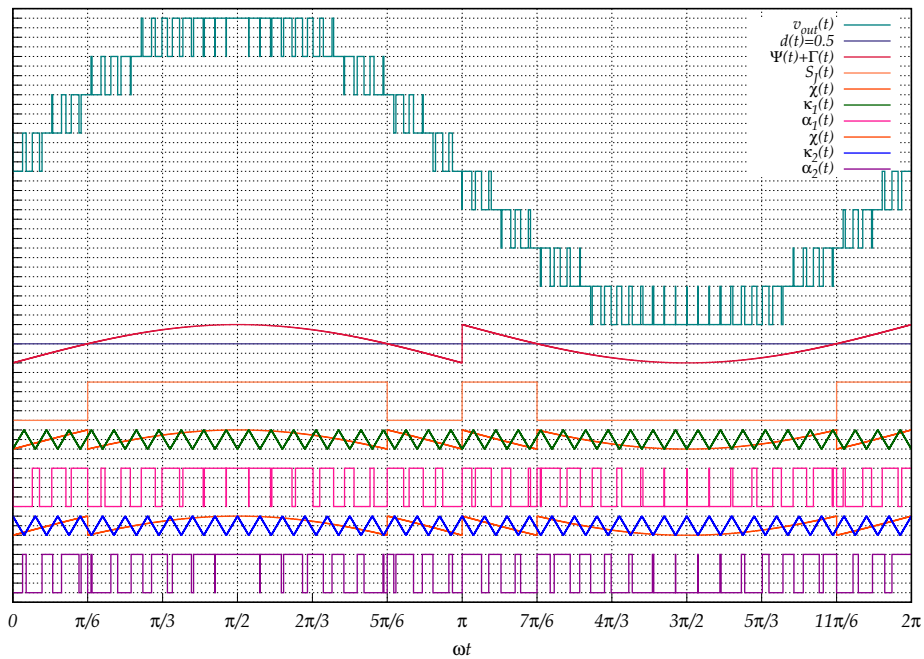


Figure 8: Generating the IGBTs switching pulses for the first case of the $0.5 \leq M \leq 1$ using bounded reference waveform $\chi(t)$, $\Psi(t) + \Gamma(t)$, $\kappa_i(t)$, and $d(t) = 0.5$: $M = 1$ and $\vartheta = \frac{\pi}{6}$.

$$\alpha_i(t) = \begin{cases} 1 & \kappa_i(t) \leq \chi(t) \\ 0 & \kappa_i(t) > \chi(t) \end{cases} \quad (11)$$

The control and switching pulses for the second case ($0 \leq M < 0.5$) are derived in Eqs. 13-17 and are illustrated in Figs. 9-10 for $M = 0.499$.

$$\eta(t) = \begin{cases} 0.5 & -\varphi \leq \omega_r t < \pi - \varphi \\ 0 & \pi - \varphi \leq \omega_r t < 2\pi - \varphi \end{cases} \quad (12)$$

$$\chi(t) = \Psi(t) + \Gamma(t) + \eta(t) \quad 0 \leq M < 0.5 \quad (13)$$

$$S_T(t) = \Gamma(t) \quad (14)$$

$$S_J(t) = \begin{cases} 1 & 0.5 \leq (\Psi(t) + \Gamma(t)) \\ 0 & 0.5 > (\Psi(t) + \Gamma(t)) \end{cases} \quad (15)$$

$$\alpha_i(t) = \begin{cases} 1 & \kappa_i(t) \leq \chi(t) \\ 0 & \kappa_i(t) > \chi(t) \end{cases} \quad (16)$$

2.2 Duo-Neutral-Point-Clamped (D-NPC) Converter

The proposed D-NPC converter's phase-leg is formed by adding the LF HV-IGBTs to the classic NPC converter's topology. This leads into a 50% reduction in the number of the HF MV-IGBTs and clamping-points along with a significant decrease in the number of the clamping-diodes. For example, to generate a 5-level single-phase voltage with a peak-to-peak value of 4 p.u., the NPC converter would require a 4 p.u. DC-bus voltage, 8 HF MV-IGBTs with 1 p.u. voltage rating, and 12 clamping-diodes with voltage ratings of 1 p.u.. The proposed five-level D-NPC converter which is shown in Fig. 11 would require a 2 p.u. DC-bus voltage, 4 HF MV-IGBTs with 1 p.u. voltage rating, 2 clamping-diodes with voltage ratings of 1 p.u., and 2 LF HV-IGBTs with a 2 p.u. voltage rating.

2.3 Duo-Neutral-Point-Piloted (D-NPP) Converter

Adding the LF HV-IGBTs to the conventional NPP converter's topology forms the proposed D-NPP converter's phase-leg. A significant decrease in the number of the HF MV-IGBTs is achieved through this topology modification. Fig. 12 shows the the proposed five-level configuration of the D-NPP topology. To generate a 5-level single-phase voltage with a peak-to-peak value of 4 p.u., the NPP converter would require a 4 p.u. DC-bus voltage and 20 HF MV-IGBTs with 1 p.u. voltage rating,

whereas the proposed D-NPP converter requires a 2 p.u. DC-bus voltage, 6 HF MV-IGBTs with 1 p.u. and 2 LF HV-IGBTs with 2 p.u. voltage ratings. It is worth pointing out that the proposed D-NPC and D-NPP converters are the same in the control, modulation, functionality, and generating the same multilevel-voltage waveform.

3 Experimental Results

To validate the proposed D-ANPC, D-NPC, and D-NPP converter topologies, the laboratory prototypes of the 3-level and 5-level ANPC, 5-level and 9-level D-ANPC, 5-level D-NPC, and 5-level D-NPP converters were built. The TMS320F28335 digital micro-processor from TI has been used to implement the proposed modulation techniques for control of the classic and proposed multilevel converters. The switching frequency, modulation index, and RL load for all converters were $f_{sw} = 5$ kHz, $M = 0.95$, and 24Ω -15mH.

3.1 Duo-Active-Neutral-Point-Clamped Converter

The experimentally measured two and one cycles ($f_r = 50$ Hz) of the output voltage ($v_{out}(t)$) and load current ($i_{out}(t)$) along with the harmonic content (FFT) of the 3-level ANPC converter's generated multilevel voltage as well as the low-frequency and high-frequency switching pulses are depicted in Fig. 13. The DC-link voltage was 300 V. The voltage harmonics occur around $\psi \times f_{sw}$ where ψ is an integer number. As presented, the voltage harmonics are placed at $\psi \times 5000$ including the 5 kHz, 10 kHz, etc. The THD of the 3-level ANPC converter's phase-voltage is approximately 59%.

The experimentally measured two and one cycles ($f_r = 50$ Hz) of the output voltage ($v_{out}(t)$) and load current ($i_{out}(t)$) along with the harmonic content (FFT) of the 5-level ANPC converter's generated multilevel voltage as well as the low-frequency and high-frequency switching pulses are depicted in Figs. 14-15. The DC-link voltage was 300 V. The transient and steady states dynamics of the FC voltage is illustrated in Fig. 16. As demonstrated, the FC voltage is regulated and balanced naturally at 75 V. The voltage harmonics occur around $\psi \times 2 \times f_{sw}$ where ψ is an integer number. As presented, the voltage harmonics are placed at $\psi \times 2 \times 5000$ including the 10 kHz, 20 kHz, etc. The THD of the 5-level ANPC converter's phase-voltage is approximately 31%.

The experimentally measured two and one cycles ($f_r = 50$ Hz) of the output voltage ($v_{out}(t)$) and load current ($i_{out}(t)$) along with the harmonic content (FFT) of the 5-level D-ANPC converter's generated multilevel voltage as well as the low-frequency and high-frequency switching pulses are depicted in Figs. 17-18. The DC-link

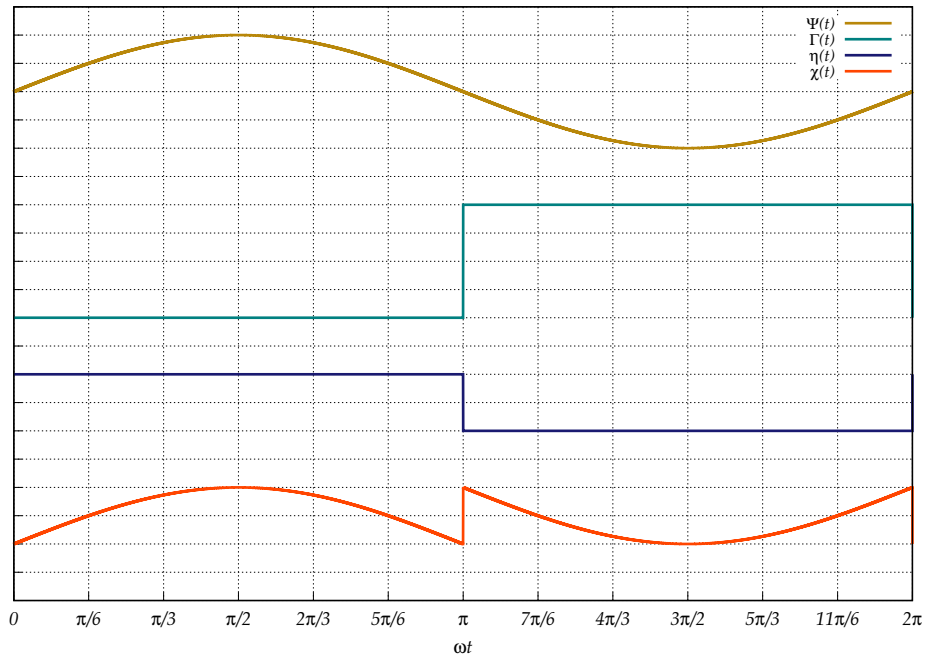


Figure 9: Derivation of the bounded reference waveform $\chi(t)$ for the second case of the $0 \leq M < 0.5$ using two pulses of $\Gamma(t) + \eta(t)$: $M = 0.499$.

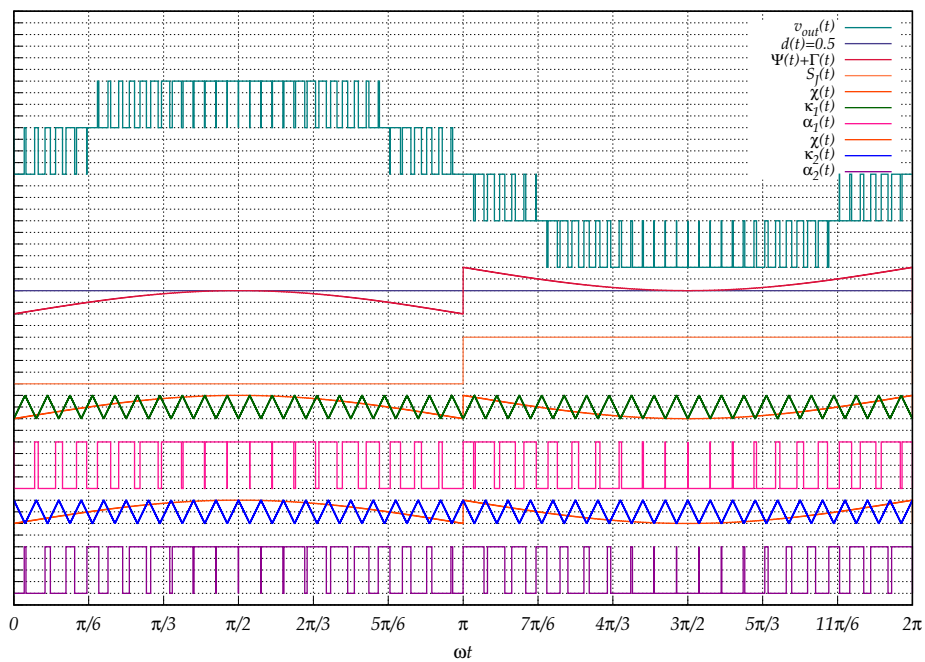


Figure 10: Generating the IGBTs switching pulses for the second case of the $0 \leq M < 0.5$ using bounded reference waveform $\chi(t)$, $\Psi(t) + \Gamma(t)$, $\kappa_i(t)$, and $d(t) = 0.5$: $M = 0.499$.

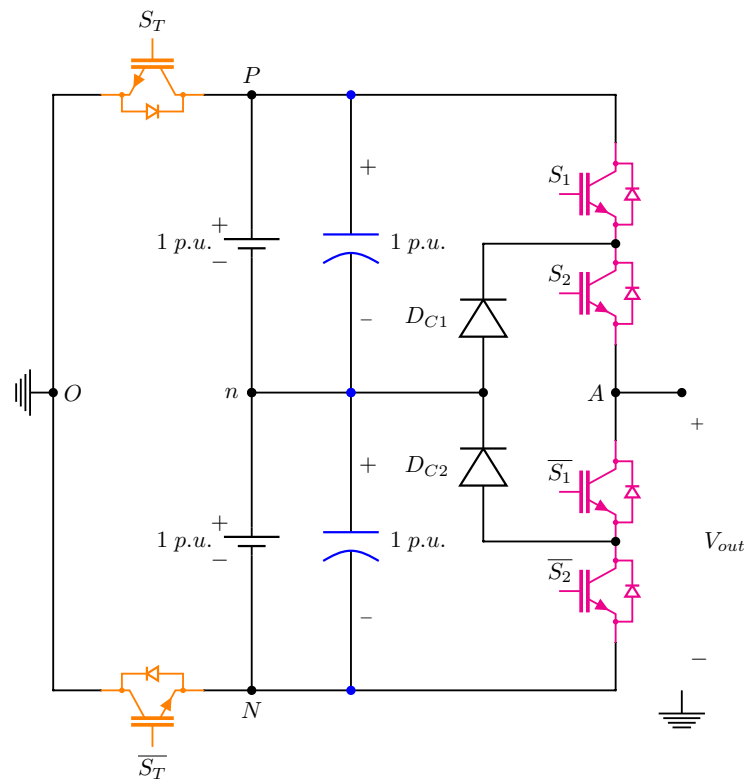


Figure 11: A 5-level 4 p.u. peak-to-peak proposed D-NPC converter.

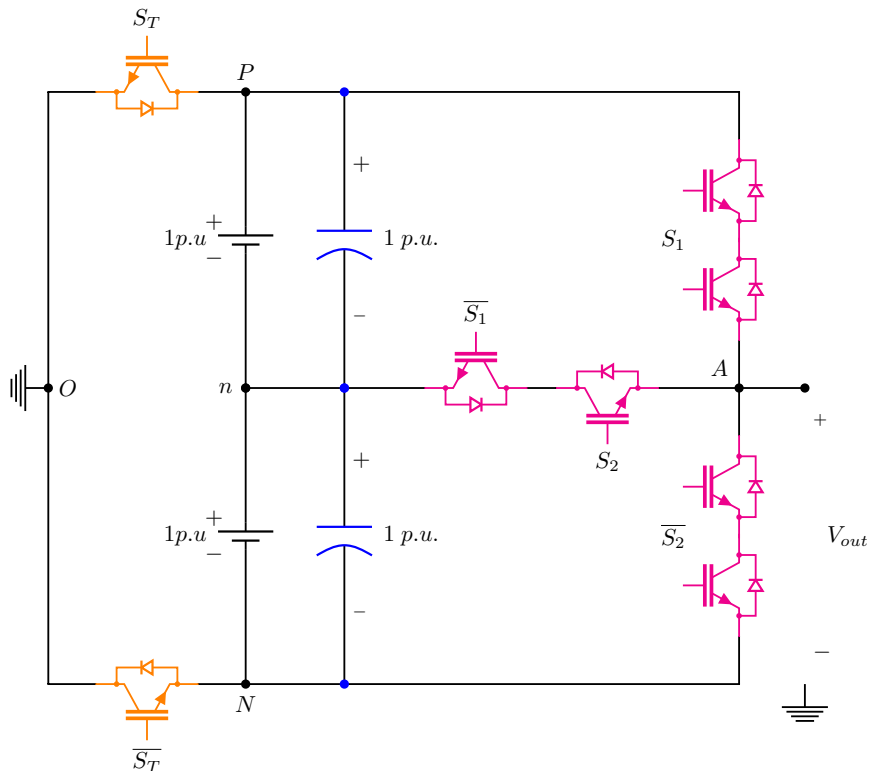


Figure 12: A 5-level 4 p.u. peak-to-peak proposed D-NPP converter.

voltage was 300 V. The voltage harmonics occur around $\psi \times f_{sw}$ where ψ is an integer number. As presented, the voltage harmonics are placed at $\psi \times 5000$ including the 5 kHz, 10 kHz, etc. The THD of the 5-level ANPC converter's phase-voltage is approximately 32.2%.

The experimentally measured two and one cycles ($f_r = 50$ Hz) of the output voltage ($v_{out}(t)$) and load current ($i_{out}(t)$) along with the harmonic content (FFT) of the 9-level D-ANPC converter's generated multilevel voltage as well as the low-frequency and high-frequency switching pulses are depicted in Figs. 19-21. The DC-link voltage was 300 V. The transient and steady states dynamics of the FC voltage is illustrated in Fig. 22. As demonstrated, the FC voltage is regulated and balanced naturally at 75 V utilizing the proposed modulation technique. The voltage harmonics occur around $\psi \times 2 \times f_{sw}$ where ψ is an integer number. As presented, the voltage harmonics are placed at $\psi \times 2 \times 5000$ including the 10 kHz, 20 kHz, etc. The THD of the 9-level D-ANPC converter's phase-voltage is approximately 16%.

As demonstrated, adding the LF HV-IGBTs to the topology of the classic ANPC multilevel converters for realizing the D-ANPC converters phase-leg improves the harmonic content of the generated phase-voltage significantly through doubling the number of the voltage-levels and consequently halving the voltage THD.

3.2 Duo-Neutral-Point-Clamped Converter

The experimentally measured two and one cycles ($f_r = 50$ Hz) of the output voltage ($v_{out}(t)$) and load current ($i_{out}(t)$) along with the harmonic content (FFT) of the 5-level D-NPC converter's generated multilevel voltage as well as the low-frequency and high-frequency switching pulses are depicted in Figs. 23-25. The DC-link voltage was 400 V. The voltage harmonics occur around $\psi \times f_{sw}$ where ψ is an integer number. As presented, the voltage harmonics are placed at $\psi \times 5000$ including the 5 kHz, 10 kHz, etc.

3.3 Duo-Neutral-Point-Piloted Converter

The experimentally measured two and one cycles ($f_r = 50$ Hz) of the output voltage ($v_{out}(t)$) and load current ($i_{out}(t)$) along with the harmonic content (FFT) of the 5-level D-NPP converter's generated multilevel voltage as well as the low-frequency and high-frequency switching pulses are depicted in Figs. 24-29. The DC-link voltage was 300 V. The voltage harmonics occur around $\psi \times f_{sw}$ where ψ is an integer number. As presented, the voltage harmonics are placed at $\psi \times 5000$ including the 5 kHz, 10 kHz, etc.

4 Conclusion

This paper proposed D-NPC, D-ANPC, and D-NPP topologies for multilevel converters. The phase-leg of the proposed topologies is realized by adding LF HV-IGBTs to their structures. This leads to a significant decrease in the number of the HF MV-IGBTs, clamping diodes, and FCs. In addition, a drastic reduction in the total voltage rating and total stored energy of the FCs within the D-ANPC topology is achieved compared to the classic ANPC configuration. It was concluded that adding the LF HV-IGBTs improves the harmonics content of the phase-voltage. This was accomplished through doubling the number of the voltage-levels. The experimental results were provided for 3-level ANPC, 5-level ANPC, 5-level D-ANPC, 9-level D-ANPC, 5-level D-NPC, and 5-level D-NPP converters to demonstrate the operational fundamentals of the proposed topologies and validate the modulation method for control of the multilevel converters.

5 Appendix

The total voltage ratings ($\mathcal{V}(n)$) and the stored energy ($\mathcal{E}(n)$) of the DC-link capacitors and FCs in the $4n + 1$ -level converters with $2E$ peak-to-peak and $4n$ -p.u. output voltage, are calculated as follows [33]:

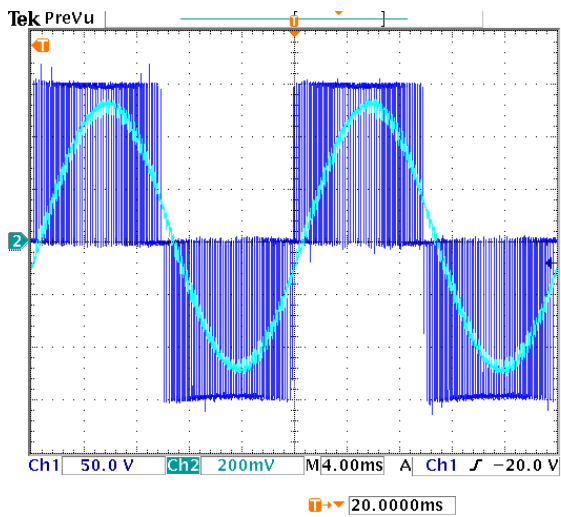
$$\begin{aligned} \mathcal{E}(n)_{FCM} &= \sum_{i=1}^{4n-1} \frac{C}{2} \left(i \times \frac{2E}{4n} \right)^2 + 2 \times \frac{C}{2} (E)^2 \\ &= \left(\frac{32n^2 + 1}{12n} \right) CE^2 \end{aligned} \quad (17)$$

$$\mathcal{V}(n)_{FCM} = \sum_{i=1}^{4n-1} \left(i \times \frac{2E}{4n} \right) + 2 \times (E) = (4n + 1) E \quad (18)$$

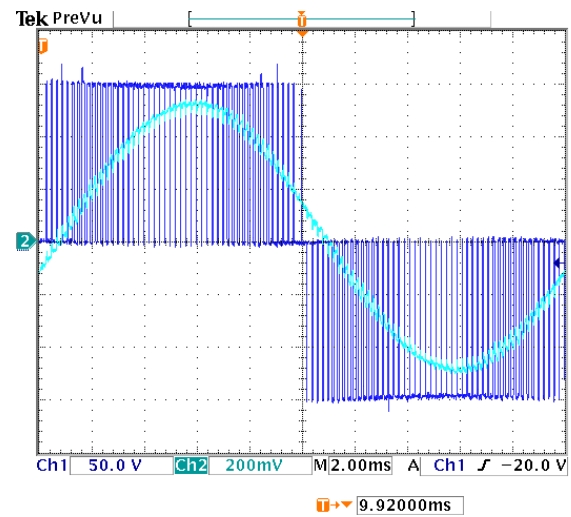
$$\mathcal{E}(n)_{SM} = 2 \times \sum_{i=1}^{2n} \frac{C}{2} \left(i \times \frac{E}{2n} \right)^2 = \left(\frac{8n^2 + 6n + 1}{12n} \right) CE^2 \quad (19)$$

$$\mathcal{V}(n)_{SM} = 2 \times \sum_{i=1}^{2n} \left(i \times \frac{E}{2n} \right) = (2n + 1) E \quad (20)$$

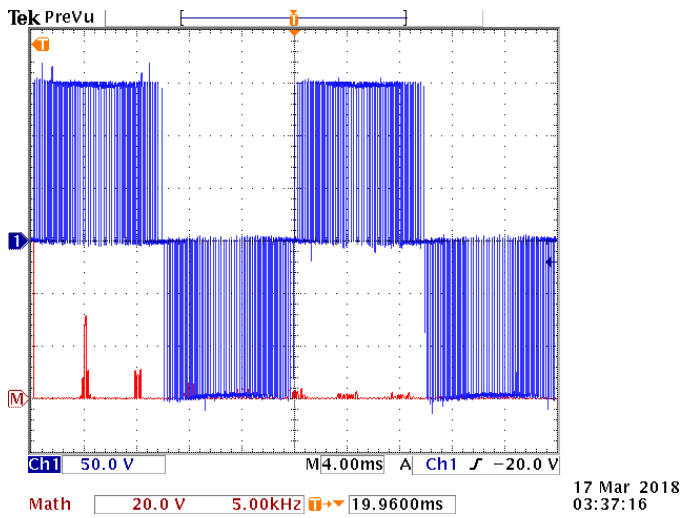
$$\begin{aligned} \mathcal{E}(n)_{ANPC} &= \sum_{i=1}^{2n-1} \frac{C}{2} \left(i \times \frac{E}{2n} \right)^2 + 2 \times \frac{C}{2} (E)^2 \\ &= \left(\frac{8n^2 + 18n + 1}{24n} \right) CE^2 \end{aligned} \quad (21)$$



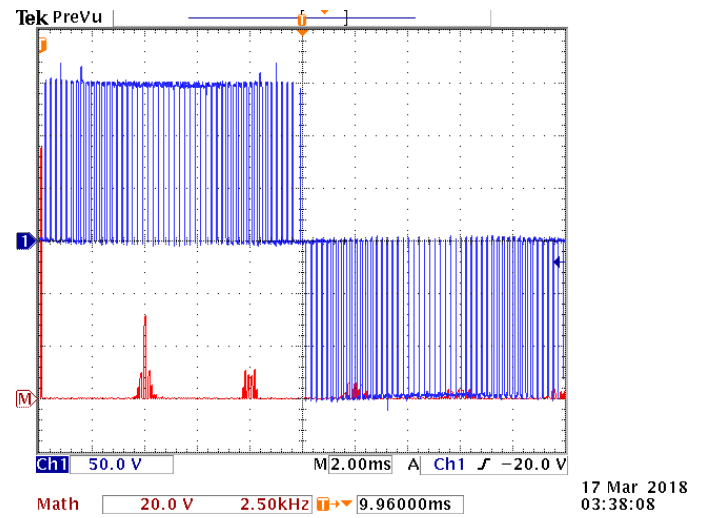
(a) Ch1: v_{out} : 50 V/Div; Ch2: i_{out} : 2 A/Div



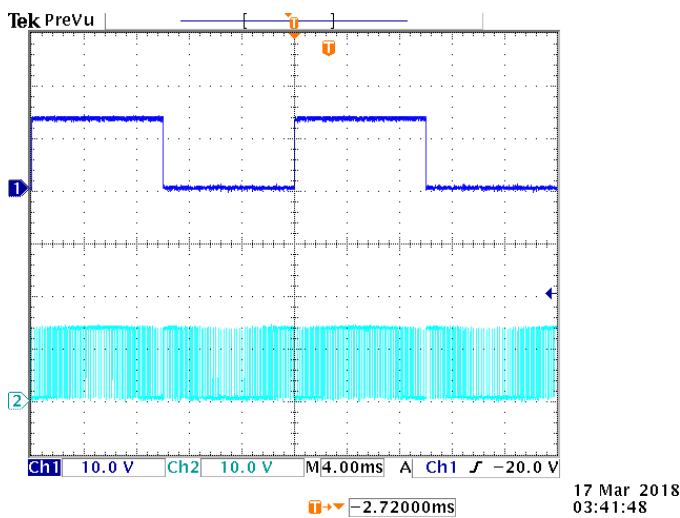
(b) Ch1: v_{out} : 50 V/Div; Ch2: i_{out} : 2 A/Div



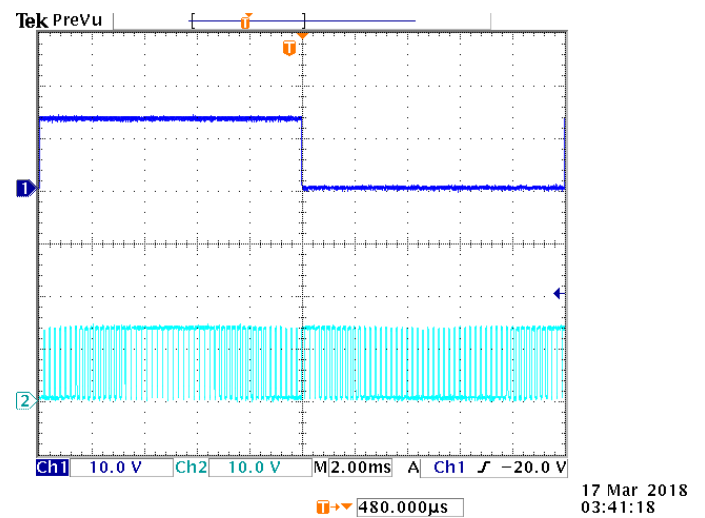
(c) Ch1: 50 V/Div, Math: 20 V/Div, 5 kHz/Div



(d) Ch1: v_{out} : 50 V/Div; Math: FFT: 20 V/Div, 2.5 kHz/Div

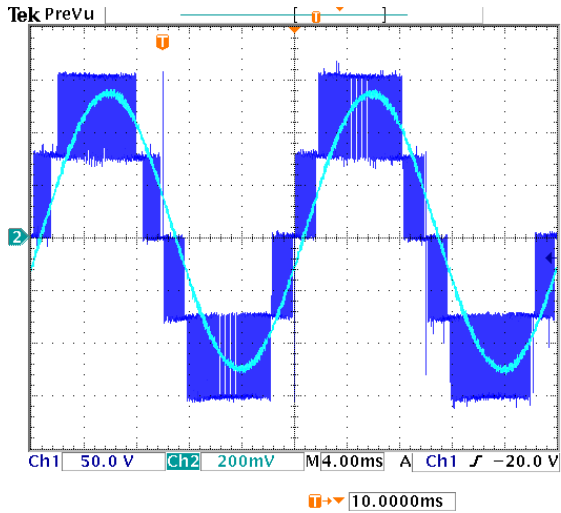


(e) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_1(t)$: 10 V/Div

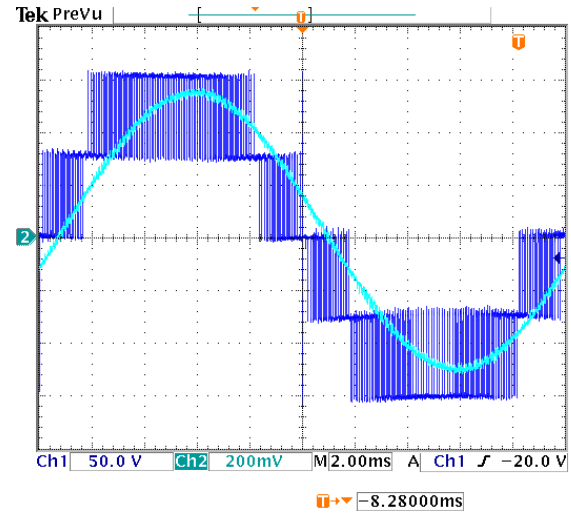


(f) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_1(t)$: 10 V/Div

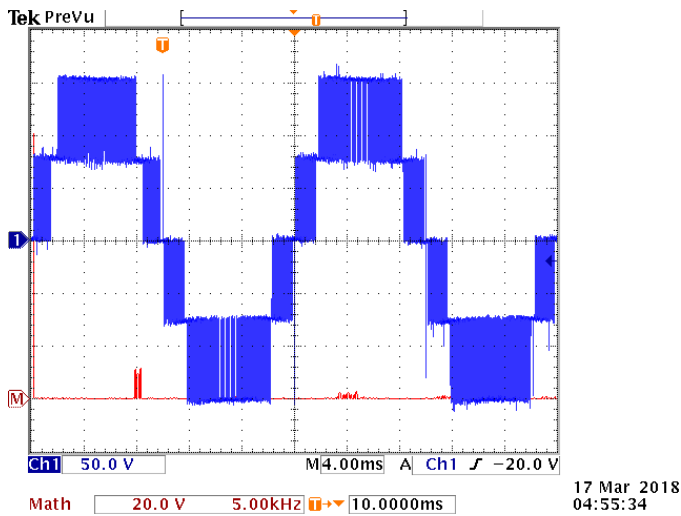
Figure 13: Experimental results for a 3-Level ANPC multilevel converter.



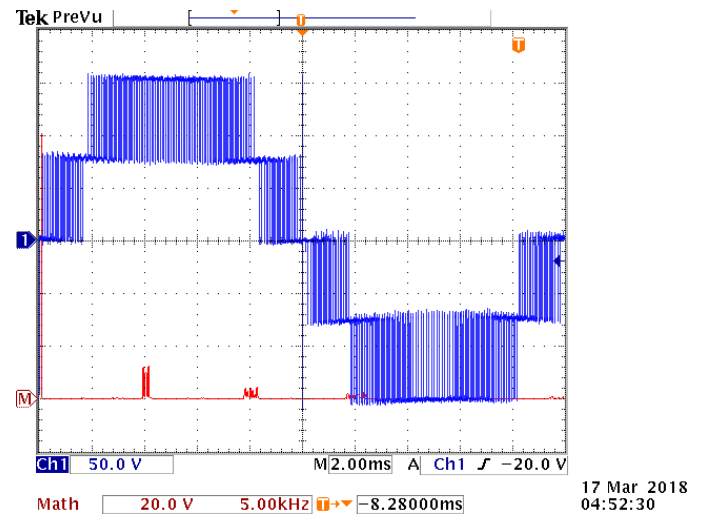
(a) Ch1: v_{out} : 50 V/Div; Ch2: i_{out} : 2 A/Div



(b) Ch1: v_{out} : 50 V/Div; Ch2: i_{out} : 2 A/Div

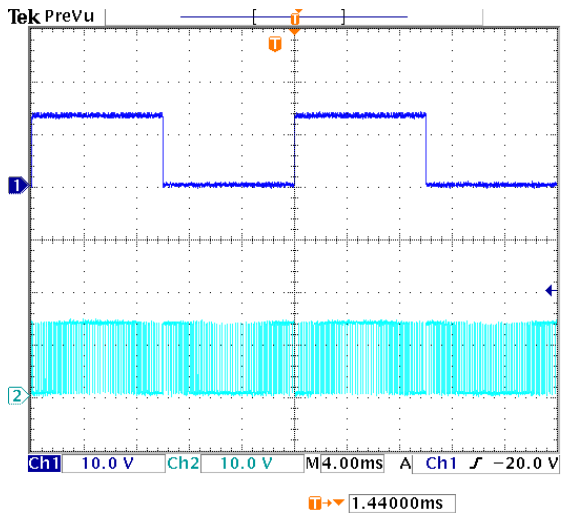


(c) Ch1: v_{out} : 50 V/Div; Math: FFT: 20 V/Div, 5 kHz/Div

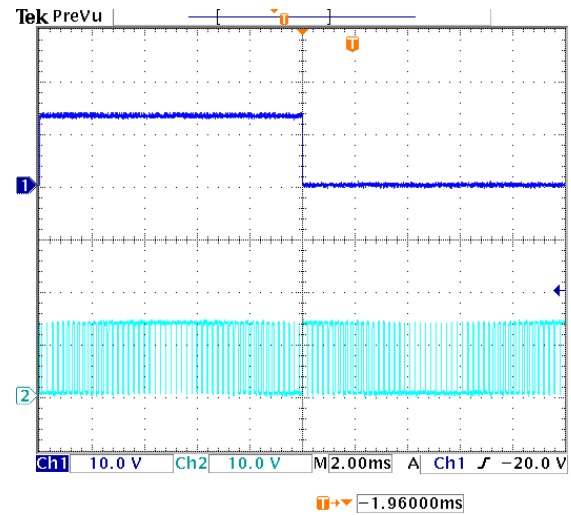


(d) Ch1: v_{out} : 50 V/Div; Math: FFT: 20 V/Div, 5 kHz/Div

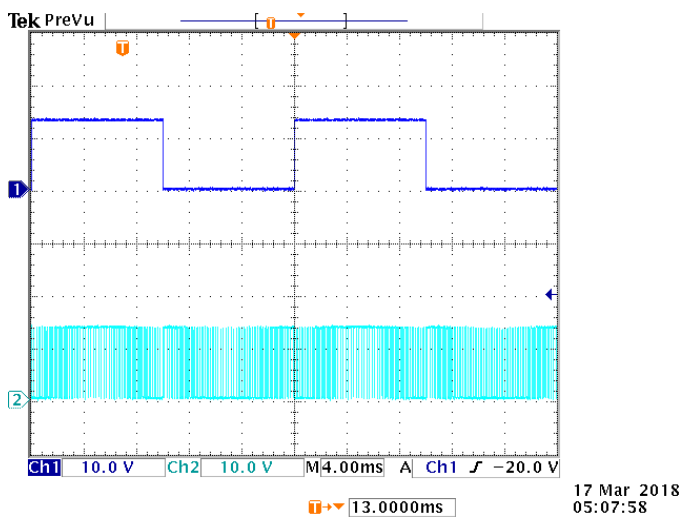
Figure 14: Experimental results for a 5-Level ANPC multilevel converter.



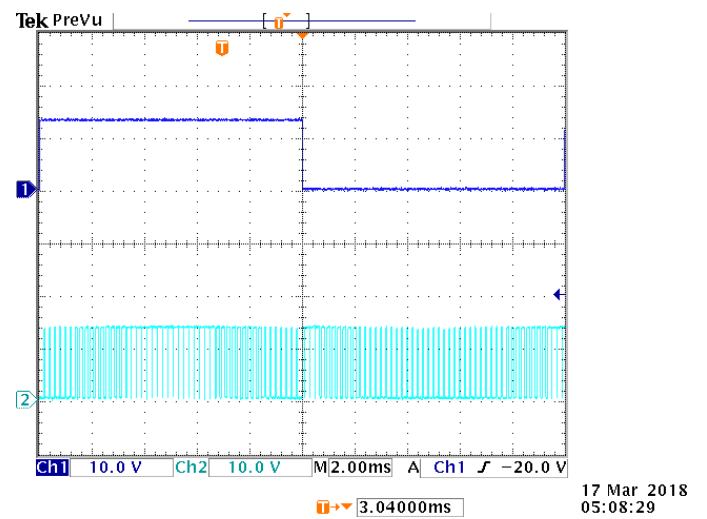
(a) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_1(t)$: 10 V/Div



(b) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_1(t)$: 10 V/Div



(c) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div



(d) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div

Figure 15: Experimental results for a 5-Level ANPC multilevel converter.

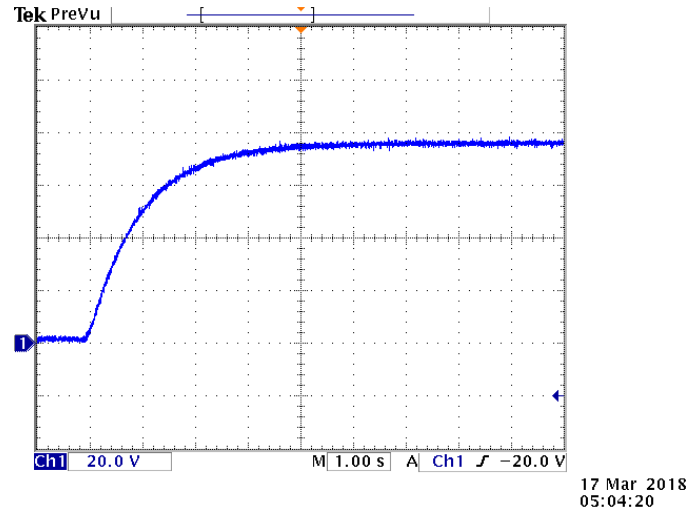


Figure 16: Transient and steady states dynamics in a 5-Level ANPC multilevel converter; Ch1: $v_{FC}(t)$: 20 V/Div.

$$\mathcal{V}(n)_{ANPC} = \sum_{i=1}^{2n-1} \left(i \times \frac{E}{2n} \right) + 2 \times (E) = (n + 1.5) E \quad (22)$$

$$\lim_{n \rightarrow +\infty} \frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{SM}} \approx \left(\frac{1}{2} \right)^3 = 0.125 = 12.5\% \quad (29)$$

$$\begin{aligned} \mathcal{E}(n)_{D-ANPC} &= \sum_{i=1}^{n-1} \frac{C}{2} \left(i \times \frac{E}{2n} \right)^2 + 2 \times \frac{C}{2} (E/2)^2 \\ &= \left(\frac{2n^2 + 9n + 1}{48n} \right) CE^2 \end{aligned} \quad (23)$$

$$\lim_{n \rightarrow +\infty} \frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{FCM}} \approx \left(\frac{1}{2} \right)^4 = 0.0625 = 6.25\% \quad (30)$$

$$\begin{aligned} \mathcal{V}(n)_{D-ANPC} &= \sum_{i=1}^{n-1} \left(i \times \frac{E}{2n} \right) + 2 \times (E/2) \\ &= (0.25n + 0.75) E \end{aligned} \quad (24)$$

References

For sufficiently large number of voltage-levels, the ratio of $\mathcal{V}(n)$ and $\mathcal{E}(n)$ converges to the following numbers:

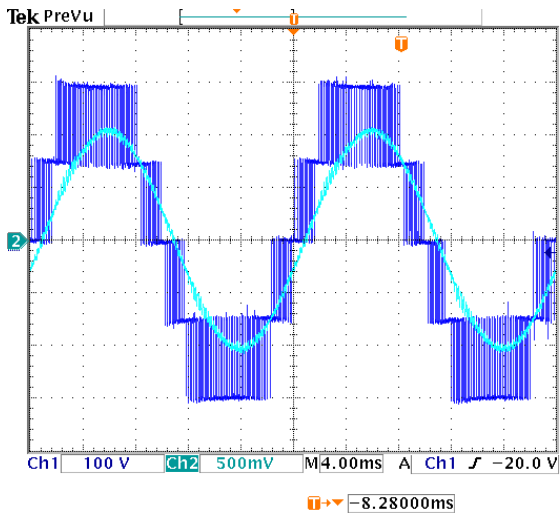
$$\lim_{n \rightarrow +\infty} \frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{ANPC}} \approx \left(\frac{1}{2} \right)^3 = 0.125 = 12.5\% \quad (25)$$

$$\lim_{n \rightarrow +\infty} \frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{SM}} \approx \left(\frac{1}{2} \right)^4 = 0.0625 = 6.25\% \quad (26)$$

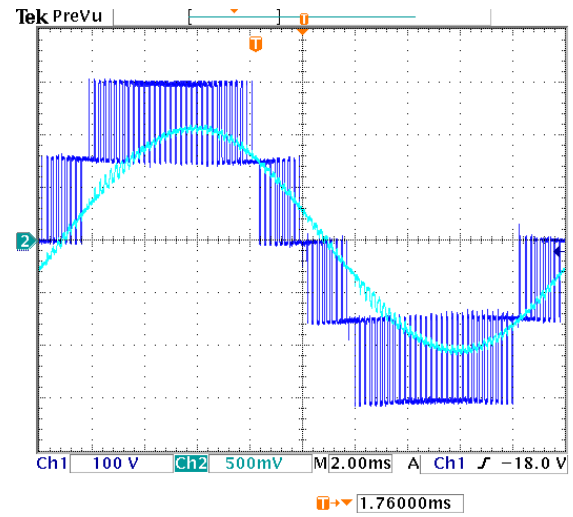
$$\lim_{n \rightarrow +\infty} \frac{\mathcal{E}(n)_{D-ANPC}}{\mathcal{E}(n)_{FCM}} \approx \left(\frac{1}{2} \right)^6 = 0.015625 = 1.5625\% \quad (27)$$

$$\lim_{n \rightarrow +\infty} \frac{\mathcal{V}(n)_{D-ANPC}}{\mathcal{V}(n)_{ANPC}} \approx \left(\frac{1}{2} \right)^2 = 0.25 = 25\% \quad (28)$$

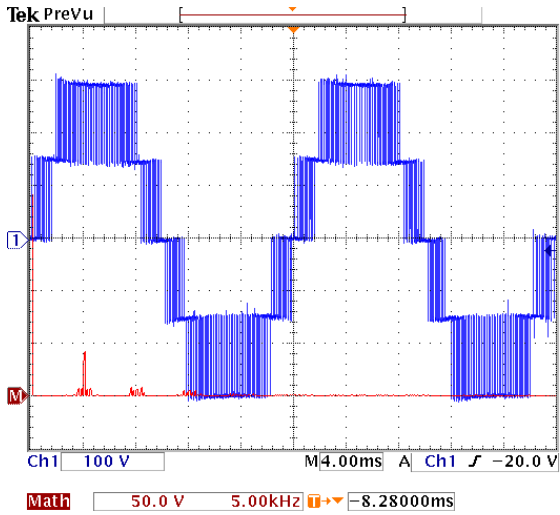
- [1] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," *IEEE Industry Applications Magazine*, vol. 18, no. 4, pp. 26–39, July 2012.
- [2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, Aug 2010.
- [3] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, June 2008.
- [4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.
- [5] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov 2017.



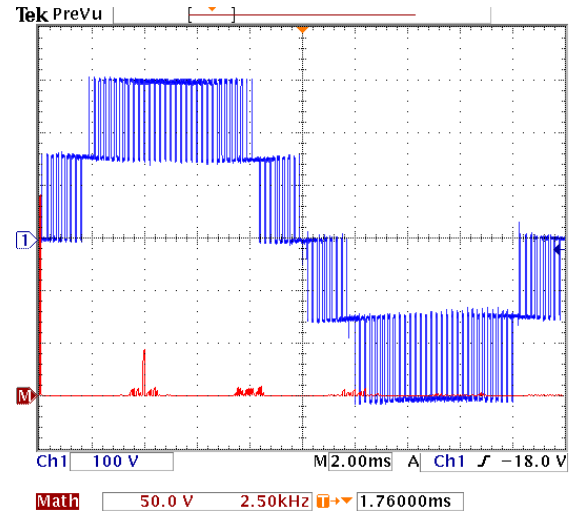
(a) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div



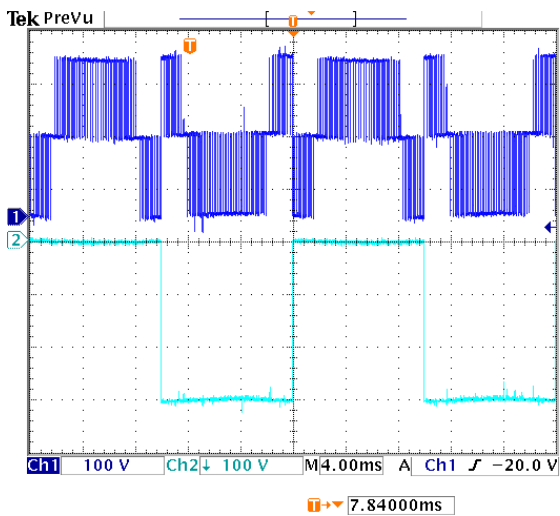
(b) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div



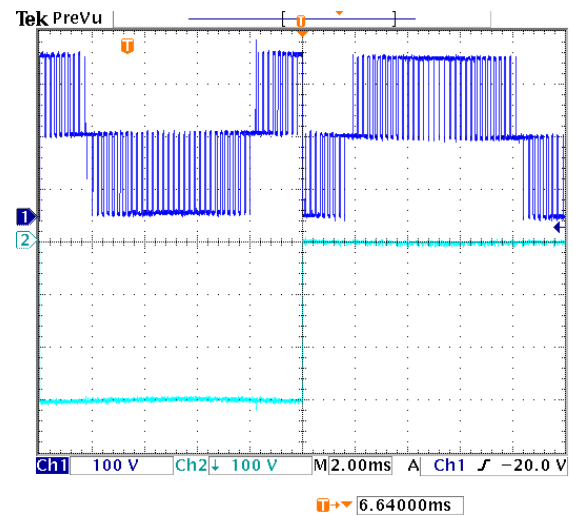
(c) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 5 kHz/Div



(d) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 2.5 kHz/Div

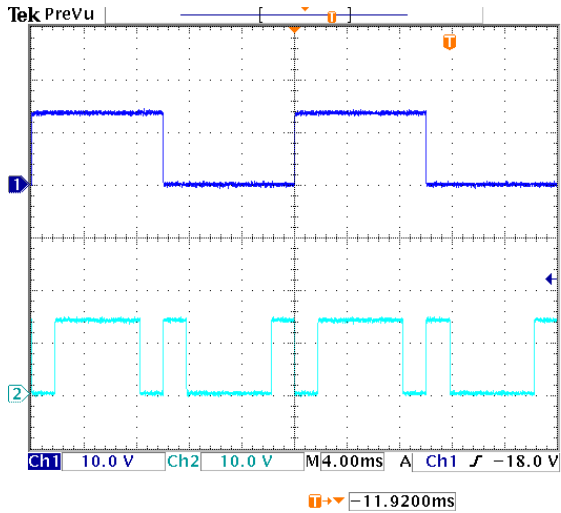


(e) Ch1: $v_{AN}(t)$: 100 V/Div; Ch2: $-v_{ON}(t)$: 100 V/Div

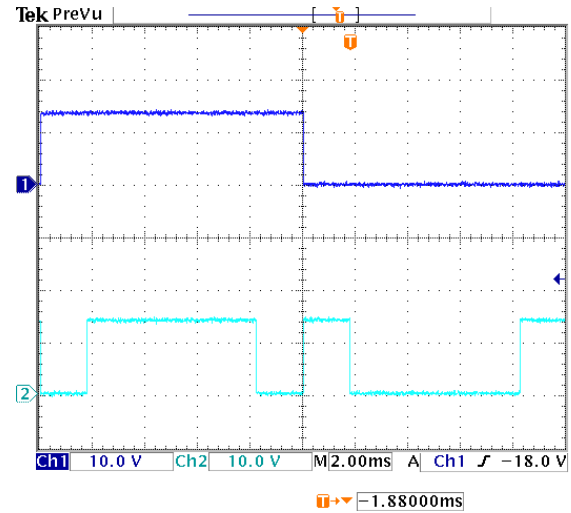


(f) Ch1: $v_{AN}(t)$: 100 V/Div; Ch2: $-v_{ON}(t)$: 100 V/Div

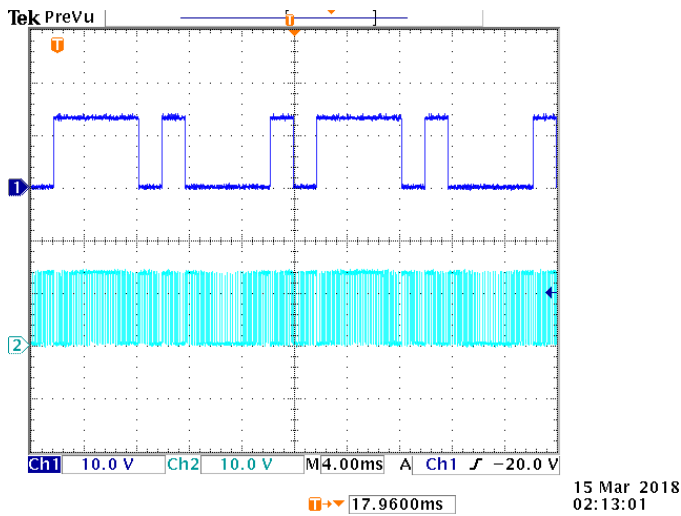
Figure 17: Experimental results for a 5-Level D-ANPC multilevel converter.



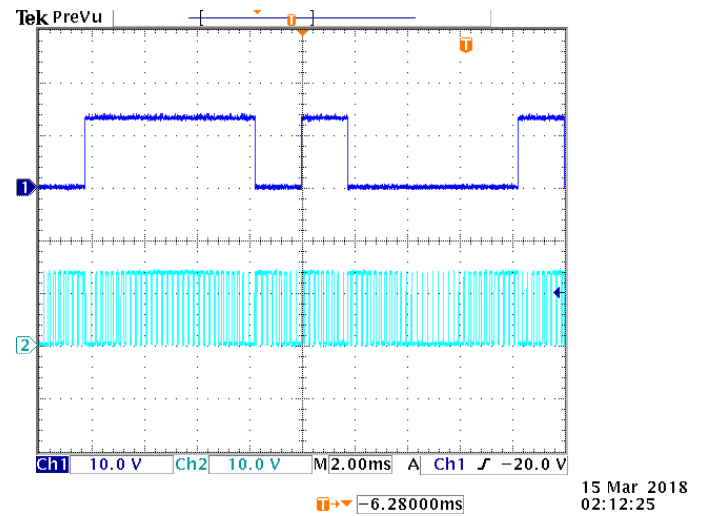
(a) Ch1: $S_T(t)$: 10 V/Div; Ch2: $S_J(t)$: 10 V/Div



(b) Ch1: $S_T(t)$: 10 V/Div; Ch2: $S_J(t)$: 10 V/Div

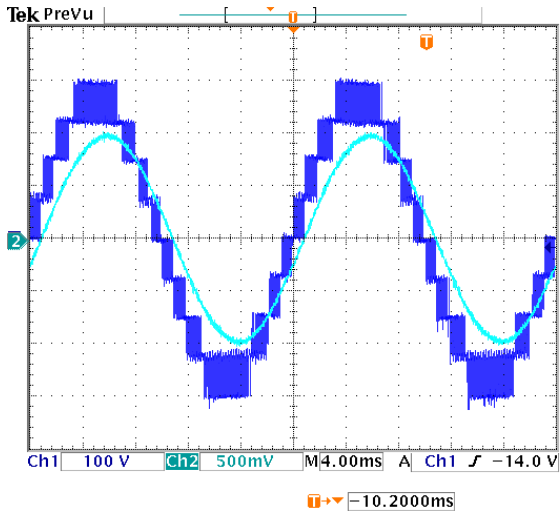


(c) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_1(t)$: 10 V/Div

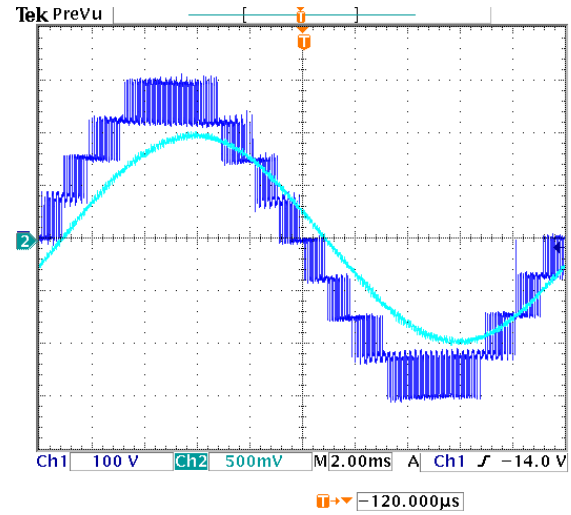


(d) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_1(t)$: 10 V/Div

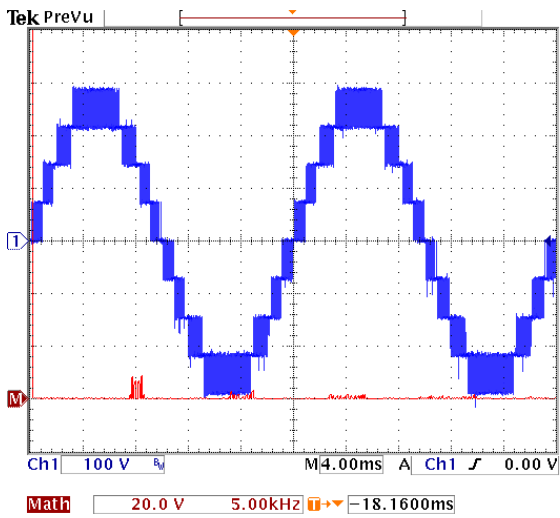
Figure 18: Experimental results for a 5-Level D-ANPC multilevel converter.



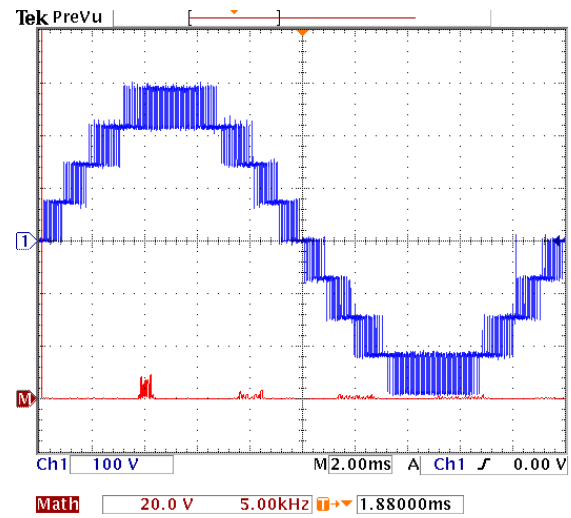
(a) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div



(b) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div

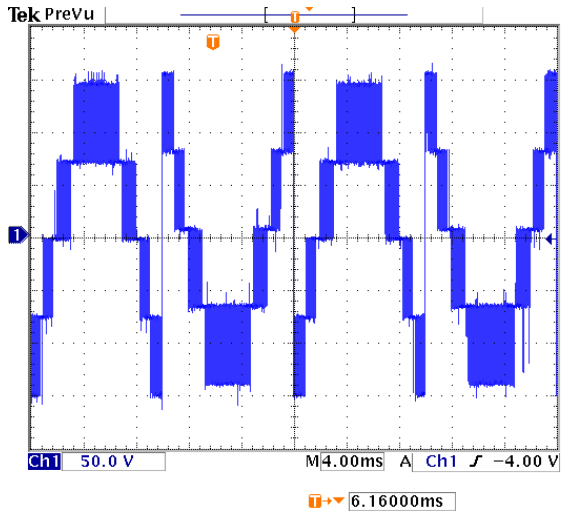


(c) Ch1: v_{out} : 100 V/Div; Math: FFT: 20 V/Div, 5 kHz/Div



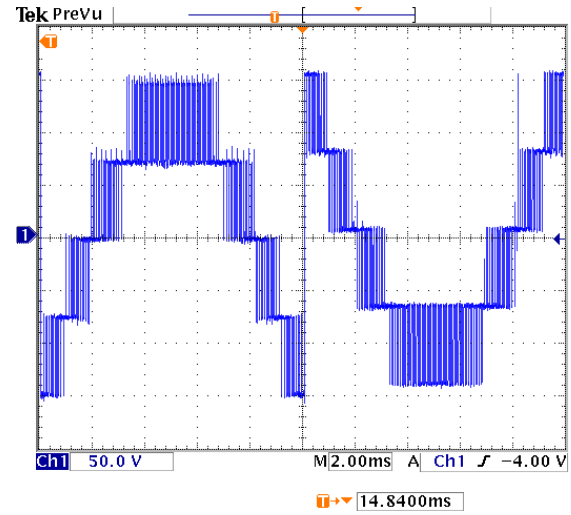
(d) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 5 kHz/Div

Figure 19: Experimental results for a 9-Level D-ANPC multilevel converter.



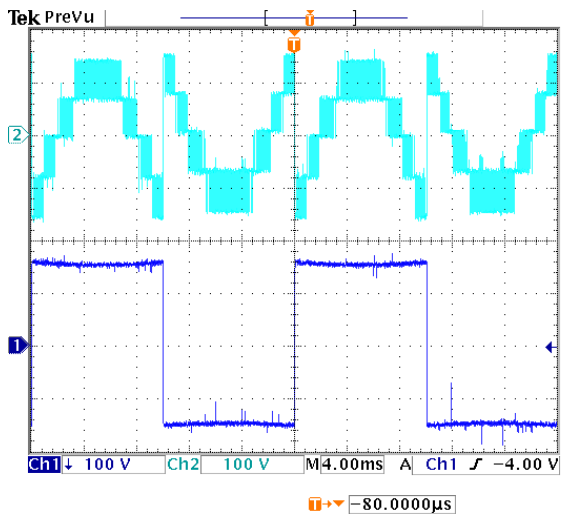
(a) Ch1: $v_{An}(t)$: 50 V/Div

14 Mar 2018
05:11:42



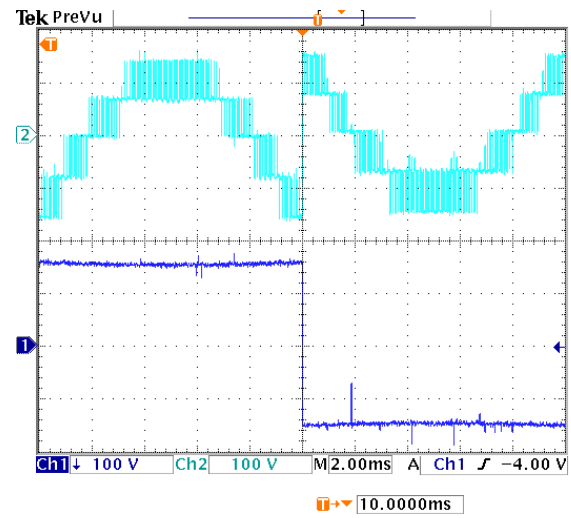
(b) Ch1: $v_{An}(t)$: 50 V/Div

14 Mar 2018
05:13:00



(c) Ch1: $-v_{On}(t)$: 100 V/Div; Ch2: $v_{An}(t)$: 100 V/Div

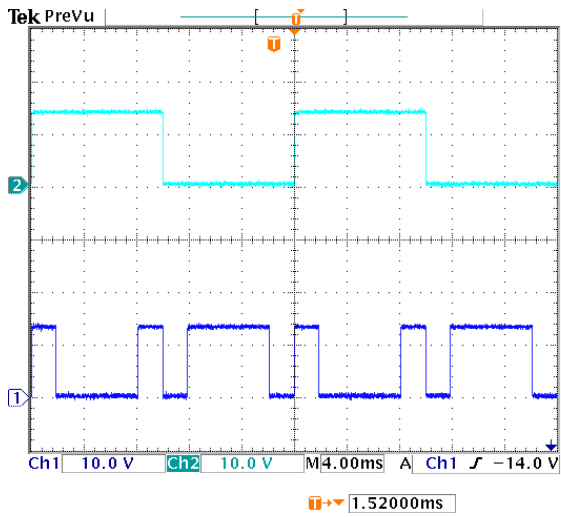
14 Mar 2018
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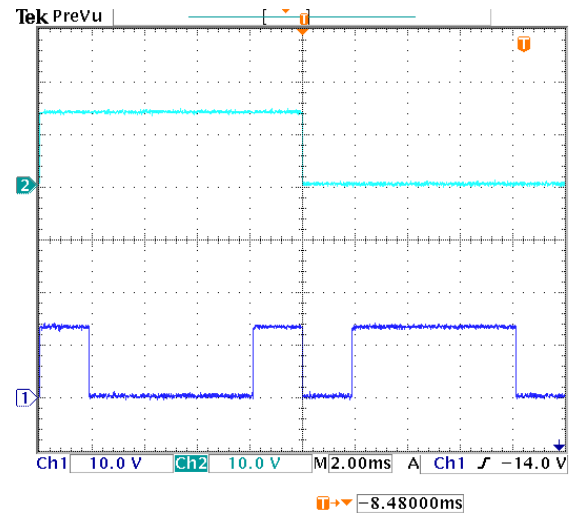
(d) Ch1: $-v_{On}(t)$: 100 V/Div; Ch2: $v_{An}(t)$: 100 V/Div

14 Mar 2018
05:25:13

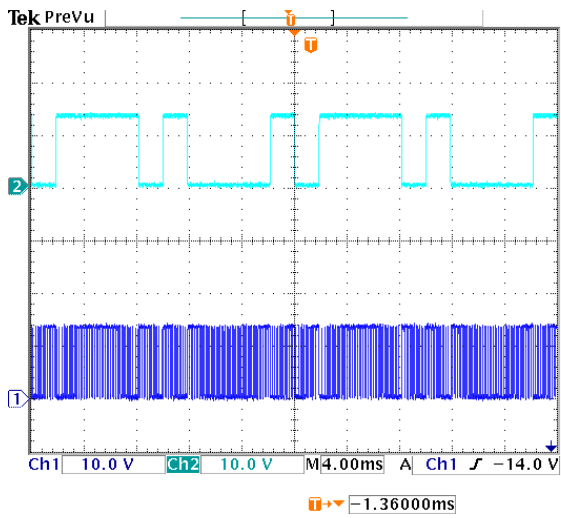
Figure 20: Experimental results for a 9-Level D-ANPC multilevel converter.



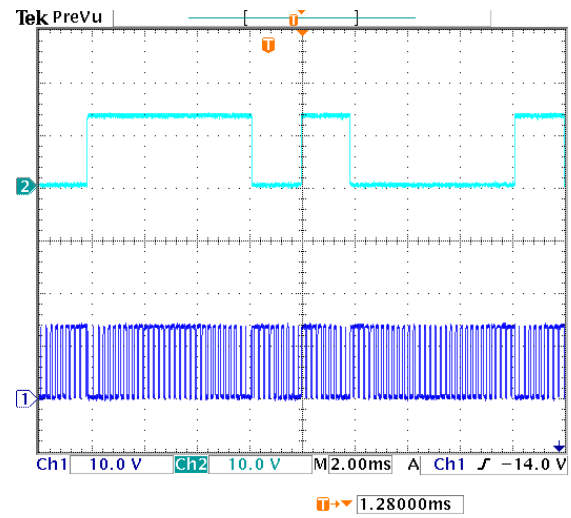
(a) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div



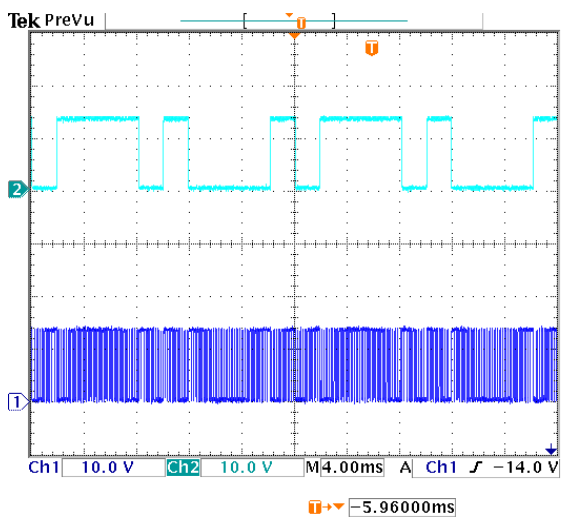
(b) Ch1: $S_J(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div



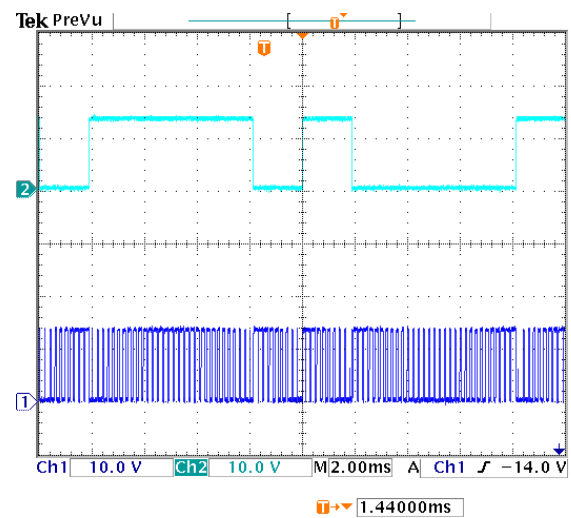
(c) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_J(t)$: 10 V/Div



(d) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_J(t)$: 10 V/Div



(e) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_J(t)$: 10 V/Div



(f) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_J(t)$: 10 V/Div

Figure 21: Experimental results for a 9-Level D-ANPC multilevel converter.

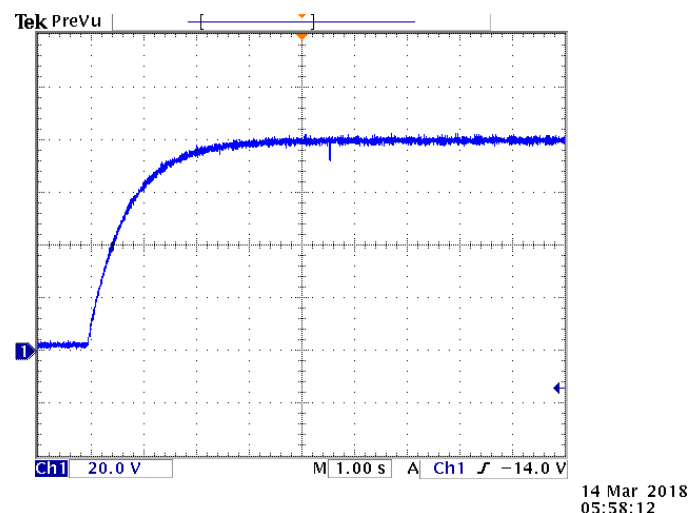
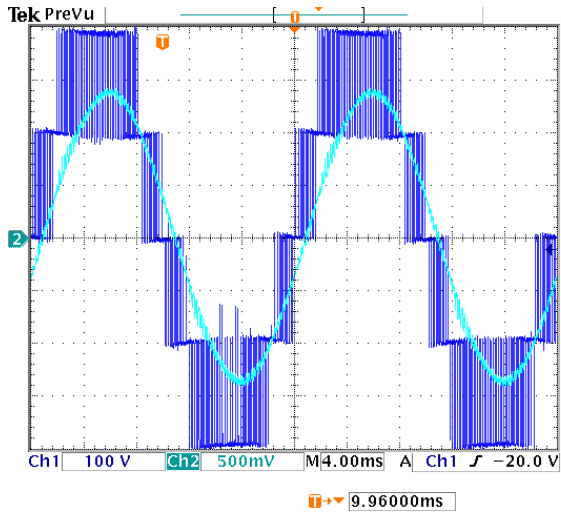
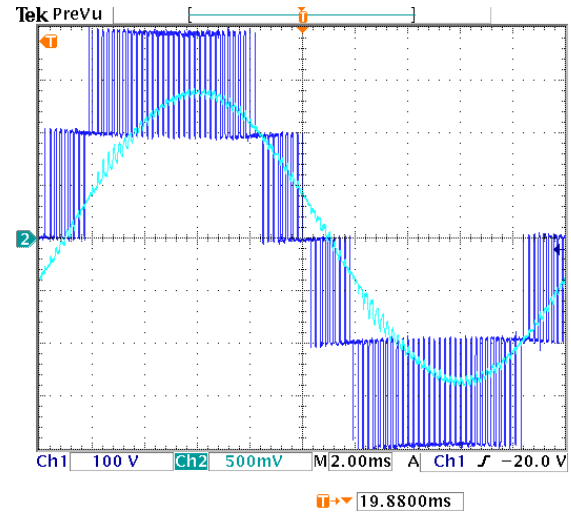


Figure 22: Transient and steady states dynamics in a 9-Level D-ANPC multilevel converter;
Ch1: $v_{FC}(t)$: 20 V/Div.

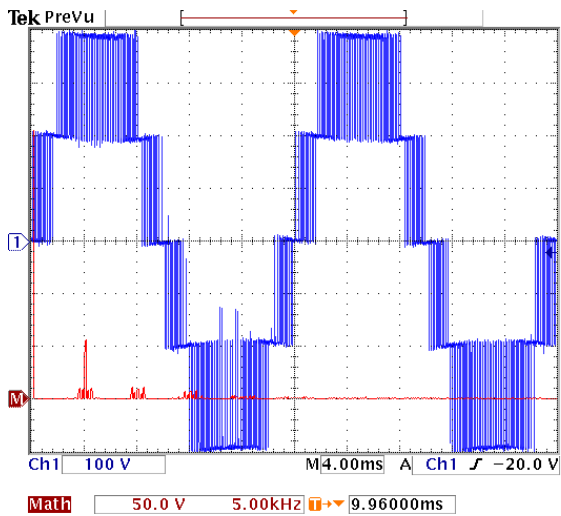
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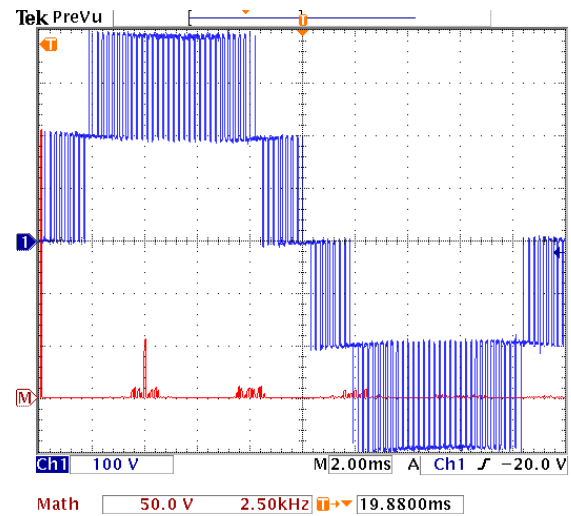
(a) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div



(b) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div

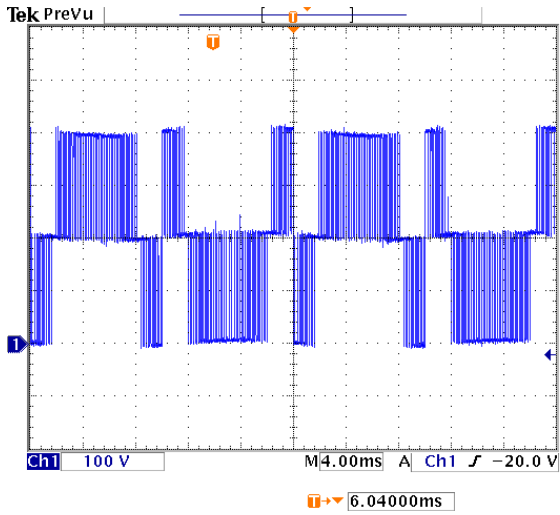


(c) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 5 kHz/Div



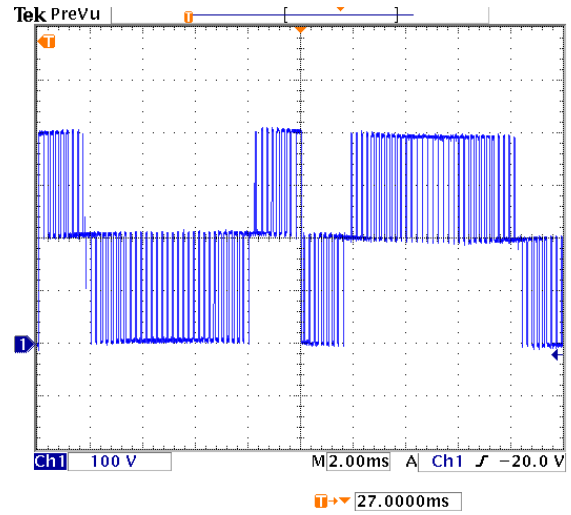
(d) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 2.5 kHz/Div

Figure 23: Experimental results for a 5-Level D-NPC multilevel converter.



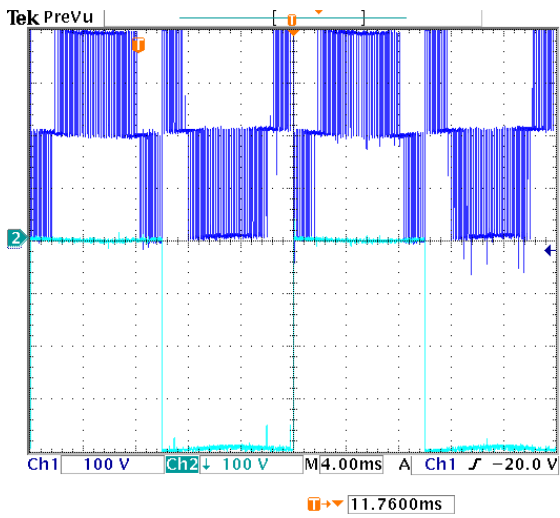
(a) Ch1: $v_{AN}(t)$: 100 V/Div

15 Mar 2018
03:51:07



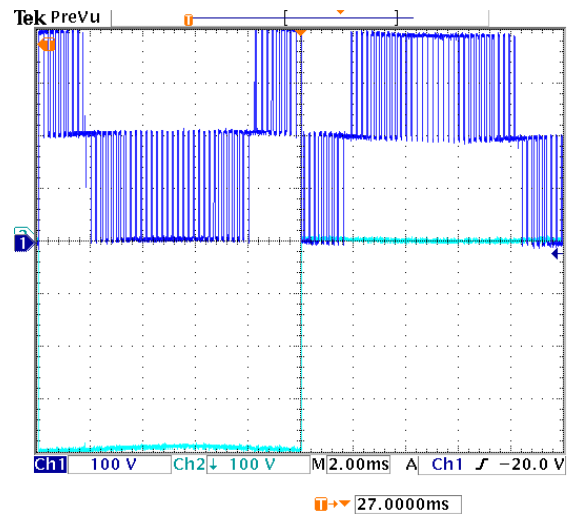
(b) Ch1: $v_{AN}(t)$: 100 V/Div

15 Mar 2018
03:50:38



(c) Ch1: $v_{AN}(t)$: 100 V/Div; Ch2: $-v_{ON}(t)$: 100 V/Div

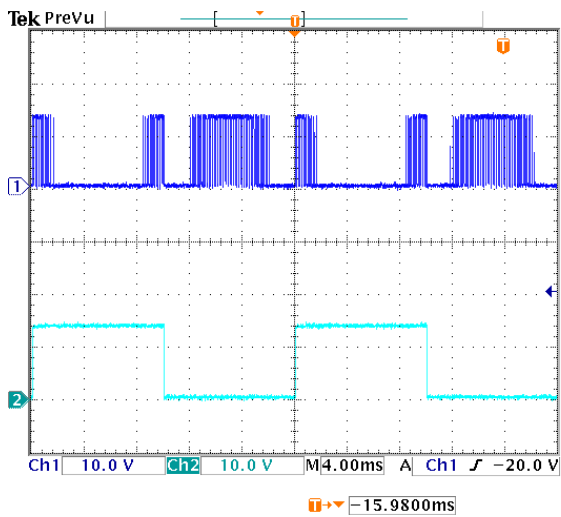
15 Mar 2018
03:52:45



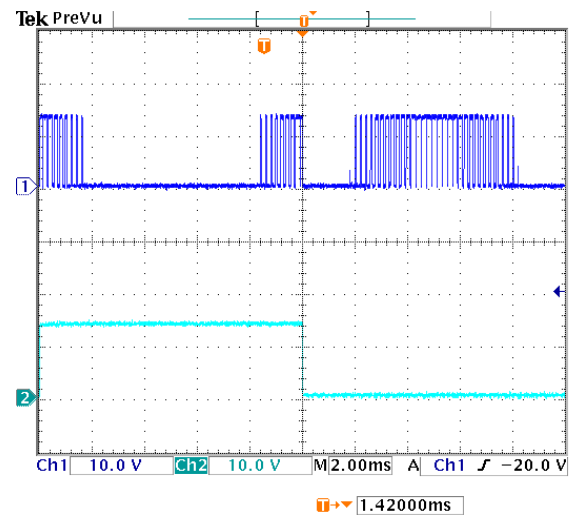
(d) Ch1: $v_{AN}(t)$: 100 V/Div; Ch2: $-v_{ON}(t)$: 100 V/Div

15 Mar 2018
03:50:09

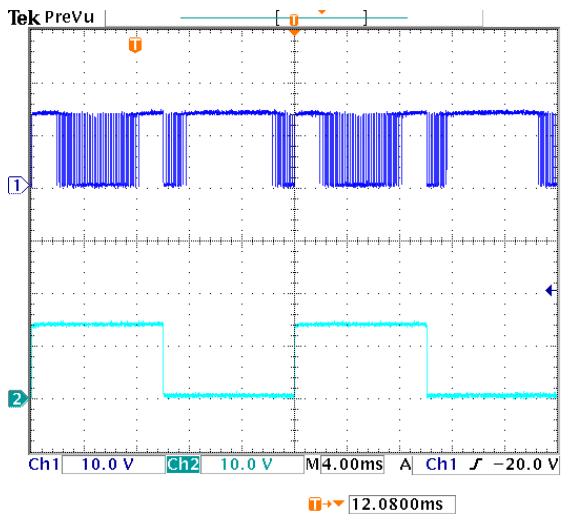
Figure 24: Experimental results for a 5-Level D-NPC multilevel converter.



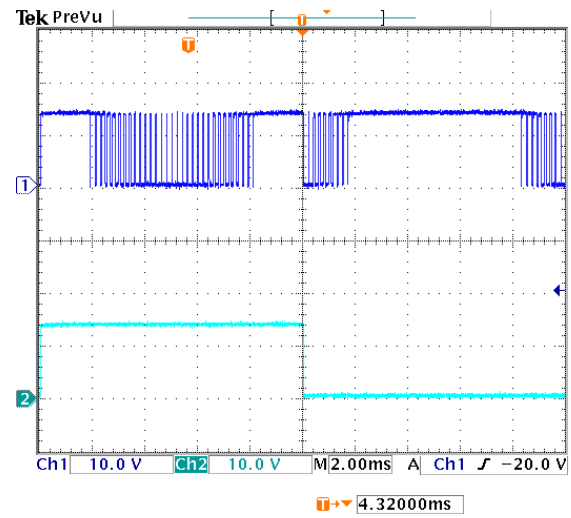
(a) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div



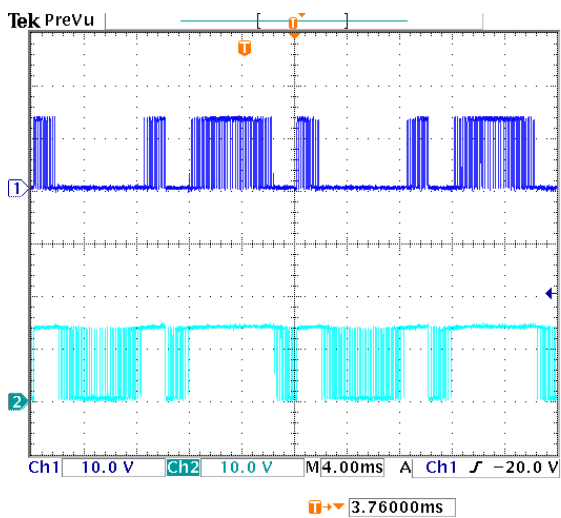
(b) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div



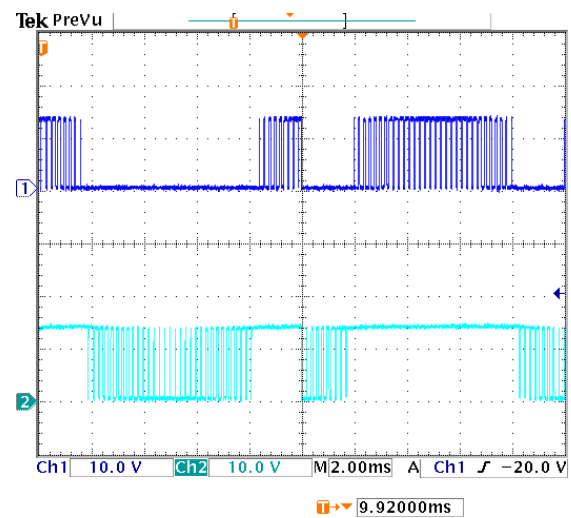
(c) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div



(d) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div

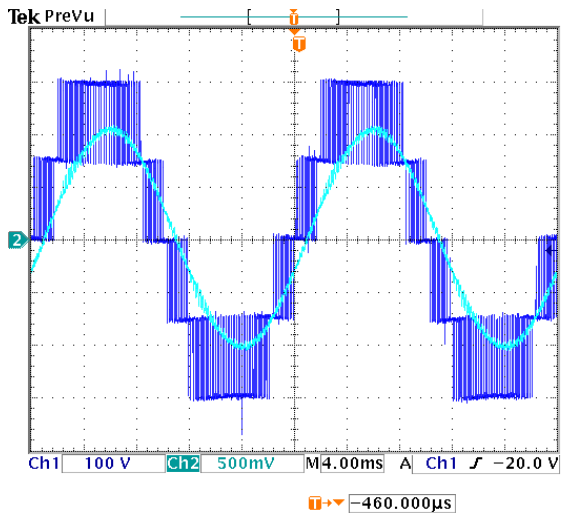


(e) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div

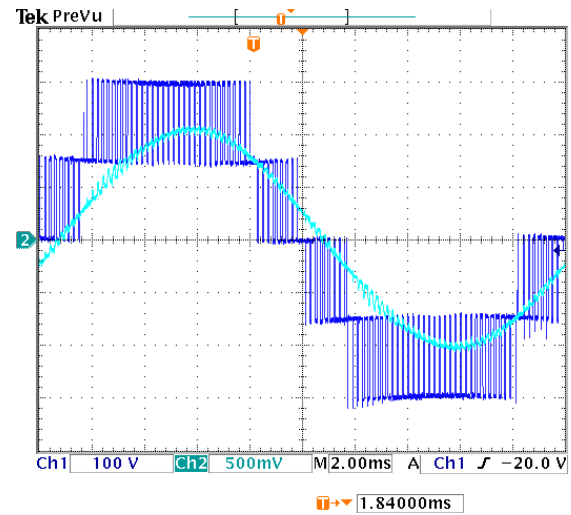


(f) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div

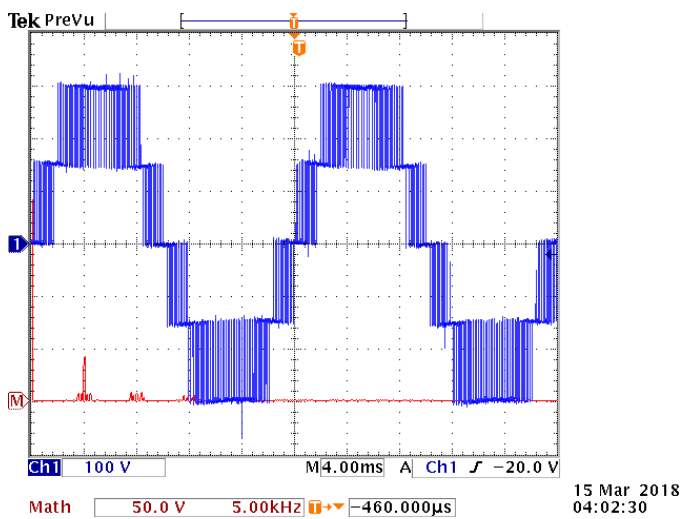
Figure 25: Experimental results for a 5-Level D-NPC multilevel converter.



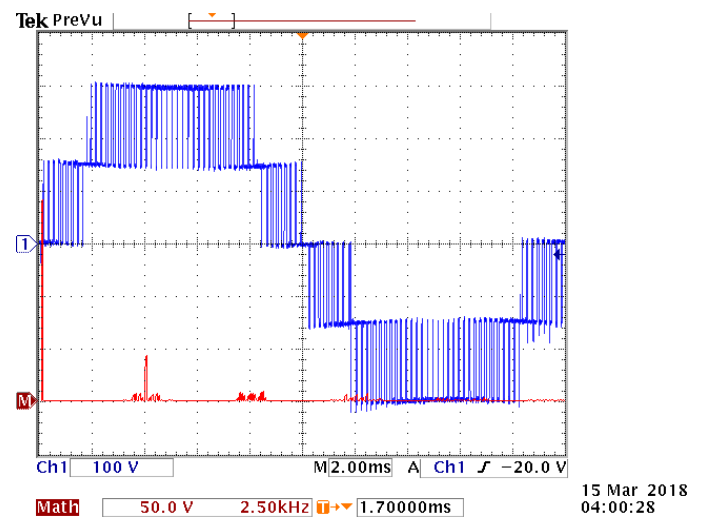
(a) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div



(b) Ch1: v_{out} : 100 V/Div; Ch2: i_{out} : 5 A/Div

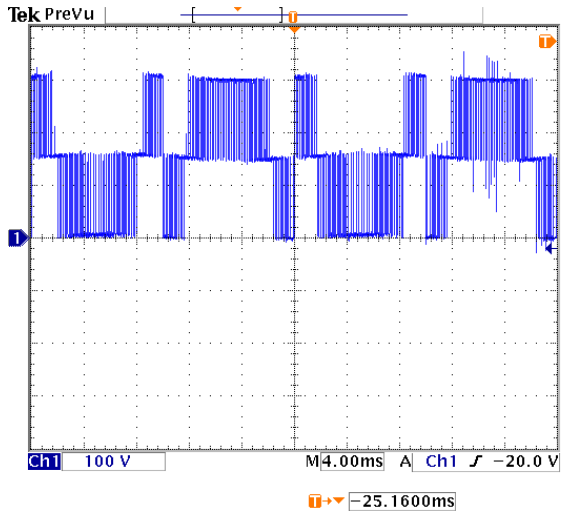


(c) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 5 kHz/Div



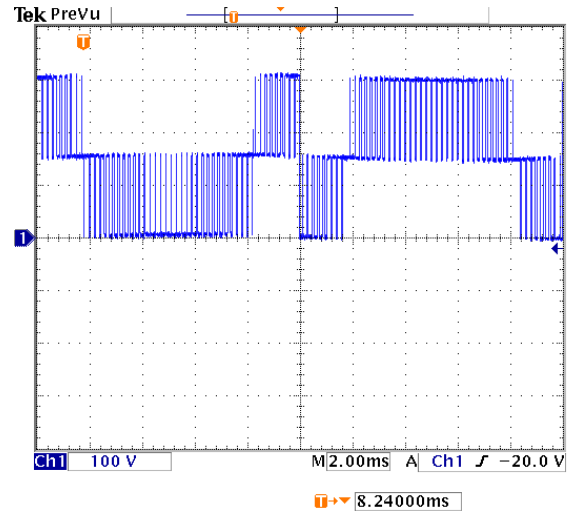
(d) Ch1: v_{out} : 100 V/Div; Math: FFT: 50 V/Div, 2.5 kHz/Div

Figure 26: Experimental results for a 5-Level D-NPP multilevel converter.



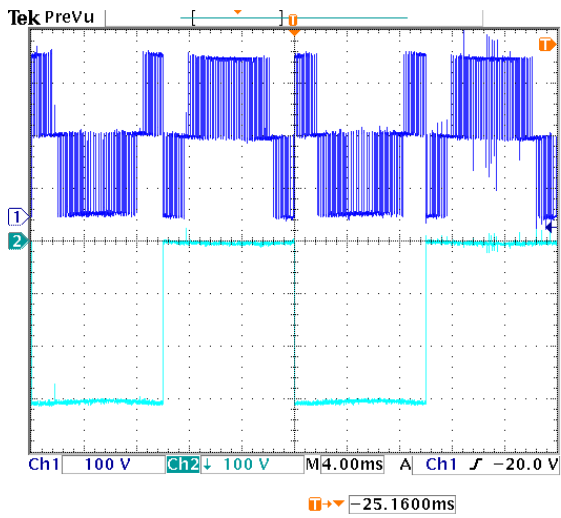
(a) Ch1: $v_{AN}(t)$: 100 V/Div

15 Mar 2018
03:57:33



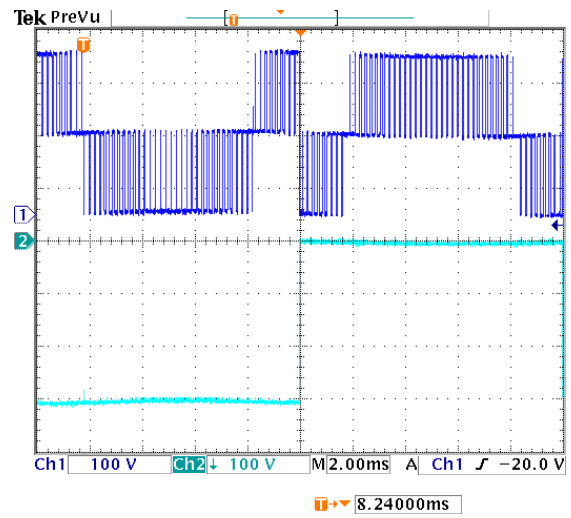
(b) Ch1: $v_{AN}(t)$: 100 V/Div

15 Mar 2018
03:55:26



(c) Ch1: $v_{AN}(t)$: 100 V/Div; Ch2: $-v_{ON}(t)$: 100 V/Div

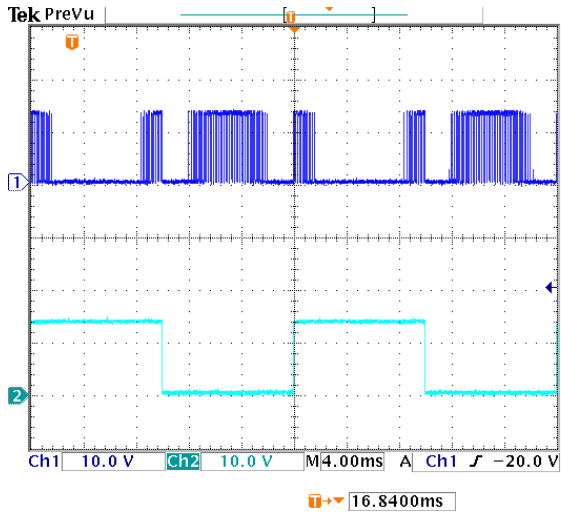
15 Mar 2018
03:56:20



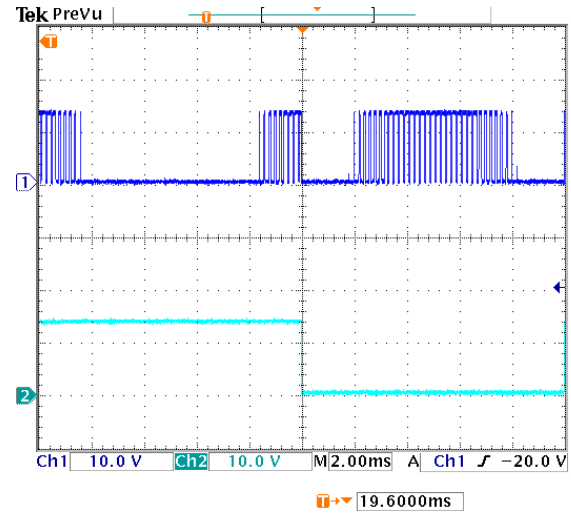
(d) Ch1: $v_{AN}(t)$: 100 V/Div; Ch2: $-v_{ON}(t)$: 100 V/Div

15 Mar 2018
03:55:02

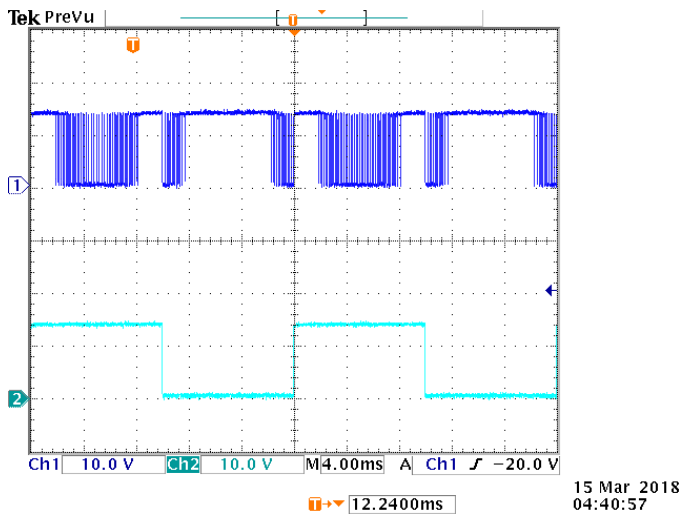
Figure 27: Experimental results for a 5-Level D-NPP multilevel converter.



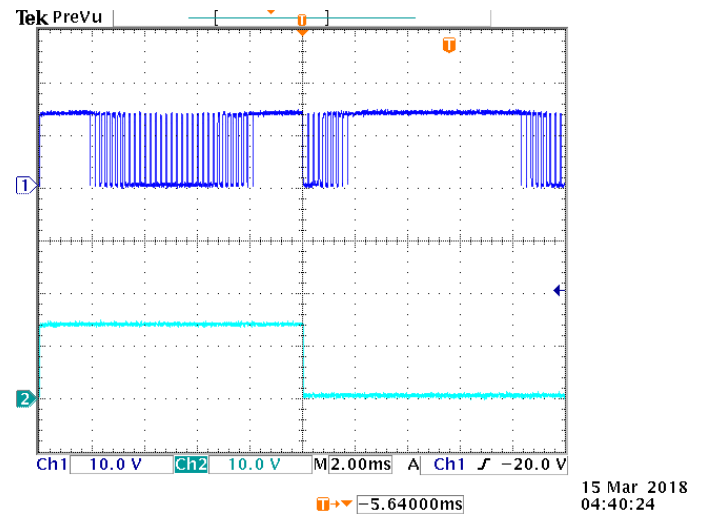
(a) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div



(b) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div

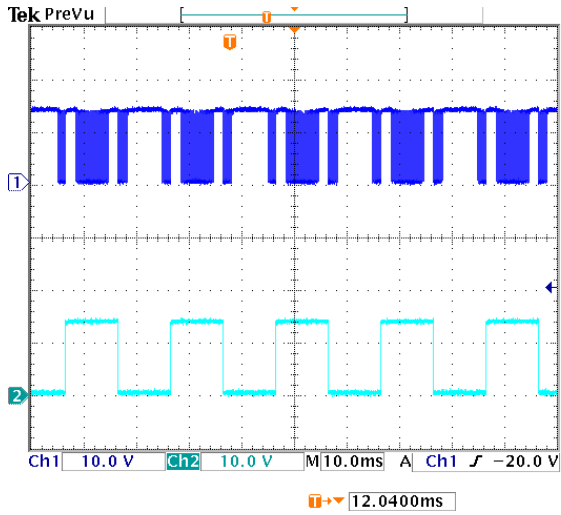


(c) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div

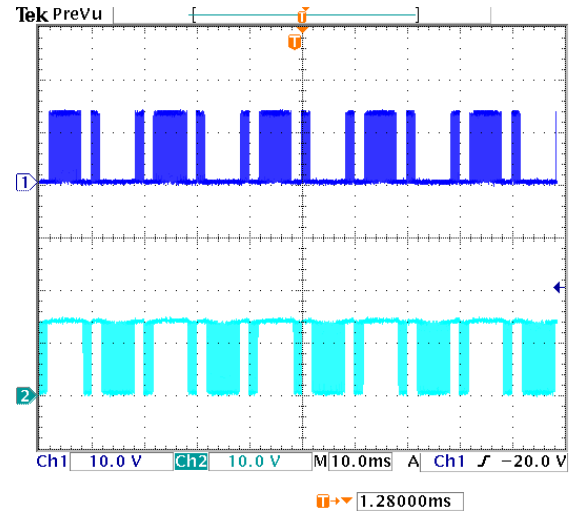


(d) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_T(t)$: 10 V/Div

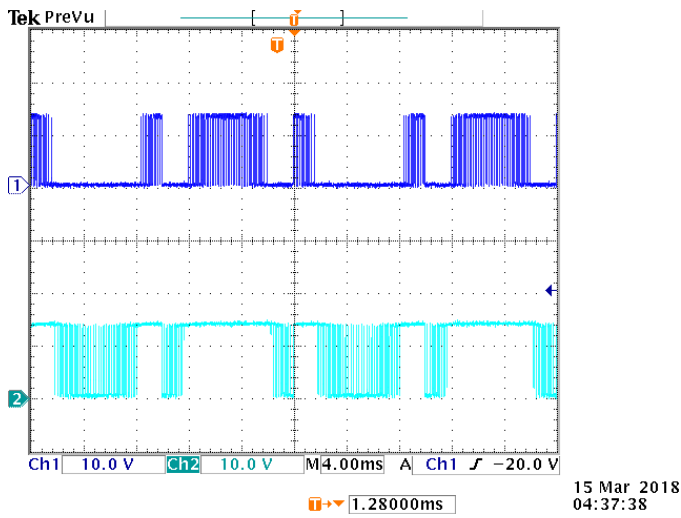
Figure 28: Experimental results for a 5-Level D-NPP multilevel converter.



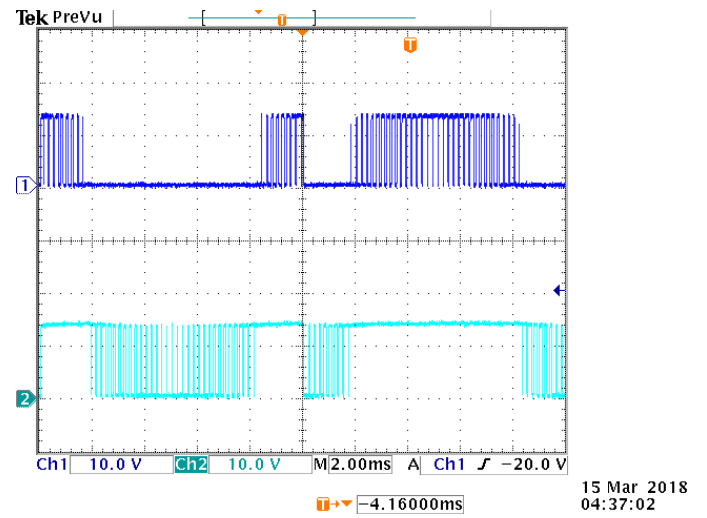
(a) Ch1: $S_2(t)$: 10 V/Div; Ch2: $S_7(t)$: 10 V/Div



(b) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div



(c) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div



(d) Ch1: $S_1(t)$: 10 V/Div; Ch2: $S_2(t)$: 10 V/Div

Figure 29: Experimental results for a 5-Level D-NPP multilevel converter.

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