Design and Implementation of the Ternary Sequences with Good Merit Factor Values

Naga Jyothi Aggala
Research Scholar, Dept. of Electronics and Communication Engineering, Andhra University, Visakhapatnam, India 500 003

Raja Rajeswari K
Professor, Dept. of Electronics and Communication Engineering, Andhra University, Visakhapatnam, India 500 003

Abstract
The pulse compression codes with low autocorrelation sidelobe levels and high Merit Factor (MF) are useful in radar, channel estimation and spread spectrum communication applications. One of the main criteria of good pulse compression is MF. A sequence with high MF can be considered as best sequence.

In this paper an efficient VLSI architecture is proposed for generation and implementation of the ternary sequences using Finite State Machines [FSM]. This VLSI architecture is implemented on the FPGA as it provides the flexibility of reconfigurability and reprogramability

The ternary pulse compression sequence elements are +1,0,-1.Ternary sequences have superior MF compared to binary sequences but cannot be transmitted with existing technology. For transmission of ternary sequences, they must be coded into binary sequences. The binary sequence is chosen such that each of these bi-alphabetic interpretations leads to high MF. At the received section again the received sequence has to be decoded from binary to ternary. The VLSI architecture for implementing ternary codes has been authored in VHDL and the synthesis was done with Xilinx XST, ISE Foundation 12.1i has been used for performing mapping, placing and routing.

Keywords
Ternary sequences, Pulse Compression, Merit Factor (MF), Finite State Machines (FSM), Auto Correlation Function(ACF), Algorithmic State Machines(ASM).

1. INTRODUCTION
Pulse compression allows radar to achieve the average transmitted power of a relatively long pulse, while obtaining the range resolution of short pulse. In radar where there are limitations on the peak power, pulse compression is the only means to obtain the resolution and accuracy associated with a sharp pulse but at the same time acquiring the detection capability of a long pulse. The researchers developed many pulse compression radar signals assisted by modern signal processing systems. Consequently, signals in different shapes have been presented like phase coded signals such as Barker codes , nested Barker codes and frequency coded signals such as simple pulse, Linear Frequency Modulation (LFM), Hyperbolic Frequency Modulation (HFM) and Costas waveform. Each of these signals has its own advantages and disadvantages . In radar scenario, no waveform is optimum for target resolution in general. The interest of many applications such as radars, communications and system identification are in generating the sequences with good autocorrelation properties. The goodness measure varies depending on applications. Levanon.N,2004 [1] has suggested many polyphase codes and all of them are significantly used in radar and sonar signal processing. Obtaining Long sequences with peaky autocorrelation, Barker in 1953 [2] has given an important criteria in the field of radar , sonar and system identification. Griep, Karl R., James A. Ritcey, and John J. Burlingame ,1992[4] as viewed this as an optimization problem for signal design for radar applications and suggested sequences like binary , polyphase, ternary and quaternary sequences. There has been extensive work on binary sequences for obtaining good MF.

A large class of ternary sequences was constructed by Ipatov [5-6] using shift registers. Moharir [7] has given necessary condition for existence of perfect ternary sequences. Shedd and Sarwatte[8] has constructed perfect ternary sequences of length 2^n-1, based on earlier work of Kasami Gold and Hellesth [9] using crosscorrelation of binary maximum length sequence. N.Balaji and et.al. , 2009[3] has given VLSI architecture for generation of ternary sequences with good discrimination factor. Tom H OHOLDT and et.al.[10] has constructed ternary sequences with perfect periodic autocorrelation. Krokhin, Andrei, Andrei Bulatov, and Peter Jeavons [11] has described a hybrid gate structure enabling Multiple Valued Logic (MVL) combination functions implemented on a single chip. J.J.Blakley, 1998[12] given an architecture for direct hardware implementation of programmable ternary de Brujin sequence generators. I.A.Pasha and et.al.,2000[13] has proposed the generation of ternary sequences considering Hamming scan and viewed this as an optimization problem. Yuen,SAM Kwok, 2006[14]has proposed technique for generation of ternary preamble sequences of two different lengths.

The problem in random number generation is in from of uncorrelated random source (of unknown probability distribution) dates back to von Neumann's 1951 work[15]. Elias (1972) [16] generalized von Neumann's scheme. Both Elias and Samuelson [16] proposed methods for generating unbiased random bits in the case of correlated sources (of unknown probability distribution), specifically, they considered finite Markov chains. However, their proposed methods are not efficient or have implementation difficulties [18-19]. Blum (1986)[20] devised an algorithm for efficiently generating random bits from degree-2 finite Markov chains in expected linear time and is still far from optimality on information-efficiency[21]. In this paper, the generalize Blum's algorithm to arbitrary degree finite Markov chains are combine it with Elias's method for efficient generation of unbiased bits [21-23].

2. TERNARY SEQUENCES

The ternary sequences are also known as non binary sequences and have the elements of unequal magnitude. Hence they do not have the ideal energy efficiency i.e. their energy efficiency is less than unity. The sequences having elements 0,+1,-1 are known as ternary sequences. The limitations of binary sequences are overcome with the ternary sequences. Ternary sequences do not meet the constant envelop property. This is a major drawback of ternary sequences.

Several efficient algorithms are available for designing ternary sequences. Moharir [24-25] has shown that the ternary Barker sequences with Discrimination factor (D) greater than 13 exits for all lengths. Though the ternary sequences resulted in superior MF when compared to binary sequences, they had two problems. The ternary alphabet has zero as an element, which implies no transmission during this time slots. Secondly, it is considered difficult to have on-off switching at high power in comparison to phase shifting.

A ternary sequence has to code into binary sequences for transmission. The binary sequences transmitted should be so chosen that each of the bi-alphabetic interpretations leads to high MF.The signal design problem for bi-alphabetic sequence is carried out in different stages and these are described below.

The ternary pulse compression sequence elements are 0,+1,-1. A '+1' is transmitted as sinusoidal signal with 0^0 phase shift and a '-1' is transmitted with 180^0 phase shift and during the period of '0' no signal is transmitted.

Proposed coding of ternary sequences into binary sequences is to replace every ternary element with a binary bigram as

+1 ⟶ 0 1 (or) 1 0

-1 ⟶ 1 1

0 ⟶ 0 0

Let S be the ternary sequence of length m, where the elements S_i are chosen from alphabets [+1 0 -1]

$$S = [S_0, S_1, - - - - -, S_{m-2}, S_{m-1}] \qquad (1)$$

Then the autocorrelation of the sequence is given by

$$\rho(k) = \sum_{i=0}^{m-1-k} S_i \; X \; S_{i+k} \qquad (2)$$

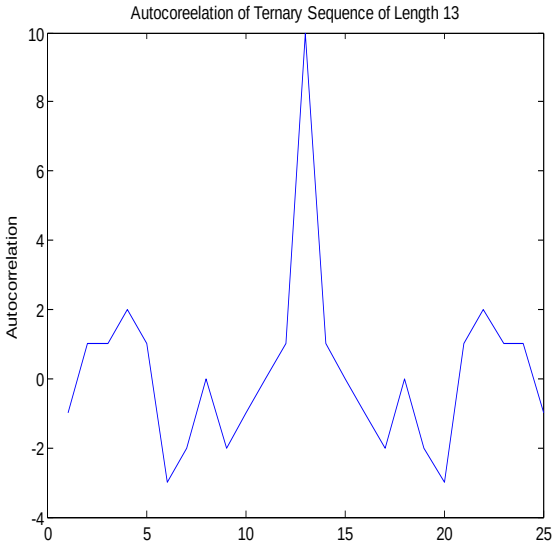

Fig 1 Autocorrelation ternary sequence of Length 13.

The binary sequences to be transmitted are designed from a ternary sequences with high MF. When such a sequence is transmitted it can be subjected to bi-alphabetic interpretation, on reception with the elements at the receiver section again these binary sequences will be decoded into ternary format.

3. FINITE STATE MACHINES

The design is a FSM which generates the individuals that make up as random binary bit strings. These generated bit stings are combined to form as ternary sequence.

FSM is a tool to model the desired behavior of a system and consists of several states. Depending on the state of the machine, outputs are generated based on either the state or the state and inputs to the machine. A FSM consists of several states. Input into the machine is combined with the current state of the machine in order to determine next state of the machine.

3.1 Operation of FSM

The first step is the generation of initial random binary bit strings. The generation can be done by using random number generator. The type of random number generator used is pseudo random generator which is capable of generating long runs.

This generation uses reoccurrence formula and is given in Eq. 3

$$X_{n+1} = (mX_n + i) mod\ M \qquad (3)$$

Where X_0 is seed value, m is the multiplier i is increment and M is modulus.

3.2 Simple FSM

With the combinational and sequential logic , a FSM can store binary information . As an example, 4 state FSM is considered.

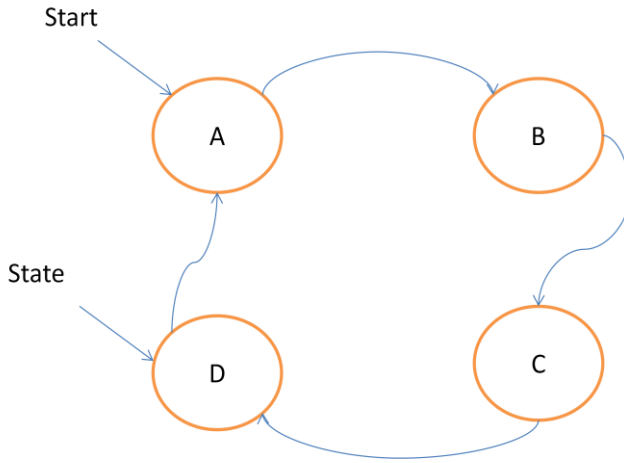

Fig. 2.Four State FSM

Table.1 Binary representation of 4 state FSM

State Name	Binary Representation
A	00
B	01
C	10
D	11

A,B,C and D will automatically transition between each in accordance with a clock signal. There states are represented in binary as two bits therefore 2 flip-flops are used to store the information. The straight arrow indicates the starting point. There can be more than two bits in a state.

3.3 Mealy and Moore Machines

Mealy and Moore machines are used to represent the elevator (up 0r down) in FSM. They support States, Inputs, and Outputs.

Moore Machines: The Output values are determined by its current state the value after the '/' is the output.

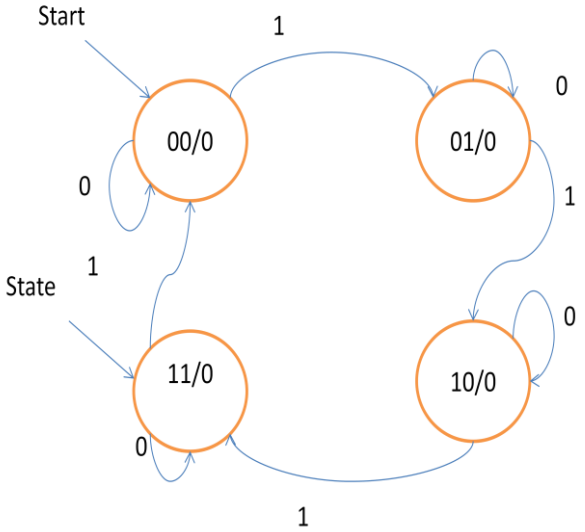

Fig. 3. Moore Machine Representation

Mealy Machine: The output values in this are determined both by its current state and current inputs.

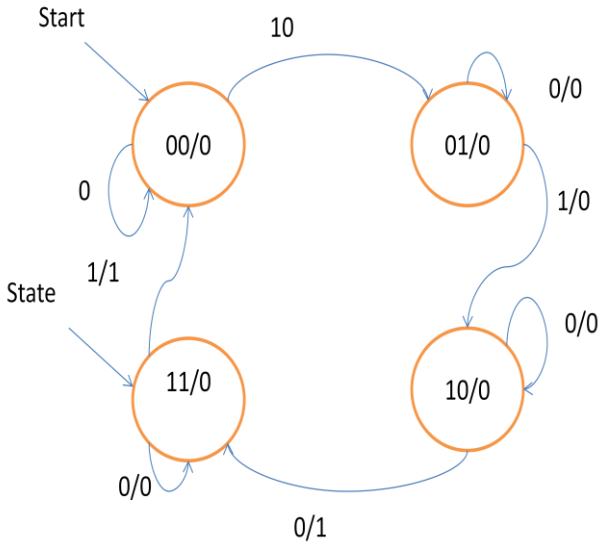

Fig. 4. Moore Machine Representation

3.4 Algorithmic State Machine (ASM)

In FSM states the flow between their states can be easily analyzed as Algorithmic State Machine.

The first step in ASM is to generate random binary bits explained in section 3.1. The ASM at this stage consists of two states (state0, state1). State 0 is a wait state, it will proceed to next state (state1) as soon as the input signal "start" is made high.

It will proceed to next state (state1) on the immediate clock. State 1 outputs the binary bit . The ASM processing are executed in single clock cycle. The random number generator is loaded to a signal named temp-A. The flow between the states depends on seed values, size of binary string therefore the total number of clock cycles required are not fixed [28].

4. NEED FOR PROPOSED ARCHITECTURE

The problem of obtaining long sequences with peaky autocorrelation has been an important problem in the field of radar technology. There has been extensive work in the field of ternary sequences for obtaining good MF values [18-19]. In this paper an efficient real time hardware solution for generation of ternary pulse compression sequences are presented.

MF is one of the main criteria for good pulse compression having minimum sidelobe amplitude and can be considered as the best ternary sequence. The architecture generates ternary sequence of length N. For all the sequences a sidelobe amplitude value are calculated and identifies the sequence with low sidelobe value simulation is carried out. The sequences are generated using FSMs.

Three states are involved in this stage they are external evaluation of the amplitude level, internal evaluation of low amplitude level and storing the sequence respectively. The total operation done is represented in Fig.5.

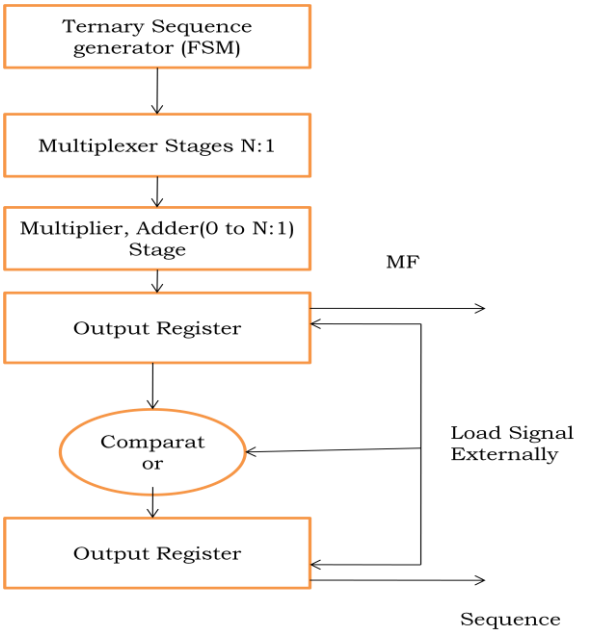

Fig. 5. Methodology for generation of ternary sequences in VLSI

When random bit strings are generated and ready to be evaluated a start signal "start" is made high and the external signal is loaded for comparison. If it found to have minimum amplitude value then the sequence is considered and simulations are performed. The MF is evaluated offline in host PC using Matlab.

5. SIMULATIONS

The architecture shown in Fig. 5 is used for implementing and generation of ternary pulse compression codes. The synthesis of these sequences was done with Xilinx XST, ISE foundation 12.1i . The behavioral simulation of ternary sequence of length 31 is shown in Fig 8.

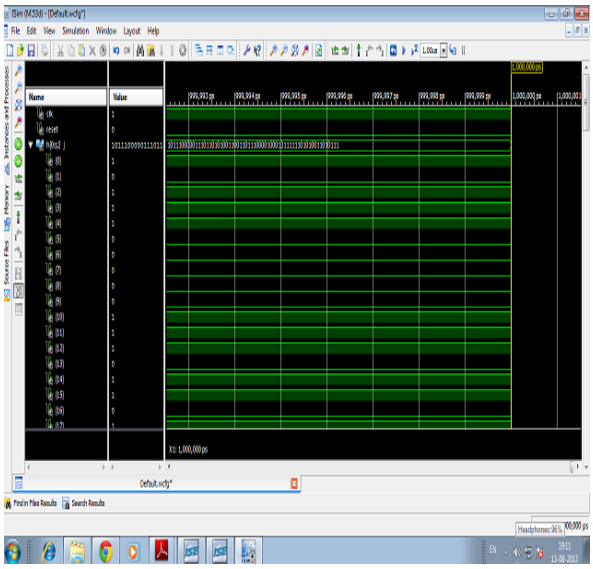

Fig. 8. Behavioral Simulation of ternary sequence of length 31.

RTL Description describes sequence of transfers between the registers. The RTL Description is shown in Fig.9 for ternary sequence of length 31.

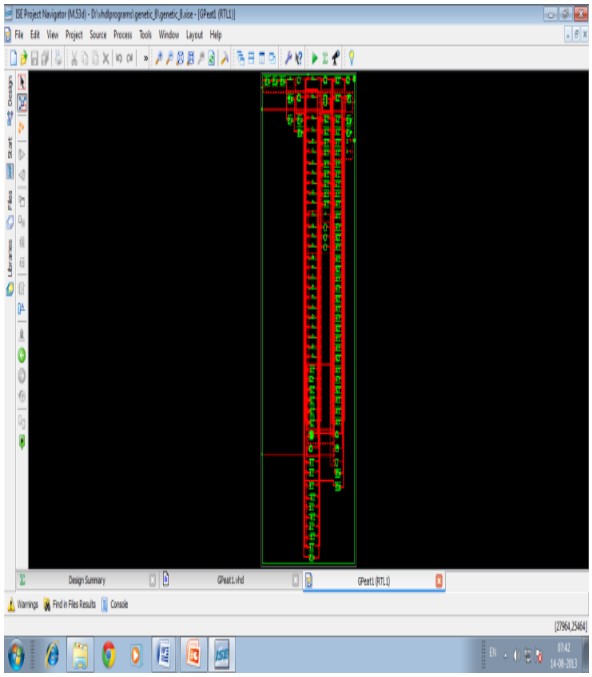

Fig. 9 RTL Schematic for ternary sequence of length 31

The technology schematic provides a flexible interface in the design and is shown in Fig.10.

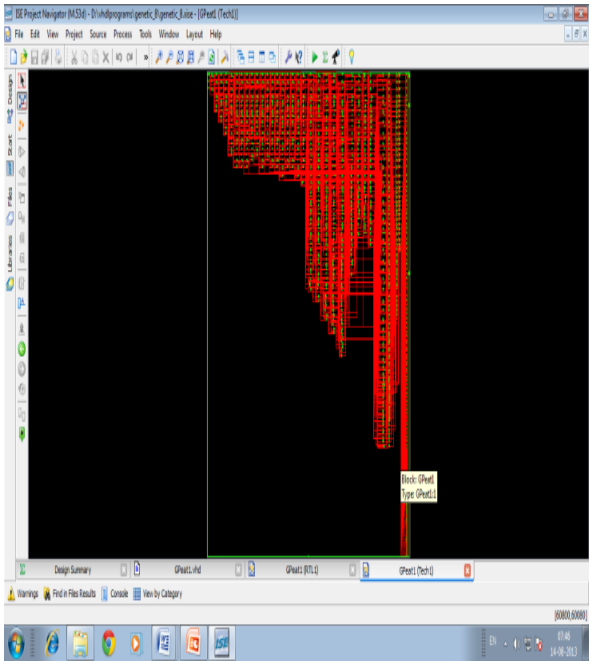

Fig .10 Technology Schematic for ternary sequence of length 31

The total number of devices, multipliers and other logic devices used can be summarized by the design summary are shown in Fig.11.

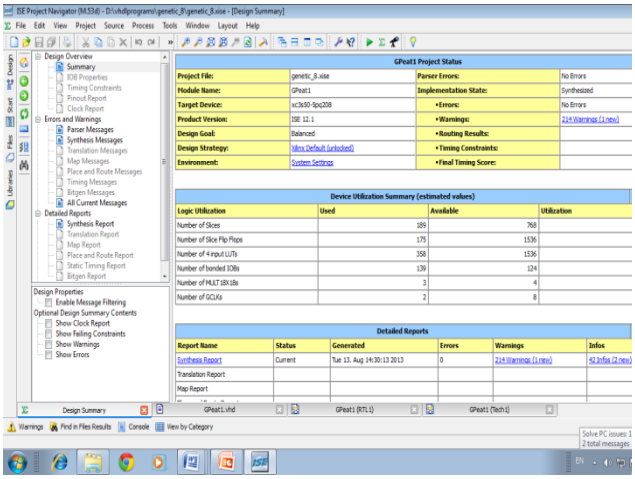

Fig.11 Technology Schematic for ternary sequence of length 31

6. RESULTS

An efficient VLSI architecture was proposed and implemented for the design of ternary sequences used in radar and communication systems for significantly improving the system performance. The synthesized ternary sequences have good MF. The synthesized ternary sequences are promising for practical application to radars and communications. It was also observed that the proposed architecture is giving good MF values for higher lengths. This shows Superiority of the architecture. The MF obtained for synthesized ternary sequences are shown in Table 2.

Table .2 Merit factor of synthesized ternary sequences

S.No	Length of the Sequence (ternary)	Merit Factor(MF)
1	4	2
2	7	4.08
3	10	8.69
4	11	7.56
5	13	13.68
6	15	10.72
7	16	9.5
8	19	9.2
9	20	9.01
10	23	10.01
11	25	9.58
12	27	13.5
13	30	15.6
14	31	18.8
15	32	12.5
16	35	14.2

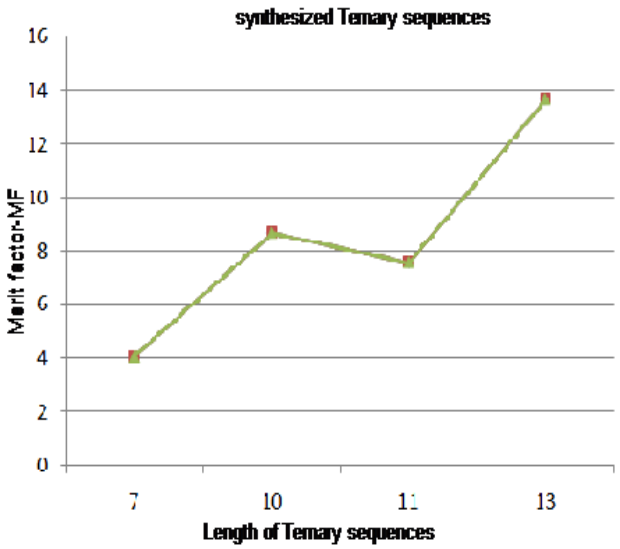

Fig.12 Length of ternary sequence Vs Merit Factor

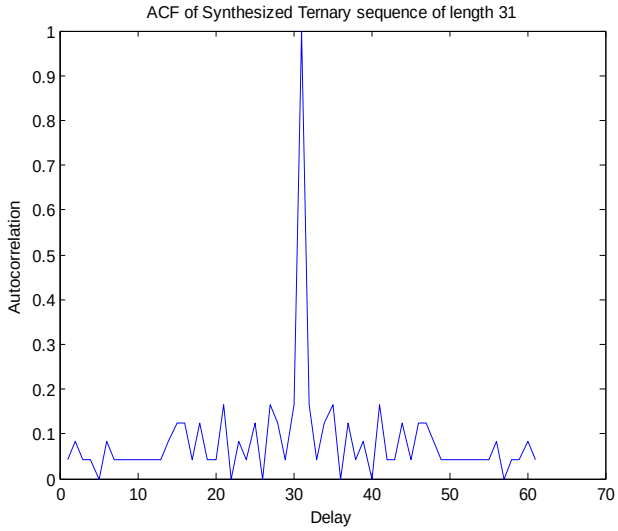

Fig .13 ACF of synthesized ternary sequence of length 31

7. CONCLUSIONS

An efficient VLSI architecture for making exhaustive search for the identification of best pulse compression sequences was proposed and implemented for the design of ternary sequences used in radar and communication systems. The proposed architecture is a unique real-time signal processing solution for ternary pulse compression sequences with as it identifies the sequences with good MF. Ternary sequences have superior MF than binary sequences. Finite State Machines were used for efficient generation of random binary bit strings which overcomes the disadvantages of unbiased random bit generation.

The VLSI architecture for implementing ternary codes has been authored in VHDL and the synthesis was done with Xilinx XST, ISE Foundation 12.1i has been used for performing mapping, placing and routing. From the device utilization summary same architecture is useful for implementation of higher lengths of ternary sequences.

8. ACKNOWLEDGEMENT

This work is being supported by Ministry of Science & Technology, Department of Science & Technology (DST), New Delhi, India, under Women Scientist Scheme (WOS-A) with the Grant No: 100/ (IFD)/8450/2010-11, Dated 15/11/2010.

9. REFERENCES

[1] Levanon. N, Eli Mozeson, "*Radar Signals*", Wiley, New York, 2004

[2] R. H. Barker, "Group synchronizing of binary digital systems, in Communication theory", Butterworth, London, 1953, pp. 273-287.

[3] Balaji, N., K. Subba Rao, and M. Srinivasa Rao. "FPGA implementation of ternary pulse compression sequences with superior merit factors." *NAUN international Journal of Circuits, systems and signal processing* 2.3 (2009): 47-54.

[4] Griep, Karl R., James A. Ritcey, and John J. Burlingame. "Poly-phase codes and optimal filters for multiple user ranging." *Aerospace and Electronic Systems, IEEE Transactions on* 31.2 (1995): 752-767

[5] Ipatov, V. P. "Ternary sequences with ideal periodic autocorrelation properties."*Radio Engineering and Electronic Physics* 24 (1979): 75-79.

[6] Ipatov, V. P., V. D. Platonov, and I. M. Samilov. "A new class of ternary sequences with ideal periodic autocorrelation properties." *Soviet Math.(Izvestiya Vuz) English Translation* 27 (1983): 57-61.

[7] Moharir, P. "Generalized PN sequences (Corresp.)." *Information Theory, IEEE Transactions on* 23.6 (1977): 782-784

[8] Shedd, D., and D. Sarwate. "Construction of sequences with good correlation properties (Corresp.)." *Information Theory, IEEE Transactions on* 25.1 (1979): 94-97.

[9] Helleseth, Tor. "Some results about the cross-correlation function between two maximal linear sequences." *Discrete Mathematics* 16.3 (1976): 209-232.

[10] Hoholdt, Tom, and Jørn Justesen. "Ternary sequences with perfect periodic autocorrelation (Corresp.)." *Information Theory, IEEE Transactions on* 29.4 (1983): 597-600.

[11] Krokhin, Andrei, Andrei Bulatov, and Peter Jeavons. "Functions of multiple-valued logic and the complexity of constraint satisfaction: A short survey."*Multiple-Valued Logic, 2003. Proceedings. 33rd International Symposium on*. IEEE, 2003

[12] Blakley, J. J. "Architecture for hardware implementation of programmable ternary de Bruijn sequence generators." *Electronics Letters* 34.25 (1998): 2389-2390

[13] Pasha, I. A., P. S. Moharir, and N. Sudarshan Rao. "Bi-alphabetic pulse compression radar signal design." *Sadhana* 25.5 (2000): 481-488.

[14] Lei, Zhongding, Francois Chin, and Yuen-Sam Kwok. "UWB ranging with energy detectors using ternary preamble sequences." *Wireless Communications and Networking Conference, 2006. WCNC 2006. IEEE*. Vol. 2. IEEE, 2006.

[15] J. von Neumann, "Various techniques used in connection with randomdigits", Appl. Math. Ser., Notes by G.E. Forstyle, Nat. Bur. Stand., vol.12, pp. 36-38, 1951

[16] P. Elias, "The efficient construction of an unbiased random sequence",Ann. Math. Statist., vol. 43, pp. 865-870, 1972.

[17] S. Pae and M. C. Loui, "Optimal random number generation from a biased coin", in Proc. Sixteenth Annu. ACM-SIAM Symp. Discrete Algorithms, pp. 1079C1088, 2005.

[18] D. Knuth and A. Yao, "The complexity of nonuniform random numbergeneration", Algorithms and Complexity: New Directions and RecentResults, pp. 357-428, 1976.

[19] Zhao, Hongchao, and Jehoshua Bruck. "Efficiently Generating Random Bits from Finite State Markov Chains." (2010).

[20] M. Blum, "Independent unbiased coin flips from a correlated biased source: a finite state Markov chain", Combinatorica, vol. 6, pp. 97-108,1986

[21] Y. Peres, "Iterating von Neumann's procedure for extracting random bits",Ann. Statist., vol 20, pp. 590-597, 1992

[22] S. Pae and M. C. Loui, "Optimal random number generation from a biased coin", in Proc. Sixteenth Annu. ACM-SIAM Symp. Discrete Algorithms, pp. 1079C1088, 2005.

[23] B.Y. Ryabko and E. Matchikina, "Fast and efficient construction of an unbiased random sequence", IEEE Trans. on Information Theory, vol. 46, pp. 1090-1093, 2000.

[24] Moharir, P.S., "Signal Design" Journal of IETE, Vol.41, Oct. 1976, pp. 381-398

[25] Moharir, P. S., R. Singh, and V. M. Maru. "SKH algorithm for signal design."*Electronics letters* 32.18 (1996): 1648.

[26] Wayne Tomasi "Electronic Communications System Fundamentals through Advanced . 5th edition, Pearson Education, 2008.

[27] Rajski J, Tyszer J, "On the diagnostic properties of linear feedback shift registers", ISSN : 0278-0070, IEEE @ 06 August 2002

[28] Naga Jyothi.A., and K.Raja Rajeswari., "Implementation and Generation of Barker and nested Barker codes" ARCNET-2013, NSTL Visakhapatnam

AUTHORS

A. Naga Jyothi was born in 1982 at Visakhapatnam. She received her B.Tech (ECE) from Nagarjuna University and M. Tech(Radar & Microwave Engineering) from Andhra University College of Engineering(A). She has a teaching experience of 3 years. Presently she is perusing her Ph. D in the area of Signal Processing in Andhra University, Visakhapatnam.

K. Raja Rajeswari obtained her B.E., M.E. and Ph.D. degrees from Andhra University, Visakhapatnam, India in 1976, 1978 and 1992 respectively. She has published over 200 papers in various National, International Journals and conferences. She is author of the textbook *Signals and Systems* published by PHI. She is co-author of the textbook *Electronics Devices and Circuits* published by Pearson. Education. Her research interests include Radar and Sonar Signal Processing, Wireless Communication Technologies She has guided fifteen Ph.D.s and presently she is guiding *twenty* students for Doctoral degree. She served as Chairperson IETE Visakhapatnam Centre for two consecutive terms (2006 t0 2010) . Present she is Governing Council Member of IETE, New Delhi. She is zonal coordinate(for south) and Technical Program Committee Chairperson. She is recipient of prestigious IETE Prof SVC Aiya Memorial National Award for the year 2009, Best Researcher Awardee by Andhra University for the year 2004 and recipient Dr. Sarvepalli Radhakrishnan Best Academician Award of the year 2009 by Andhra University. She is Senior Member in IEEE. She is expert member for various national level academic and research committees and reviewer for various national/international journals.