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Admittance Reshaping Control Methods to Mitigate the Interactions between Inverters and Grid

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Received: 20 May 2019; Accepted: 19 June 2019; Published: 26 June 2019



Abstract: With the increasing impedance coupling between inverters and grid caused by the phase-locked loop (PLL), traditional three-phase inverters suffer from the harmonic distortion or instability problems under weak grid conditions. Therefore, the admittance reshaping control methods are proposed to mitigate the interactions between inverters and grid. Firstly, a dynamics model of traditional inverter output admittance including main circuit and PLL is developed in the direct-quadrature (dq) frame. And the qq channel impedance of the inverter presents as a negative incremental resistance with the PLL effect. Secondly, two admittance reshaping control methods are proposed to improve the system damping. The first reshaping technique uses the feedforward point of common coupling (PCC) voltage to modify the inverter output admittance. The second reshaping technique adopts the active damping controller to reconstruct the PLL equivalent admittance. The proposed control methods not only increase the system phase margin, but also ensure the system dynamic response speed. And the total harmonic distortion of steady-state grid-connected current is reduced to less than 2%. Furthermore, a specific design method of control parameters is depicted. Finally, experimental results are provided to prove the validity of the proposed control methods.

Keywords: distributed generation; weak grid; inverter; impedance coupling; admittance reshaping

1. Introduction

With the increasing prevalence of renewable energy systems, the systems are connected to the utility grid by multiple transformers and long transmission lines because of the distributed locations of renewable energy generations [1,2]. Therefore, the utility grid shows the feature of the weak grid where the grid impedance cannot be ignored [3]. Grid-connected inverters are the important part, which transfer renewable energy to the weak grid [4,5]. Under the weak grid condition, the impedance coupling between inverters and grid may cause harmonic distortion or instability problems [6,7].

There are two impedance-based analysis methods to analyze the interaction stability between inverters and weak grid [8–11]. On the one hand, References [8,9] proposed the sequence impedance model by the harmonic linearization modeling method, which is represented by a diagonal matrix, including the positive sequence and negative sequence components. On the other hand, References [10,11] developed the dq impedance model by transforming three-phase variables into a rotating dq reference frame. The phase-locked loop (PLL) effect can be explained through linearizing the transitions between the system and the control dq frame. By the generalized Nyquist criterion, dq impedances can be utilized to analyze system stability considering the PLL effect. The following conclusions can be obtained from the above references: The negative impact of PLL on system stability is caused by the range of negative incremental resistance. It will increase the impedance coupling between inverters and grid, which reduces the system phase margin or leads to system instability.

The impedance reshaping techniques were used to mitigate the interactions between inverters and grid. References [12,13] presented the virtual impedance or active damping methods under the weak grid condition, which changes the structure of inverter output impedance or the output filter parameters. However, only the current control loop of the inverter is considered. Reference [14] proposed a special regulator replacement method with consideration of the PLL, which can effectively improve system stability by adjusting the PLL bandwidth. However, if the PLL bandwidth is small, it may weaken the dynamic performance of the system when the load changes abruptly [15]. Reference [16] used multiple resonance compensators to enhance the amplitude of the inverter output impedance at specific harmonic frequency. However, the process of selecting control parameters is unknown in this control method [17].

Motivated by the above limitations, admittance reshaping control methods are proposed in this paper. The strong points of the proposed methods are given below: On the premise of ensuring the system dynamic response speed, it can increase the system phase margin. Furthermore, a specific design method of control parameters is depicted. This paper is organized as follow: Section 2 presents the admittance model and a stability analysis of the traditional control method; Section 3 proposes two admittance reshaping control methods, designs the control parameters and comparatively analyzes system stability; Section 4 provides experimental results to prove the validity of the proposed control methods; Finally, the conclusions are summarized in Section 5.

2. Admittance Model of Three-Phase Grid-Connected System

2.1. System Description

Figure 1 presents the system structure, which includes the inverter subsystem and the grid subsystem. U_{dc} is the DC-side voltage. u_{inv} , u_{C1} and u_{pcc} are the inverter output voltage, filter capacitor voltage and point of common coupling (PCC) voltage. u_g is the grid voltage. Z_g is the grid impedance. The inductance-capacitance-inductance (LCL) filter is constituted by the inverter-side inductor L_1 , grid-side inductor L_2 and filter capacitor C_1 . R_{L1} and R_{L2} are parasitic resistances of L_1 and L_2 . i_{L1} is the inverter-side inductor current. i_g is the grid-connected current. i_{C1} is the filter capacitor current.

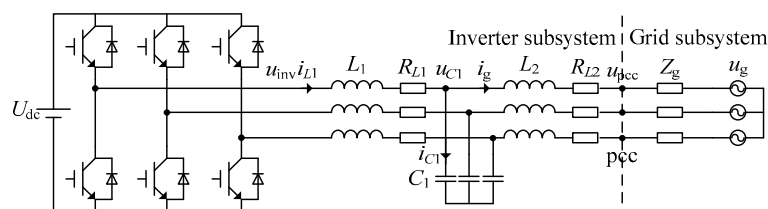


Figure 1. Three-phase grid-connected system.

2.2. Admittance Model of Traditional Control Method

The diagram of the PLL description is shown in Figure 2, where T_{PLL} is the proportional integral (PI) controller of PLL, $T_{PLL} = k_{ppll} + k_{ipll}/s$, k_{ppll} is the proportional coefficient of PLL PI controller, and k_{ipll} is the integral gain of PLL PI controller. Because of the PLL dynamics, there are two dq frames in the system. The first is the system dq frame that is identified by the PCC voltage. The second is the control dq frame that is identified by PLL.

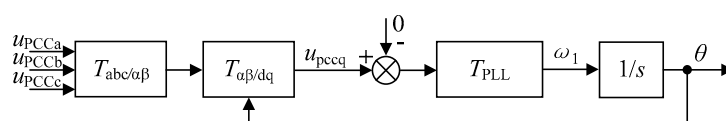


Figure 2. The diagram of PLL description.

The dq admittance model of the traditional control method, considering the PLL effect, is shown in Figure 3. Outside the dotted line of Figure 3, the control diagram of the traditional control method without considering the PLL effect is pretended. The PI controller [18] is often utilized for the grid-connected current loop due to its simplicity and efficiency. The filter capacitor current feedback [19] is often introduced for the active damping loop to suppress the resonance peak of the LCL filter, which does not require additional passive components or energy loss. However, by adding the small-signal disturbance, PLL affects the grid-connected current vector and filter capacitance current vector in the control dq frame and duty cycle vector in the system dq frame. Therefore, the above vectors are converted between the system dq frame and the control dq frame, and considering the PLL effect, are shown inside the dotted line of Figure 3.

In Figure 3, the superscript variable is “sy,” which represents the variable in the system dq frame, the superscript variable is “c,” which represents the variable in the control dq frame, and the front variable is “Δ,” which represents the small-signal variable. The matrices $A_{D-ig}^{sy-c} = \Delta i_{gdq}^{sy} / \Delta D_{dq}^{sy}$, $A_{upcc-ig}^{sy-c} = \Delta i_{gdq}^{sy} / \Delta u_{pccdq}^{sy}$, $A_{upcc-D}^{sy-c} = \Delta D_{dq}^{sy} / \Delta u_{pccdq}^{sy}$, $A_{upcc-ic1}^{sy-c} = \Delta i_{gdq}^{c} / \Delta u_{pccdq}^{sy}$, $A_{upcc-ic1}^{sy-c} = \Delta i_{C1dq}^{c} / \Delta u_{pccdq}^{sy}$, A_{PI} is the PI controller matrix of grid-connected current loop and A_{ad} is the active damping coefficient matrix. The derivation of the above matrices are as follows.

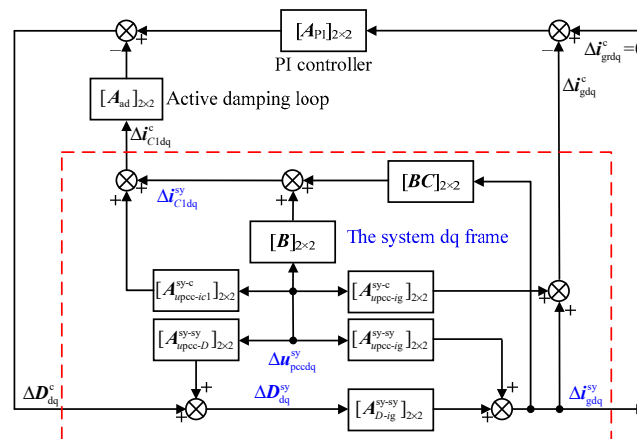


Figure 3. The dq admittance model of traditional control method.

The vectors are converted from the system dq frame to the control dq frame via the translation matrix $T_{\Delta\theta}$, which can be defined as

$$T_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix}. \tag{1}$$

The small-signal pcc voltage can be obtained as

$$\begin{bmatrix} u_{pccd}^c + \Delta u_{pccd}^c \\ u_{pccq}^c + \Delta u_{pccq}^c \end{bmatrix} = \begin{bmatrix} 1 & \Delta\theta \\ -\Delta\theta & 1 \end{bmatrix} \begin{bmatrix} u_{pccd}^{sy} + \Delta u_{pccd}^{sy} \\ u_{pccq}^{sy} + \Delta u_{pccq}^{sy} \end{bmatrix}. \tag{2}$$

And (2) can be rewritten as

$$\begin{bmatrix} \Delta u_{pccd}^c \\ \Delta u_{pccq}^c \end{bmatrix} = \begin{bmatrix} \Delta u_{pccd}^{sy} + u_{pccq}^{sy} \Delta\theta \\ -u_{pccd}^{sy} \Delta\theta + \Delta u_{pccq}^{sy} \end{bmatrix}. \tag{3}$$

From Figure 2, the angle $\Delta\theta$ can be calculated as

$$\Delta\theta = \frac{T_{PLL}(s) \Delta u_{pccq}^c}{s}. \tag{4}$$

Combining (3) and (4), the following equation can be obtained as

$$\Delta\theta = \frac{T_{PLL}(s)\Delta u_{pccq}^{sy}}{s + u_{pccd}^{sy}T_{PLL}(s)} = G_{PLL}\Delta u_{pccq}^{sy} \quad (5)$$

where $G_{PLL} = \frac{T_{PLL}(s)}{s + u_{pccd}^{sy}T_{PLL}(s)}$.

Substitute (5) into (3), (3) can be obtained as

$$\begin{bmatrix} \Delta u_{pccd}^c \\ \Delta u_{pccq}^c \end{bmatrix} = \begin{bmatrix} 0 & u_{pccq}^{sy}G_{PLL} \\ 0 & -u_{pccd}^{sy}G_{PLL} \end{bmatrix} \begin{bmatrix} \Delta u_{pccd}^{sy} \\ \Delta u_{pccq}^{sy} \end{bmatrix} + \begin{bmatrix} \Delta u_{pccd}^{sy} \\ \Delta u_{pccq}^{sy} \end{bmatrix} \quad (6)$$

Similarly, the small-signal duty ratio can be expressed as

$$\begin{bmatrix} \Delta D_d^{sy} \\ \Delta D_q^{sy} \end{bmatrix} = \begin{bmatrix} 0 & -D_q^{sy}G_{PLL} \\ 0 & D_d^{sy}G_{PLL} \end{bmatrix} \begin{bmatrix} \Delta u_{pccd}^{sy} \\ \Delta u_{pccq}^{sy} \end{bmatrix} + \begin{bmatrix} \Delta D_d^c \\ \Delta D_q^c \end{bmatrix} \quad (7)$$

And the matrix A_{upcc-D}^{sy-sy} can be obtained as

$$A_{upcc-D}^{sy-sy} = \frac{\Delta D_{dq}^{sy}}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{3dd} & -A_{3dq} \\ A_{3qd} & A_{3qq} \end{bmatrix} = \begin{bmatrix} 0 & -D_q^{sy}G_{PLL} \\ 0 & D_d^{sy}G_{PLL} \end{bmatrix} \quad (8)$$

Meanwhile, the small-signal grid-connected current can be expressed as

$$\begin{bmatrix} \Delta i_{gd}^c \\ \Delta i_{gq}^c \end{bmatrix} = \begin{bmatrix} 0 & i_{gq}^{sy}G_{PLL} \\ 0 & -i_{gd}^{sy}G_{PLL} \end{bmatrix} \begin{bmatrix} \Delta u_{pccd}^{sy} \\ \Delta u_{pccq}^{sy} \end{bmatrix} + \begin{bmatrix} \Delta i_{gd}^{sy} \\ \Delta i_{gq}^{sy} \end{bmatrix} \quad (9)$$

And the matrix $A_{upcc-ig}^{sy-c}$ can be obtained as

$$A_{upcc-ig}^{sy-c} = \frac{\Delta i_{gdq}^c}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{4dd} & A_{4dq} \\ A_{4qd} & -A_{4qq} \end{bmatrix} = \begin{bmatrix} 0 & i_{gq}^{sy}G_{PLL} \\ 0 & -i_{gd}^{sy}G_{PLL} \end{bmatrix} \quad (10)$$

At the same time, the small-signal filter capacitance current can be expressed as

$$\begin{bmatrix} \Delta i_{C1d}^c \\ \Delta i_{C1q}^c \end{bmatrix} = \begin{bmatrix} 0 & i_{C1q}^{sy}G_{PLL} \\ 0 & -i_{C1d}^{sy}G_{PLL} \end{bmatrix} \begin{bmatrix} \Delta u_{pccd}^{sy} \\ \Delta u_{pccq}^{sy} \end{bmatrix} + \begin{bmatrix} \Delta i_{C1d}^{sy} \\ \Delta i_{C1q}^{sy} \end{bmatrix} \quad (11)$$

And the matrix $A_{upcc-ic1}^{sy-c}$ can be obtained as

$$A_{upcc-ic1}^{sy-c} = \frac{\Delta i_{C1dq}^c}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{5dd} & A_{5dq} \\ A_{5qd} & -A_{5qq} \end{bmatrix} = \begin{bmatrix} 0 & i_{C1q}^{sy}G_{PLL} \\ 0 & -i_{C1d}^{sy}G_{PLL} \end{bmatrix} \quad (12)$$

According to the small-signal open-loop circuit model of LCL filter in the system dq frame, the following equation can be expressed as

$$\begin{cases} \begin{bmatrix} \Delta D_q^{sy} U_{dc}/2 \\ \Delta D_q^{sy} U_{dc}/2 \end{bmatrix} - \begin{bmatrix} \Delta u_{C1d}^{sy} \\ \Delta u_{C1q}^{sy} \end{bmatrix} = \mathbf{A} \begin{bmatrix} \Delta i_{L1d}^{sy} \\ \Delta i_{L1q}^{sy} \end{bmatrix} \\ \begin{bmatrix} \Delta i_{L1d}^{sy} \\ \Delta i_{L1q}^{sy} \end{bmatrix} - \begin{bmatrix} \Delta i_{gd}^{sy} \\ \Delta i_{gq}^{sy} \end{bmatrix} = \mathbf{B} \begin{bmatrix} \Delta u_{C1d}^{sy} \\ \Delta u_{C1q}^{sy} \end{bmatrix} \\ \begin{bmatrix} \Delta u_{C1d}^{sy} \\ \Delta u_{C1q}^{sy} \end{bmatrix} - \begin{bmatrix} \Delta u_{pccd}^{sy} \\ \Delta u_{pccq}^{sy} \end{bmatrix} = \mathbf{C} \begin{bmatrix} \Delta i_{gd}^{sy} \\ \Delta i_{gq}^{sy} \end{bmatrix} \end{cases}, \quad (13)$$

where $\mathbf{A} = \begin{bmatrix} sL_1 + R_{L1} & -\omega_1 L_1 \\ \omega_1 L_1 & sL_1 + R_{L1} \end{bmatrix}$, $\mathbf{B} = \begin{bmatrix} sC_1 & -\omega_1 C_1 \\ \omega_1 C_1 & sC_1 \end{bmatrix}$, $\mathbf{C} = \begin{bmatrix} sL_2 + R_{L2} & -\omega_1 L_2 \\ \omega_1 L_2 & sL_2 + R_{L2} \end{bmatrix}$.
 From (13), (14) can be obtained as

$$\Delta i_{C1dq}^{sy} = \mathbf{B} \Delta u_{pccdq}^{sy} + \mathbf{BC} \Delta i_{gdq}^{sy}. \quad (14)$$

By setting ΔU_{dc} and Δu_{pccdq}^{sy} to zero, the matrix $\mathbf{A}_{D-ig}^{sy-sy}$ can be obtained as

$$\mathbf{A}_{D-ig}^{sy-sy} = \frac{\Delta i_{gdq}^{sy}}{\Delta D_{dq}^{sy}} = \mathbf{E} \cdot (\mathbf{C} + \mathbf{A} + \mathbf{ABC})^{-1}, \quad (15)$$

where $\mathbf{E} = [U_{dc}/2, 0; 0, U_{dc}/2]$.

Similarly, by setting ΔU_{dc} and ΔD_{dq}^{sy} to zero, the matrix $\mathbf{A}_{upcc-ig}^{sy-sy}$ can be obtained as

$$\mathbf{A}_{upcc-ig}^{sy-sy} = \frac{\Delta i_{gdq}^{sy}}{\Delta u_{pccdq}^{sy}} = -(\mathbf{AB} + \mathbf{I}) \cdot (\mathbf{ABC} + \mathbf{A} + \mathbf{C})^{-1}, \quad (16)$$

where \mathbf{I} is the identity matrix.

Meanwhile, the matrix \mathbf{A}_{PI} can be defined as

$$\mathbf{A}_{PI} = \begin{bmatrix} A_{6dd} & A_{6dq} \\ A_{6qd} & A_{6qq} \end{bmatrix} = \begin{bmatrix} G_i & 0 \\ 0 & G_i \end{bmatrix}. \quad (17)$$

And the matrix \mathbf{A}_{ad} can also be defined as

$$\mathbf{A}_{ad} = \begin{bmatrix} A_{7dd} & A_{7dq} \\ A_{7qd} & A_{7qq} \end{bmatrix} = \begin{bmatrix} K_C & 0 \\ 0 & K_C \end{bmatrix}. \quad (18)$$

From Figure 3 and Mason's gain formula, the inverter output admittance \mathbf{Y}_{inv_PLL} with considering the PLL effect using traditional control method can be calculated as

$$\mathbf{Y}_{inv_PLL} = \begin{bmatrix} Y_{dd} & Y_{dq} \\ Y_{qd} & Y_{qq} \end{bmatrix} = \frac{\mathbf{A}_{upcc-ig}^{sy-sy} + \mathbf{A}_{D-ig}^{sy-sy} (\mathbf{A}_{upcc-D}^{sy-sy} - \mathbf{A}_{PI} \mathbf{A}_{upcc-ig}^{sy-c} - \mathbf{A}_{ad} (\mathbf{A}_{upcc-ic1}^{sy-c} + \mathbf{B}))}{\mathbf{I} + \mathbf{A}_{D-ig}^{sy-sy} (\mathbf{A}_{PI} + \mathbf{A}_{ad} (\mathbf{BC}))}. \quad (19)$$

Without considering the PLL effect, $\mathbf{A}_{upcc-D}^{sy-sy} = \mathbf{A}_{upcc-ig}^{sy-c} = \mathbf{A}_{upcc-ic1}^{sy-c} = 0$. The inverter output admittance \mathbf{Y}_{inv} using traditional control method can be calculated as

$$\mathbf{Y}_{inv} = \begin{bmatrix} Y_{invdd} & Y_{invdq} \\ Y_{invqd} & Y_{invqq} \end{bmatrix} = \frac{\mathbf{A}_{upcc-ig}^{sy-sy} - \mathbf{A}_{D-ig}^{sy-sy} \mathbf{A}_{ad} \mathbf{B}}{\mathbf{I} + \mathbf{A}_{D-ig}^{sy-sy} (\mathbf{A}_{PI} + \mathbf{A}_{ad} (\mathbf{BC}))}. \quad (20)$$

Meanwhile, the PLL equivalent admittance \mathbf{Y}_{PLL} can be calculated as

$$\mathbf{Y}_{\text{PLL}} = \mathbf{Y}_{\text{inv_PLL}} - \mathbf{Y}_{\text{inv}} = \begin{bmatrix} Y_{\text{PLLdd}} & Y_{\text{PLLdq}} \\ Y_{\text{PLLqd}} & Y_{\text{PLLqq}} \end{bmatrix} = \frac{\mathbf{A}_{D\text{-ig}}^{\text{sy-sy}} (\mathbf{A}_{\text{upcc-D}}^{\text{sy-sy}} - \mathbf{A}_{\text{PI}} \mathbf{A}_{\text{upcc-ig}}^{\text{sy-c}} - \mathbf{A}_{\text{ad}} \mathbf{A}_{\text{upcc-ic1}}^{\text{sy-c}})}{\mathbf{I} + \mathbf{A}_{D\text{-ig}}^{\text{sy-sy}} (\mathbf{A}_{\text{PI}} + \mathbf{A}_{\text{ad}} (\mathbf{BC}))}. \quad (21)$$

2.3. Impedance-Based Stability Criterion

Under the weak grid condition, the grid impedance can be expressed as

$$\mathbf{Z}_g = \begin{bmatrix} Z_{\text{gdd}} & Z_{\text{gdq}} \\ -Z_{\text{gdq}} & Z_{\text{gdd}} \end{bmatrix} = \begin{bmatrix} sL_g & -\omega_1 L_g \\ \omega_1 L_g & sL_g \end{bmatrix}. \quad (22)$$

According to the Norton theorem, the equivalent circuit of the system using the traditional control method is shown in Figure 4. The inverter subsystem is equivalent to a parallel connection between the current source and inverter output admittance $\mathbf{Y}_{\text{inv_PLL}} = (\mathbf{Y}_{\text{inv}} // \mathbf{Y}_{\text{PLL}})$. The grid subsystem is equivalent to the grid impedance \mathbf{Z}_g and an ideal grid in the series connection.

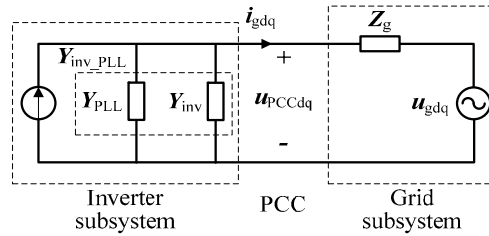


Figure 4. Equivalent circuit of the system with the traditional control method.

On the basis of the generalized Nyquist criterion [20], if the Nyquist curve for the eigenfunction of the return-ratio matrix \mathbf{L} does not encircle $(-1, j^* 0)$, the system is in a stable state. \mathbf{L} can be depicted as

$$\mathbf{L} = \mathbf{Z}_g \cdot \mathbf{Y}_{\text{inv_PLL}} = \begin{bmatrix} Z_{\text{gdd}} Y_{\text{dd}} & Z_{\text{gdq}} Y_{\text{qq}} \\ -Z_{\text{gdq}} Y_{\text{dd}} & Z_{\text{gdd}} Y_{\text{qq}} \end{bmatrix}. \quad (23)$$

Therefore, the eigenfunction of the return-ratio matrix \mathbf{L} can be calculated as

$$\begin{cases} l_1 = \underbrace{Z_{\text{gdd}} Y_{\text{dd}} / 2 + Z_{\text{gdd}} Y_{\text{qq}} / 2}_{x_1} - \underbrace{(Z_{\text{gdd}}^2 Y_{\text{dd}}^2 - 2Z_{\text{gdd}}^2 Y_{\text{dd}} Y_{\text{qq}} - 4Z_{\text{gdq}}^2 Y_{\text{dd}} Y_{\text{qq}} + Z_{\text{gdd}}^2 Y_{\text{qq}}^2)^{1/2} / 2}_{x_2} \\ l_2 = \underbrace{Z_{\text{gdd}} Y_{\text{dd}} / 2 + Z_{\text{gdd}} Y_{\text{qq}} / 2}_{x_1} + \underbrace{(Z_{\text{gdd}}^2 Y_{\text{dd}}^2 - 2Z_{\text{gdd}}^2 Y_{\text{dd}} Y_{\text{qq}} - 4Z_{\text{gdq}}^2 Y_{\text{dd}} Y_{\text{qq}} + Z_{\text{gdd}}^2 Y_{\text{qq}}^2)^{1/2} / 2}_{x_2} \end{cases}. \quad (24)$$

From (24), the retained component x_1 and secondary component x_2 can be defined as

$$\begin{cases} x_1 = \frac{1}{2} Z_{\text{gdd}} \cdot (Y_{\text{dd}} + Y_{\text{qq}}) \\ x_2 = \frac{1}{2} (Z_{\text{gdd}}^2 Y_{\text{dd}}^2 - 2Z_{\text{gdd}}^2 Y_{\text{dd}} Y_{\text{qq}} - 4Z_{\text{gdq}}^2 Y_{\text{dd}} Y_{\text{qq}} + Z_{\text{gdd}}^2 Y_{\text{qq}}^2)^{1/2} \end{cases}. \quad (25)$$

According to (25), the Bode diagrams of the retained component x_1 and secondary component x_2 are shown in Figure 5. When the distance between the two is the smallest, the magnitude of x_1 is -15.6 dB, the magnitude of x_2 is -47.2 dB. The magnitude of x_1 is 31.6 dB larger than that of x_2 , which is equivalent to 38.02 times. Therefore, ignoring the secondary components x_2 , (24) can be rewritten as

$$l_1 = l_2 = x_1 = \left(\frac{Z_{\text{gdd}}}{2} \right) \cdot (Y_{\text{dd}} + Y_{\text{qq}}). \quad (26)$$

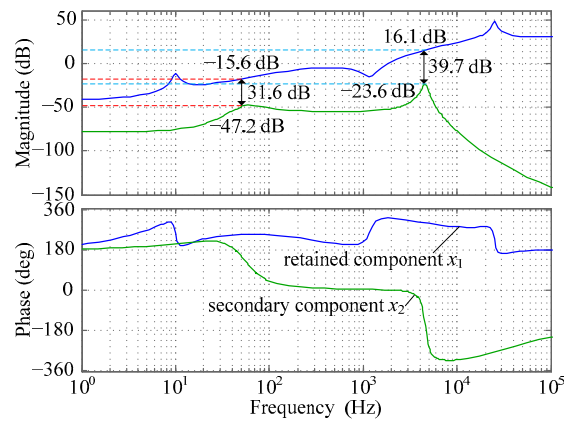


Figure 5. The Bode diagrams of the retained component x_1 and secondary component x_2 .

However, a dynamic interconnected system will be formed in the weak grid. The phase margin of the system may be insufficient. That results in increasing the distortion of grid-connected current. To guarantee enough stability and good dynamics, the range of phase margin of the system is usually required to be $30\text{--}60^\circ$ under the weak grid condition.

In the Nyquist curve, the intersection point for the eigenfunction and unit circle is defined as the system cut-off frequency f_i , and the location is determined as the phase margin of the system α_{PM} [21]. From (26), α_{PM} can be expressed as

$$\alpha_{PM} = 180^\circ - \arg\left(\frac{Z_{gdd}(f_i)}{2}\right) - \arg(Y_{dd}(f_i) + Y_{qq}(f_i)). \quad (27)$$

From (27), the system phase margin is increased by decreasing $\arg(Z_{gdd}(f_i)/2)$ and $\arg(Y_{dd}(f_i) + Y_{qq}(f_i))$. It is difficult to control the phase of grid impedance $\arg(Z_{gdd}(f_i)/2)$. Therefore, the target needs to be achieved by decreasing $\arg(Y_{dd}(f_i) + Y_{qq}(f_i))$.

2.4. Stability Analysis of Traditional Control Method

The Nyquist diagram of the eigenfunction with the traditional control method is shown as in Figure 6. The system cut-off frequency f_i is 181 Hz and the system phase margin α_{PM} is 16° , which does not satisfy the requirement of sufficient stability of the system. Therefore, the system phase margin should be improved under the traditional control method.

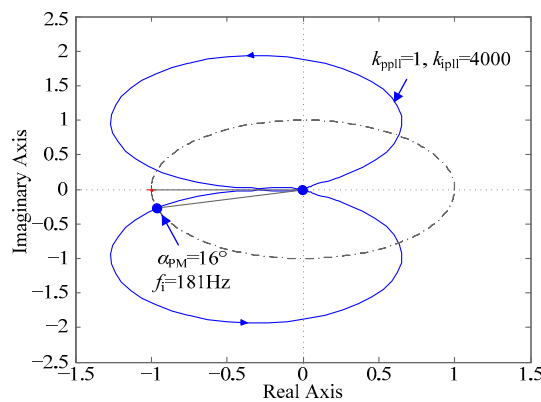


Figure 6. The Nyquist diagram of the eigenfunction with the traditional control method.

The Bode diagrams of inverter output admittance Y_{inv_PLL} using the traditional control method are shown in Figure 7. The amplitudes and phases of Y_{dd} , Y_{dq} , Y_{qd} and Y_{qq} can be obtained at the

system cut-off frequency, so $\arg(Y_{dd}(f_i) + Y_{qq}(f_i)) = 74^\circ$. Because the grid impedance is equivalent to the inductance, $\arg(Z_{gdd}(f_i)/2)$ is generally equal to 90° . According to (27), the system phase margin α_{PM} is 16° , which does not meet sufficient stability of the system. The results are consistent with those in Figure 6. Therefore, the system phase margin should be improved under the traditional control method. Specifically, the PLL shapes the Z_{qq} ($1/Y_{qq}$) as a negative incremental resistance that may destabilize the system. Meanwhile, $|Y_{dd}|$ and $|Y_{qq}|$ are far larger than $|Y_{dq}|$ and $|Y_{qd}|$, so $|Y_{dq}|$ and $|Y_{qd}|$ are equal to 0, which verifies the correctness of (23). Within the range of the error, the measurement results are in agreement with the model results, which proves the correctness of the model.

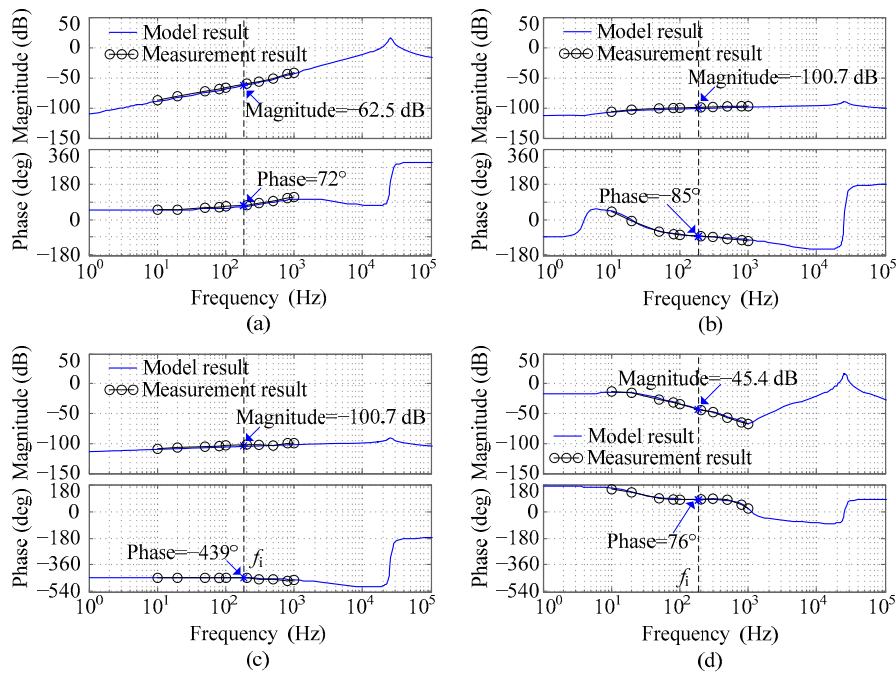


Figure 7. The Bode diagrams of inverter output admittance Y_{inv_PLL} of traditional control method. (a) Y_{dd} ; (b) Y_{qd} ; (c) Y_{dq} ; (d) Y_{qq} .

3. Admittance Reshaping Control Methods for Three-Phase Grid-Connected Inverter

3.1. Admittance Reshaping Technique 1 (the Feedforward PCC Voltage)

To improve the system’s stability, the proposed admittance reshaping technique 1 uses the feedforward PCC voltage to modify the inverter output admittance Y_{inv} , which is equivalent to adding the virtual admittance to connect in parallel with inverter output admittance. The system diagram of the proposed admittance reshaping technique 1—considering the effect of PLL—is shown in Figure 8. Inside the left dotted line of Figure 8, the control diagram of the proposed admittance reshaping technique 1—without considering the PLL effect—is presented. The vectors are converted between the system dq frame and the control dq frame that considers the PLL effect are shown outside the left dotted line of Figure 8.

From Figure 8, the feedforward matrix A_{com} can be defined as

$$A_{com} = \begin{bmatrix} G_{comdd} & 0 \\ 0 & G_{comqq} \end{bmatrix}. \tag{28}$$

From Figure 8, the dq admittance model of the proposed admittance reshaping technique 1 is obtained, as shown in Figure 9, where the matrix $A_{upcc-upcc}^{sy-c}$ can be obtained as

$$A_{u_{pcc}-u_{pcc}}^{sy-c} = \frac{\Delta u_{pccdq}^c}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{8dd} & A_{8dq} \\ A_{8qd} & -A_{8qq} \end{bmatrix} = \begin{bmatrix} 0 & u_{pccq}^{sy} G_{PLL} \\ 0 & -u_{pccd}^{sy} G_{PLL} \end{bmatrix}. \quad (29)$$

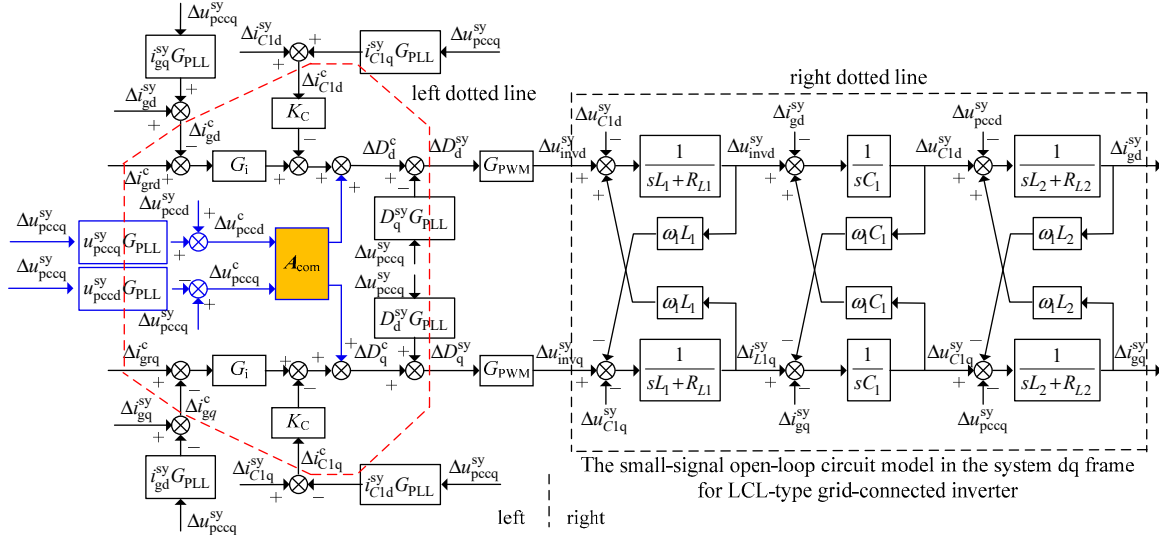


Figure 8. The system diagram of proposed admittance reshaping technique 1 considering the phase-locked loop (PLL) effect.

Therefore, the inverter output admittance Y_{invc_PLL} with the proposed admittance reshaping technique 1 can be expressed as

$$Y_{invc_PLL} = \begin{bmatrix} Y_{cdd} & Y_{cdq} \\ Y_{cq d} & Y_{cqq} \end{bmatrix} = \frac{A_{u_{pcc}-ig}^{sy-sy} + A_{D-ig}^{sy-sy} (A_{u_{pcc}-D}^{sy-sy} + A_{com} A_{u_{pcc}-upcc}^{sy-c} - A_{PI} A_{u_{pcc}-ig}^{sy-c} - A_{ad} (A_{u_{pcc}-ic1}^{sy-c} + B))}{I + A_{D-ig}^{sy-sy} (A_{PI} + A_{ad} (BC))}. \quad (30)$$

Without considering the PLL effect, $A_{u_{pcc}-D}^{sy-sy} = A_{u_{pcc}-ig}^{sy-c} = A_{u_{pcc}-ic1}^{sy-c} = 0$. The inverter output admittance Y_{invc} using the proposed admittance reshaping technique 1 can be calculated as

$$Y_{invc} = \begin{bmatrix} Y_{invcdd} & Y_{invcdq} \\ Y_{invcq d} & Y_{invcqq} \end{bmatrix} = \frac{A_{u_{pcc}-ig}^{sy-sy} + A_{D-ig}^{sy-sy} (A_{com} A_{u_{pcc}-upcc}^{sy-c} - A_{ad} B)}{I + A_{D-ig}^{sy-sy} (A_{PI} + A_{ad} (BC))}. \quad (31)$$

Next, the calculation process of the feedforward matrix A_{com} is introduced. The optimization function $G_p(s)$ of the inverter output admittance phase, which can be given as

$$G_p(s) = \frac{1 + k_\omega s}{1 + k_p k_\omega s} \cdot k_m, \quad (32)$$

where k_p is the proportional coefficient, k_ω is the phase coefficient, and k_m is the gain coefficient. k_p and k_ω can reduce the phase at the desired frequency and k_m can compensate for the amplitude offset at the desired frequency.

The Bode diagram of the optimization function $G_p(s)$ is shown in Figure 10. By selecting the appropriate parameters, the amplitude of $G_p(s)$ is 0 dB at the desired frequency and the phase reaches the minimum at the desired frequency.

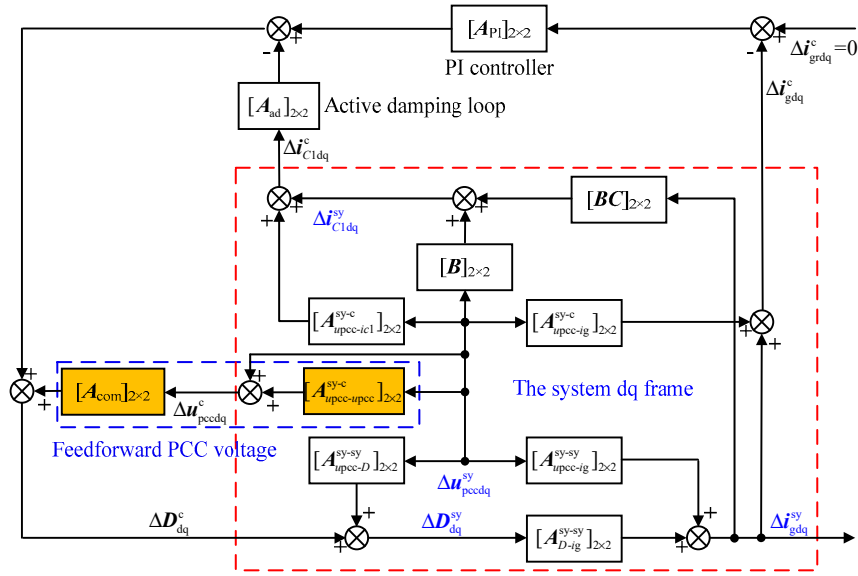


Figure 9. The dq admittance model of proposed admittance reshaping technique 1.

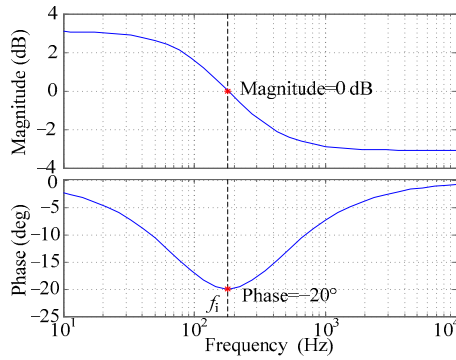


Figure 10. The Bode diagram of the optimization function $G_p(s)$.

Meanwhile, the optimization matrix A_p can be defined as

$$A_p = \begin{bmatrix} G_p & 0 \\ 0 & G_p \end{bmatrix}. \tag{33}$$

If the series correction between the optimization matrix A_p and inverter output admittance Y_{inv_PLL} is taken, the aim of compensating for the phase of inverter output admittance at the desired frequency will be realized. Meanwhile, the feedforward matrix A_{com} can also be obtained. Therefore, the inverter output admittance Y_{invc_PLL} with using the proposed admittance reshaping technique 1 can be rewritten as

$$Y_{invc_PLL} = A_p Y_{inv_PLL}. \tag{34}$$

Therefore, G_{comdd} in the feedforward matrix can be expressed as

$$G_{comdd} = \frac{(1 - k_m k_p) k_\omega s + (1 - k_m)}{k_m (k_p k_\omega s + 1)} \cdot \frac{G_1 - G_2}{G_{PWM} G_{PLL} u_{pccd}^{sy}}, \tag{35}$$

where $G_1 = 1 + \frac{(sL_1 + R_{L1})sC_1}{(1 + sC_1 R_{C1})}$ and $G_2 = L_1 C_1 \omega_1^2$.

Meanwhile, G_{comqq} in the feedforward matrix can also be expressed as

$$G_{\text{comqq}} = \frac{(1 - k_m k_p) k_\omega s + (1 - k_m)}{k_m (k_p k_\omega s + 1)} \cdot \frac{G_1 - G_2 - G_3}{G_{\text{PWM}} G_{\text{PLL}} u_{\text{pccd}}^{\text{sy}}}, \quad (36)$$

where $G_3 = G_{\text{PLL}} G_{\text{PWM}} (D_d^{\text{sy}} + G_i i_{\text{gd}}^{\text{sy}} + K_C i_{\text{C1d}}^{\text{sy}})$.

Using the proposed admittance reshaping technique 1, $Y_{\text{invc_PLL}}$ is equivalent to the parallel connection between Y_{PLL} and Y_{invc} . Therefore, the proposed admittance reshaping technique 1 is equivalent to adding the virtual admittance to connect in parallel with inverter output admittance Y_{inv} .

The Bode diagrams of inverter output admittances $Y_{\text{invc_PLL}}$ with the proposed admittance reshaping technique 1 are shown in Figure 11, where $\arg(Y_{\text{cdd}}(f_i) + Y_{\text{cqq}}(f_i)) = 54^\circ$. Because the grid impedance is equivalent to the inductance, $\arg(Z_{\text{gdd}}(f_i)/2)$ is generally equal to 90° . According to (27), the system phase margin α_{PM} is 36° , which meets sufficient stability of the system. Therefore, the proposed admittance reshaping technique 1 increases the system phase margin. At the same time, the measurement results are in good agreement with the modified model, which proves the correctness of the modified model.

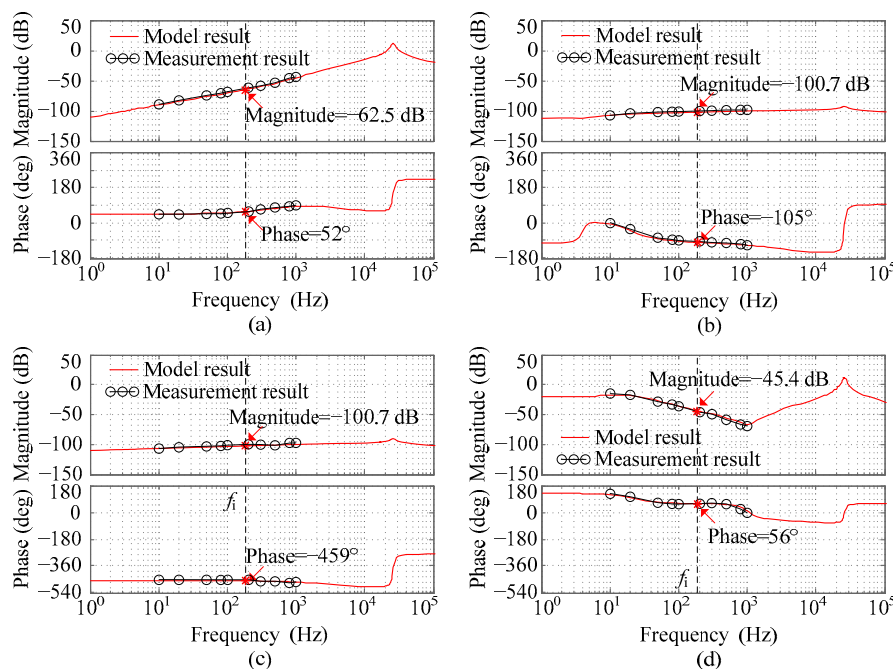


Figure 11. The Bode diagrams of inverter output admittances $Y_{\text{invc_PLL}}$ with proposed admittance reshaping technique 1. (a) Y_{cdd} ; (b) Y_{cqd} ; (c) Y_{cdq} ; (d) Y_{cqq} .

3.2. Admittance Reshaping Technique 2 (the Active Damping Controller)

To increase the system phase margin, the proposed admittance reshaping technique 2 adopts the active damping controller to reconstruct the PLL equivalent admittance Y_{PLL} . The control block diagram of the improved PLL is shown in Figure 12. The proposed admittance reshaping technique 2 reduces the phase of PLL equivalent admittance at the system cut-off frequency, which improves system stability.

From Figure 12, the closed-loop transfer function of PLL G_{PLLc} using the proposed admittance reshaping technique 2 can be expressed as

$$G_{\text{PLLc}} = \frac{T_{\text{PLL}}}{s + u_{\text{pccd}}^{\text{sy}} T_{\text{PLL}} + \frac{G_{\text{AD}}}{1 + G_{\text{AD}}} T_{\text{PLL}}}. \quad (37)$$

Therefore, the matrix $A_{u_{\text{pccd}}^{\text{sy}}-D}^{\text{sy-sy}}$ in (8) can be rewritten as

$$A_{upcc-D_c}^{sy-sy} = \frac{\Delta D_{dq}^{sy}}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{3cdd} & -A_{3cdq} \\ A_{3cq d} & A_{3cqq} \end{bmatrix} = \begin{bmatrix} 0 & -D_q^{sy} G_{PLLc} \\ 0 & D_d^{sy} G_{PLLc} \end{bmatrix}. \quad (38)$$

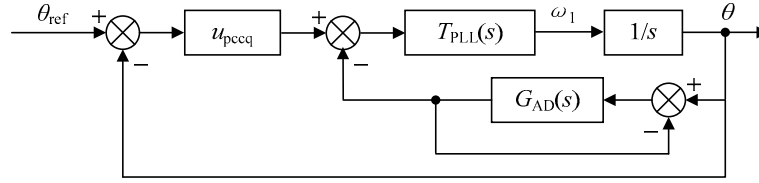


Figure 12. The control block diagram of the improved PLL.

Meanwhile, the matrix $A_{upcc-ig}^{sy-c}$ in (10) can be rewritten as

$$A_{upcc-ig_c}^{sy-c} = \frac{\Delta i_{gdq}^c}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{4cdd} & A_{4cdq} \\ A_{4cq d} & -A_{4cqq} \end{bmatrix} = \begin{bmatrix} 0 & i_{gq}^{sy} G_{PLLc} \\ 0 & -i_{gd}^{sy} G_{PLLc} \end{bmatrix}. \quad (39)$$

At the same time, the matrix $A_{upcc-ic1}^{sy-c}$ in (12) can be rewritten as

$$A_{upcc-ic1_c}^{sy-c} = \frac{\Delta i_{C1dq}^c}{\Delta u_{pccdq}^{sy}} = \begin{bmatrix} A_{5cdd} & A_{5cdq} \\ A_{5cq d} & -A_{5cqq} \end{bmatrix} = \begin{bmatrix} 0 & i_{C1q}^{sy} G_{PLLc} \\ 0 & -i_{C1d}^{sy} G_{PLLc} \end{bmatrix}. \quad (40)$$

Therefore, the inverter output admittance Y_{inv_PLLc} using the proposed admittance reshaping technique 2 can be expressed as

$$Y_{inv_PLLc} = \begin{bmatrix} Y_{cdd} & Y_{cdq} \\ Y_{cq d} & Y_{cqq} \end{bmatrix} = \frac{A_{upcc-ig}^{sy-sy} + A_{D-ig}^{sy-sy} (A_{upcc-D_c}^{sy-sy} - A_{PI} A_{upcc-ig_c}^{sy-c} - A_{ad} (A_{upcc-ic1_c}^{sy-c} + B))}{I + A_{D-ig}^{sy-sy} (A_{PI} + A_{ad} (BC))}. \quad (41)$$

Next, the calculation process of the active damping controller G_{AD} is introduced. According to (32), the closed-loop transfer function of PLL G_{PLLc} using the proposed admittance reshaping technique 2 can be rewritten as

$$Y_{inv_PLLc} = A_p Y_{inv_PLL}. \quad (42)$$

Therefore, the active damping controller G_{AD} can be obtained as

$$G_{AD} = \frac{(1 - G_p)s}{(G_p - 1)s + T_{PLL}G_p}. \quad (43)$$

Using proposed admittance reshaping technique 2, Y_{inv_PLLc} is equivalent to the parallel connection between Y_{PLLc} and Y_{inv} . Therefore, the proposed admittance reshaping technique 2 is equivalent to adding the virtual admittance to connect in parallel with the PLL equivalent admittance Y_{PLL} . Using the proposed admittance reshaping technique 2, the reconstructed inverter output admittances Y_{inv_PLLc} can achieve the same purpose as proposed admittance reshaping technique 1.

3.3. Design Method of Control Parameters

By selecting the appropriate parameters k_p and k_ω , the phase of the inverter output admittance is reduced at the system cut-off frequency, which increases the system phase margin. In addition, the amplitude of the inverter output admittance at the system cut-off frequency will be changed. Therefore, it is essential to select the appropriate parameter k_m to compensate for the amplitude offset.

The phase-frequency function of $G_p(s)$ is expressed as

$$\phi_p(\omega) = -\arctan\left(\frac{(k_p - 1)k_\omega\omega}{k_p k_\omega^2 \omega^2 + 1}\right). \quad (44)$$

If $d\phi_p(\omega)/d\omega = 0$, the maximum compensation angular frequency ω_m can be obtained as

$$\omega_m = 1/(\sqrt{k_p k_\omega}). \quad (45)$$

Combining (44) and (45), the maximum compensation phase ϕ_m can be derived as

$$\phi_m = -\arctan\left(\frac{k_p - 1}{2\sqrt{k_p}}\right). \quad (46)$$

To maintain the amplitude of the inverter output admittance at the system cut-off frequency, the amplitude of $G_p(s)$ should be 0 dB at the system cut-off frequency, that is, $|G_p(j2\pi f_i)| = 1$. The gain coefficient of phase compensation k_m can be expressed as

$$k_m = \sqrt{\frac{k_p^2 k_\omega^2 \omega_m^2 + 1}{k_\omega^2 \omega_m^2 + 1}}. \quad (47)$$

Using the traditional control method, the system cut-off frequency f_i is 181 Hz, and the system phase margin α_{PM} is 16° , which does not meet sufficient stability of the system. The parameter design process of the proposed control methods can be illustrated as follows. Firstly, the maximum compensation phase frequency ω_m should be equivalent to the system cut-off angular frequency $\omega_i = 2\pi f_i \approx 1137 \text{ rad/s}$. Secondly, the range of maximum compensation phase ϕ_m is $-14^\circ \sim -44^\circ$ on the basis of the required system phase margin. Then, the range of k_p is 1.6383~5.55 by (46). Next, the range of k_ω is $3.7325 \times 10^{-4} \sim 6.8698 \times 10^{-4}$ by (45). Finally, the range of k_m is 1.28~2.3558 by (47).

3.4. Contrast Analysis of System Stability

The Nyquist diagrams of the eigenfunction are shown in Figure 13. Using the traditional control method, the system phase margin α_{PM} is separately 16° . Using the proposed control methods, the system phase margins α_{PM} are separately 30° and 60° , which are increased by 14° and 44° , respectively. The result is the same as the designed maximum compensation phase, which meets sufficient stability and good dynamics of the system.

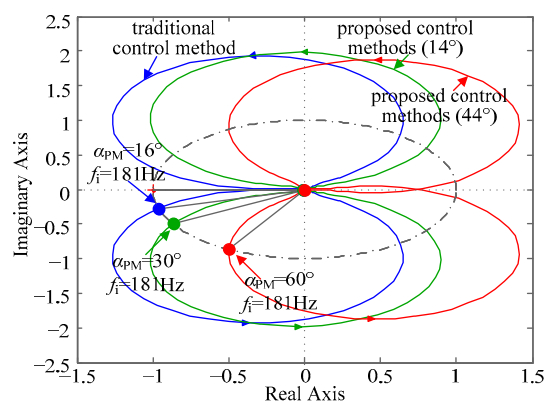


Figure 13. The Nyquist diagrams of the eigenfunction.

4. Experiments Verification

To prove the validity of the theoretical analysis, the experimental platform for a three-phase grid-connected system was built, as shown in Figure 14a, which included a three-phase grid-connected inverter, a detection and data acquisition circuit (voltage and current sensors), and an industrial personal computer. The three-phase grid-connected inverter in Figure 14b includes the main circuit, control board and LCL filter circuit. The system parameters are shown in Table 1.

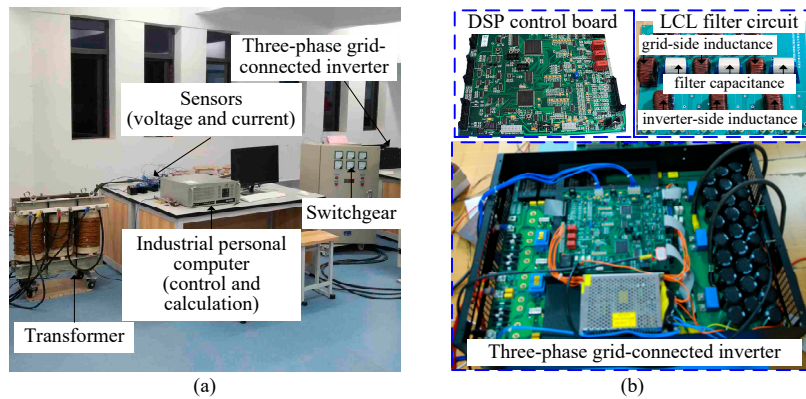


Figure 14. Experimental platform for a three-phase grid-connected system. (a) Whole; (b) Details.

Table 1. System parameters.

Parameter/Unit	Value
DC voltage U_{dc}/V	720
Inverter-side inductor $L_1/mH, R_{L1}/\Omega$	0.6, 0.01
Filter capacitor $C_1/\mu F$	10
Grid-side inductor $L_2/mH, R_{L2}/\Omega$	0.15, 0.001
Grid inductor L_g/mH	0.05
Grid-connected current reference $i_{grd}^s, i_{grq}^s/A$	-73, 0
Grid-connected current $i_{gd}^s, i_{gq}^s/A$	-73, 0
PCC voltage $u_{pccd}^s, u_{pccq}^s/V$	311, 0
Filter capacitor current $i_{C1d}^s, i_{C1q}^s/A$	0.03, 0.90
Duty ratio D_d^s, D_q^s	0.55, 0.01
PLL PI controller k_{ppll}, k_{ipll}	1, 4000
Grid current loop PI controller k_{pi}, k_{ii}	0.45, 1000
Active damping coefficient K_C	1.15
Fundamental frequency f_1/Hz	50
Switching frequency f_s/kHz	10

To improve the stable operation range, the stability enhancement method was proposed [14] by largely reducing the PLL bandwidth, abbreviated as the traditional control method. The traditional control method, the proposed admittance reshaping techniques 1 and 2, the experimental waveforms of PCC voltage u_{pcc} and the grid-connected current i_g are shown in Figures 15–17. The experimental results of the grid-connected current in the three cases are shown in Table 2.

In the case of the traditional control method from Figure 15a, the total harmonic distortion (THD) of the steady-state grid-connected current is 9.71%. The harmonic contents of the grid-connected current are large. The reason is that the phase margin of the system may be insufficient using the traditional control method. Therefore, it is essential to propose the control method to increase the system phase margin.

To increase the system phase margin, admittance reshaping techniques 1 and 2 are proposed, which use a set of parameters within the design range shown in Table 3. In the case of the proposed admittance reshaping techniques 1 and 2 from Figures 16a and 17a, the THD of the steady-state grid-connected

currents are 1.72% and 1.93%. In both cases, the harmonic contents of the grid-connected current are greatly attenuated. The reason is that the proposed admittance reshaping techniques 1 and 2 increase the system damping and improve system stability. Therefore, the validity of the theoretical analysis is verified.

As can be seen in Figures 15b, 16b and 17b, the reference grid-connected current increases from 36.5A to 73A in the case of the traditional control method and the proposed admittance reshaping techniques 1 and 2. The transient experimental results in the three cases are similar. Therefore, compared with the traditional control method, the proposed admittance reshaping techniques 1 and 2 can ensure system dynamics.

Table 2. The experimental results of the grid-connected current.

Case	THD of the Steady-State Grid-Connected Current
Traditional control method	9.71%
Admittance reshaping technique 1 (within the parameter design range)	1.72%
Admittance reshaping technique 2 (within the parameter design range)	1.93%
Admittance reshaping technique 1 (without the parameter design range)	5.62%
Admittance reshaping technique 2 (without the parameter design range)	5.84%

Table 3. Different sets of parameters.

Case	ϕ_m	k_p	k_ω	k_m
within the design range	-20°	2.04	6.16×10^{-4}	1.43
without the design range	-10°	1.42	7.38×10^{-4}	1.19

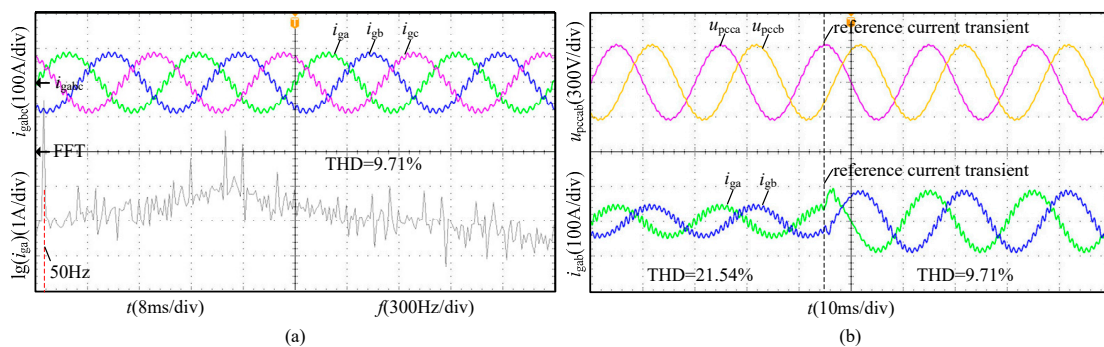


Figure 15. Experimental waveforms of point of common coupling (PCC) voltage u_{pcc} and grid-connected current i_g with traditional control method. (a) Steady state; (b) Transient.

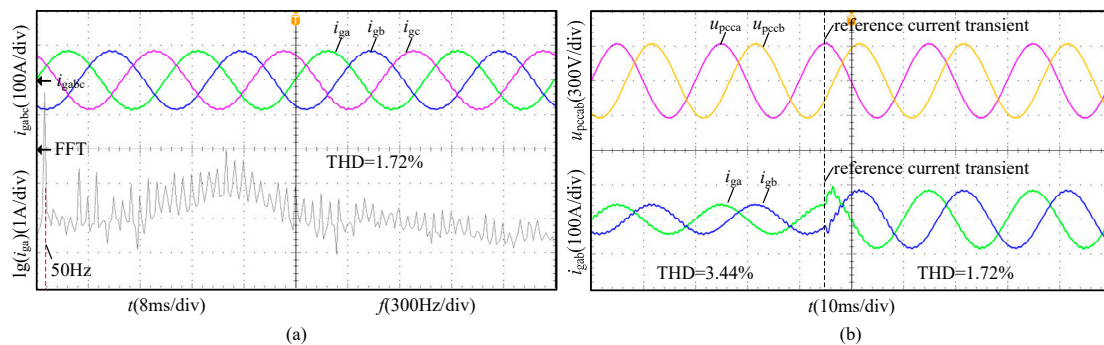


Figure 16. Experimental waveforms of u_{pcc} and i_g with proposed admittance reshaping technique 1 within the parameter design range. (a) Steady state; (b) Transient.

To verify the reasonableness of the parameter design for the proposed admittance reshaping techniques 1 and 2, another set of parameters without the design range is shown in Table 3. The experimental waveforms of PCC voltage u_{pcc} and grid-connected current i_g in both cases are shown as Figures 18 and 19. The experimental results of the grid-connected current in both cases are shown in Table 2.

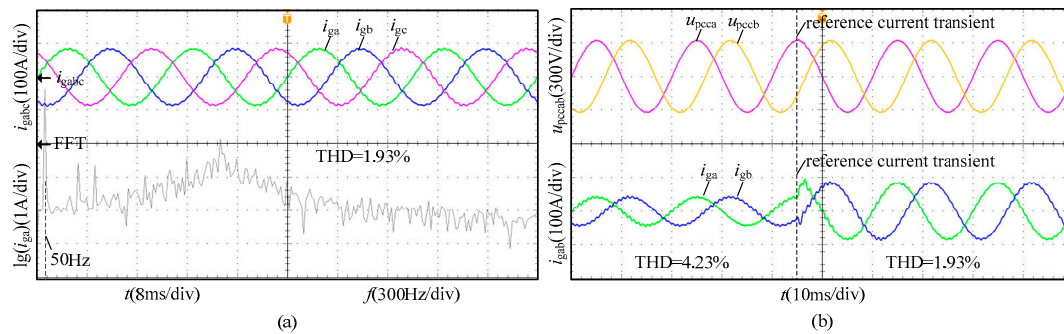


Figure 17. Experimental waveforms of u_{pcc} and i_g with proposed admittance reshaping technique 2 within the parameter design range. (a) Steady state; (b) Transient.

From Figures 18a and 19a, the THD of the steady-state grid-connected current is 5.62% and 5.84% in the case of the proposed control methods without the design range. The THD of the grid-connected current in both cases is less than that in Figure 15a with the traditional control method, but greater than that in Figures 16a and 17a within the design range. The reason is that the phase margin of the system has been improved but it has not yet met sufficient stability of the system. Therefore, the reasonableness of the parameter design is verified for the proposed control methods.

As can be seen in Figures 15b, 18b and 19b, the reference grid-connected current increases from 36.5 A to 73 A and the transient experimental results in the three cases are similar. Therefore, compared with the traditional control method, the proposed control methods without the design range can also ensure the system dynamics.

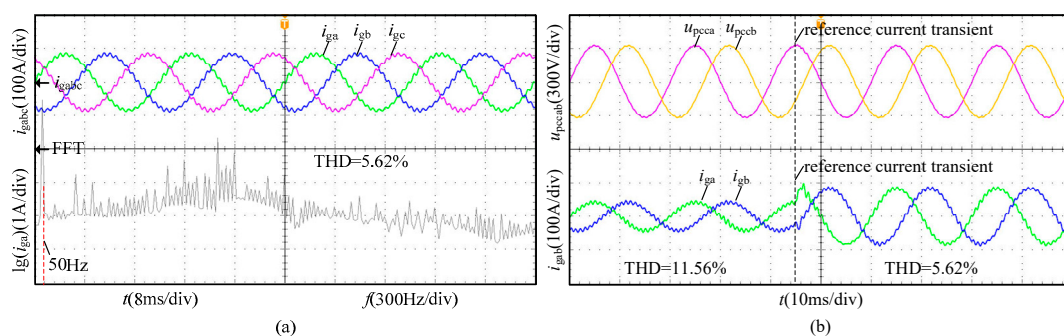


Figure 18. Experimental waveforms of u_{pcc} and i_g with proposed admittance reshaping technique 1 without the parameter design range. (a) Steady state; (b) Transient.

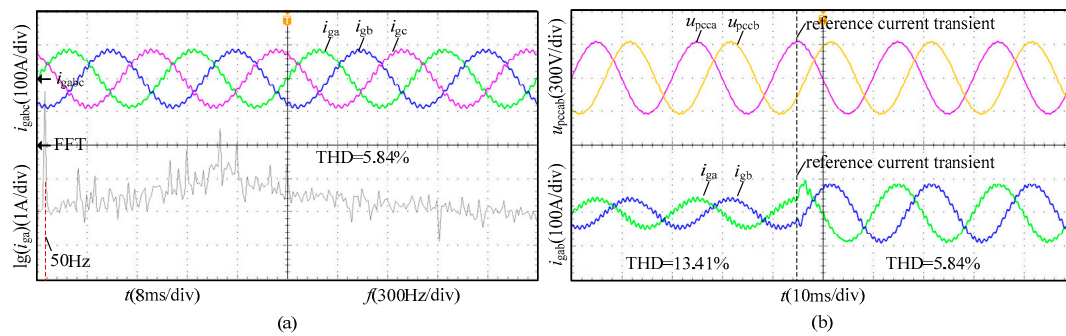


Figure 19. Experimental waveforms of u_{pcc} and i_g with proposed admittance reshaping technique 2 without the parameter design range. (a) Steady state; (b) Transient.

5. Conclusions

The negative impact of PLL on system stability is caused by the range of negative incremental resistance. It will increase impedance coupling between inverters and grid, which reduces the system phase margin or leads to system instability. Therefore, two admittance reshaping control methods that consider the PLL effect are proposed to improve system damping. The first reshaping technique uses the feedforward PCC voltage to modify the inverter output admittance. The second reshaping technique adopts the active damping controller to reconstruct the PLL equivalent admittance. The proposed control methods not only increase the system phase margin but also ensure the system dynamic response speed. The total harmonic distortion of the steady-state grid-connected current is reduced to less than 2%. Furthermore, a specific design method of control parameters is depicted. Finally, experimental results are provided to prove the validity of the proposed control methods. Still, the paper does not study the effect of time delay on the proposed control methods, which is an important topic to be explored in the future.

Author Contributions: L.Y. and Y.C. provided the original idea for this paper. L.Y., A.L. and K.H. organized the manuscript and attended the discussions when analysis and verification were carried out. All the authors gave comments and suggestions for the writing of and descriptions in the manuscript.

Funding: This research was supported by the National Key R&D Program of China under Grant No. 2017YFB0902000, and the Science and Technology Project of State Grid under Grant No. SGXJ0000KXJS1700841.

Conflicts of Interest: The authors declare no conflict of interest.

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