A Review of Modular Multilevel Converters for Stationary Applications

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Abstract: A modular multilevel converter (MMC) is an advanced voltage source converter applicable to a wide range of medium and high-voltage applications. It has competitive advantages such as quality output performance, high modularity, simple scalability, and low voltage and current rating demand for the power switches. Remarkable studies have been carried out regarding its topology, control, and operation. The main purpose of this review is to present the current state of the art of the MMC technology and to offer a better understanding of its operation and control for stationary applications. In this study, the MMC configuration is presented regarding its conventional and advanced submodule (SM) and overall topologies. The mathematical modeling, output voltage, and current control under different grid conditions, submodule balancing control, circulating current control, and modulation methods are discussed to provide the state of the MMC technology. The challenges linked to the MMC are associated with submodule balancing control, circulating current control, control complexity, and transient performance. Advanced nonlinear and predictable control strategies are expected to improve the MMC control and performance in comparison with conventional control methods. Finally, the power losses associated with the advanced wide bandgap (WBG) power devices (such as SiC, GaN) are explored by using different modulation schemes and switching frequencies. The results indicate that although the phase-shifted carrier-based pulse width modulation (PSC-PWM) has higher power losses, it outputs a better quality voltage with lower total harmonic distortion (THD) in comparison with phase-disposition pulse width modulation (PD-PWM) and sampled average modulation pulse width modulation (SAM-PWM). In addition, WBG switches such as silicon carbide (SiC) and gallium nitride (GaN) devices have lower power losses and higher efficiency, especially at high switching frequency in the MMC applications.

Keywords: modular multilevel converter (MMC); submodule topology; output voltage and current control; submodule balancing control; circulating current control; nonlinear and predictive control; power losses; WBG technology (SiC and GaN), MPC for MMC; grid applications; smart grid; battery inverters

1. Introduction

The modular multilevel converter (MMC), as a recently developed member of the multilevel converter family, was first proposed by Lesnicar and Marquardt in 2002 [1]. In 2010, this innovative converter was first commercially used by Siemens in San Francisco's Trans bay project [2]. Since its first introduction, the MMC has gained considerable attention and development owing to its

promising advantages such as excellent output performance, high modularity, simple scalability, and low voltage and current rating demand for the power switches [3,4]. These are clear advantages for the MMC over the traditional two-level and multilevel converters [5]. The MMC is particularly applicable to a wide range of medium and high-voltage power conversion systems, such as high-voltage direct current (HVDC) transmission systems [6–8], medium voltage motor drives [9–12], renewable energy systems [13–15], battery energy storage systems (BESS) [16–18], static synchronous compensator (STATCOM) [19,20], (hybrid) electrical vehicle chargers and drivers [21–24], and power interfacing applications [25,26].

The main purpose of this review paper is to present the current state of the art of the MMC technology and offer a better understanding of its operation and control. In this context, a detailed review is conducted associated with the main research issues regarding circuit topologies, mathematical modeling, control schemes, and modulation methods. The MMC circuit configuration is reviewed comprehensively from the perspective of the submodule and overall topologies. Despite limited DC fault tolerance [27,28], the half-bridge submodule (HBSM) is much preferred commercially among a variety of two-level and multilevel topologies considering its simple configuration and low cost. Advanced overall topologies are reported over the past years to meet application-oriented requirements. The MMC control methods are developed and reported with respect to the output voltage and current regulation [29], submodule balancing [30], and circulating current elimination [31] or injection [32]. Meanwhile, nonlinear and predictive controls [33] provide a solution to improve the MMC dynamic response instead of using a conventional proportional integral (PI) regulator or resonant controller. The modulation techniques of the power converter [34] directly affect the output value and output quality on power semiconductors. Numerous studies have been carried out to improve the modulation methods and are considered in this review. The emerging WBG technology [35] leads to a revolution in power electronics, which is prospected with power losses estimation using different modulation techniques in the MMC application.

The remainder of this paper is organized as follows. Section 2 introduces a variety of conventional and advanced submodule (SM) topologies together with overall architectures depending on the phase structure and arm connection mode. This is followed by an investigation of the MMC mathematical modeling and control strategies in Section 3, including output voltage and current control, submodule balancing control, circulating current control, and nonlinear and predictive control. Several MMC multilevel modulation techniques are presented in Section 4. Section 5 reviews and prospects the incorporation of advanced WBG technology together with power losses evaluation with various PWM modulation methods. Finally, the concluding remarks are drawn in Section 6.
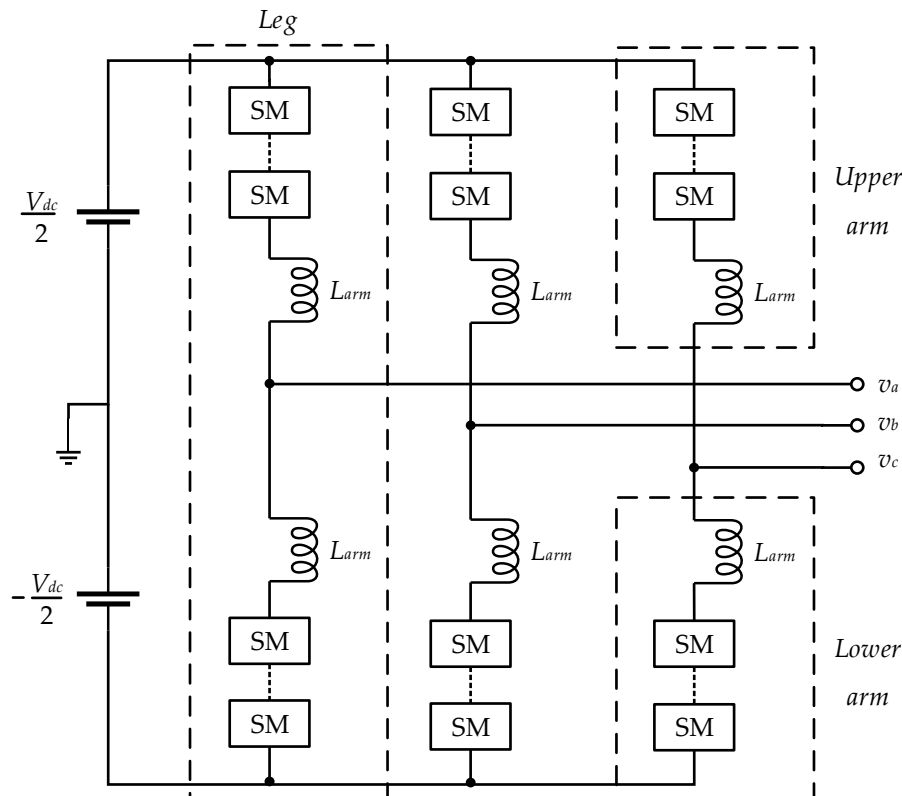
Figure 1. Generalized configuration of a three-phase modular multilevel converter (MMC).

2. MMC Topologies

2.1. Submodule Topologies

The generalized configuration of a three-phase MMC is comprised of a DC terminal, an AC terminal, and a converting kernel involving three phase legs, as shown in Figure 1. Each leg/phase has two symmetric arms referred to as the upper arm and lower arm. The upper arm and lower arm contain a group of identical submodules connected in series together with a chock inductor to suppress high-frequency components in the arm current. An MMC can achieve bidirectional power conversion.

2.1.1. Two-Level Submodule Topologies

The SM is the fundamental component of an MMC. During the past two decades, researchers have proposed a range of submodule topologies. According to the output voltage level, these submodules can be classified into two categories: two-level submodule topologies with a single source and multilevel submodule topologies with multiple sources.

Among all the SM topologies, the half-bridge submodule (HBSM) [1] is the most popular configuration thanks to its simple structure together with a low system cost. The HBSM is comprised of two power switches with anti-parallel diodes and a floating capacitor, as shown in Figure 2a. The submodule voltage can be switched to zero or capacitor voltage v_{c1}, depending on whether the capacitor is bypassed or inserted. Thus, the HBSM is also named as the chopper SM. One apparent disadvantage of an HBSM is its vulnerability to DC fault current.
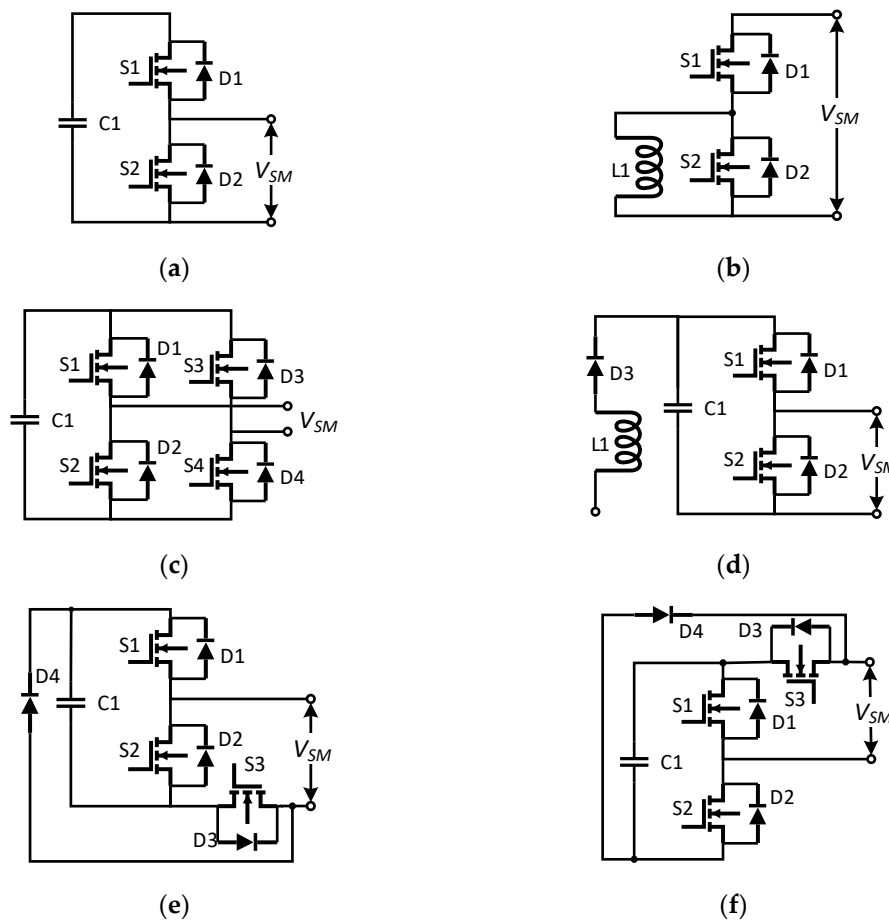
Currently, power converters are in majority voltage source converters (VSC), while current source converters (CSC) are less common. In terms of submodule for current source MMCs, an inductor replaces the capacitor in the HBSM [36], and the anti-parallel diodes are connected in series with the switching devices (Figure 2b). The output current is either zero ($L1$ bypassed) or the inductor current ($L1$ inserted).

Another well-known SM topology for MMC is a full-bridge structure (FBSM) [37]. An FBSM has two half-bridge legs with one floating capacitor. Each leg includes two switches with anti-parallel diodes. Its configuration is shown in Figure 2c. The output voltages can be zero, v_c, and $-v_c$, which enables FBSMs to counter DC failure current. To reduce the cost of power devices, some studies [38,39] proposed unidirectional topologies in which certain IGBT(s) are substituted by a diode(s).

A kind of self-balancing submodule (SBSM) is introduced in [40,41]. It is composed of the HBSM with an inductor and one diode (Figure 2d). It can self-balance unipolar voltage due to the clamped diode D3. This topology allows the submodule to balance capacitor voltage automatically (without voltage balancing algorithm).

To enhance the DC fault blocking capability of the HBSM, a clamp-single submodule (CSSM) [42] is proposed to suppress failure current. A clamp-single cell is also named a unipolar full-bridge SM self-blocking SM. A CSSM has two types of configurations (Figure 2e and Figure 2f) composed of a half-bride module connected with a transistor and a diode. During normal operation, S3 is always conducting. When a DC fault is detected, all transistors are set to off to block the short-circuit current.

Another concept to tackle the vulnerability of the HBSM during DC fault is to introduce thyristors to the half-bridge cell. For instance, the study in [27] proposes a single-thyristor HBSM and double-thyristor HBSM where thyristor(s) are connected in the terminal shown in Figure 2g and Figure 2h, respectively. The thyristors are always turned off during normal operation and are triggered to force the current to flow through it once the DC short failure is monitored. The double-thyristor structure has an advantage compared to the single-thyristor cell in terms of bidirectional current. It is cost-effective compared to other topologies with a DC blocking function such as FBSM, since there are no extra switching power losses during normal operation.
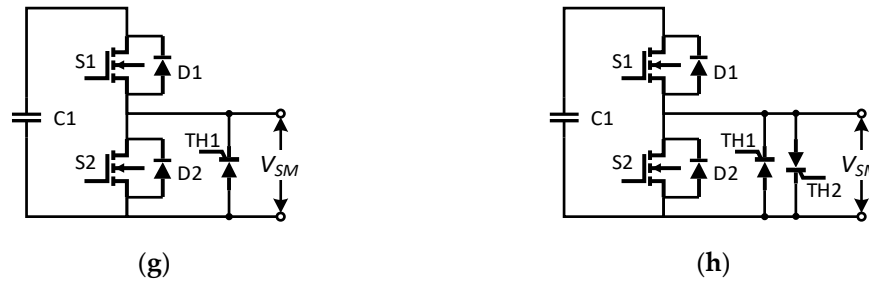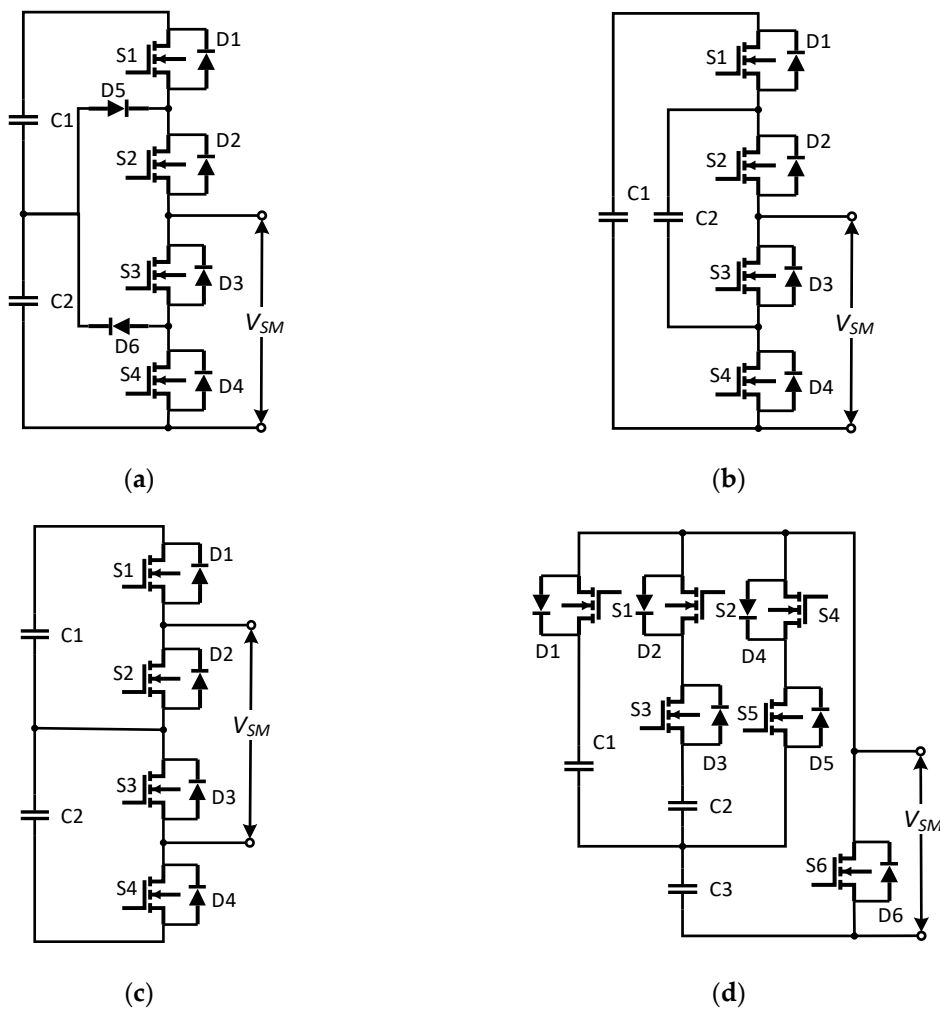

(**a**)

(**b**)

(**c**)

(**d**)

(**e**)

(**f**)

(**g**)

(**h**)

Figure 2. Two-level submodule topologies: (**a**) half-bridge submodule (HBSM); (**b**) current source HBSM; (**c**) full-bridge structure (FBSM); (**d**) self-balancing submodule (SBSM); (**e**) clamp-single submodule (CSSM) type-I; (**f**) CSSM type-II; (**g**) Single-thyristor HBSM; (**h**) Double-thyristor HBSM.

2.1.2. Multilevel Submodule Topologies

Neutral point clamped (NPC) and flying capacitor (FC) concepts are classical multilevel converter topologies. They were also introduced as three-level submodules in MMCs. The circuit configurations of the NPC submodule (NPCSM) and FC submodule (FCSM) [43,44] are presented in Figure 3a and Figure 3b, respectively. NPCSM contains four IGBT devices with anti-parallel diodes, two clamping diodes, and two capacitors. FCSM includes similar components except for the clamping diodes. Both of them can generate three voltage levels: $v_{c1} + v_{c2}$, v_{c2}, zero for NPCSM, and v_{c1}, $v_{c1} - v_{c2}$ or v_{c2}, zero for FCSM.

The cascaded half-bridge submodule (CHBSM) [45] is another configuration that outputs three voltage states: $v_{c1} + v_{c2}$, v_{c1} or v_{c2}, and zero. It is composed of two series-connected half-bridge cells, as drawn in Figure 3c.
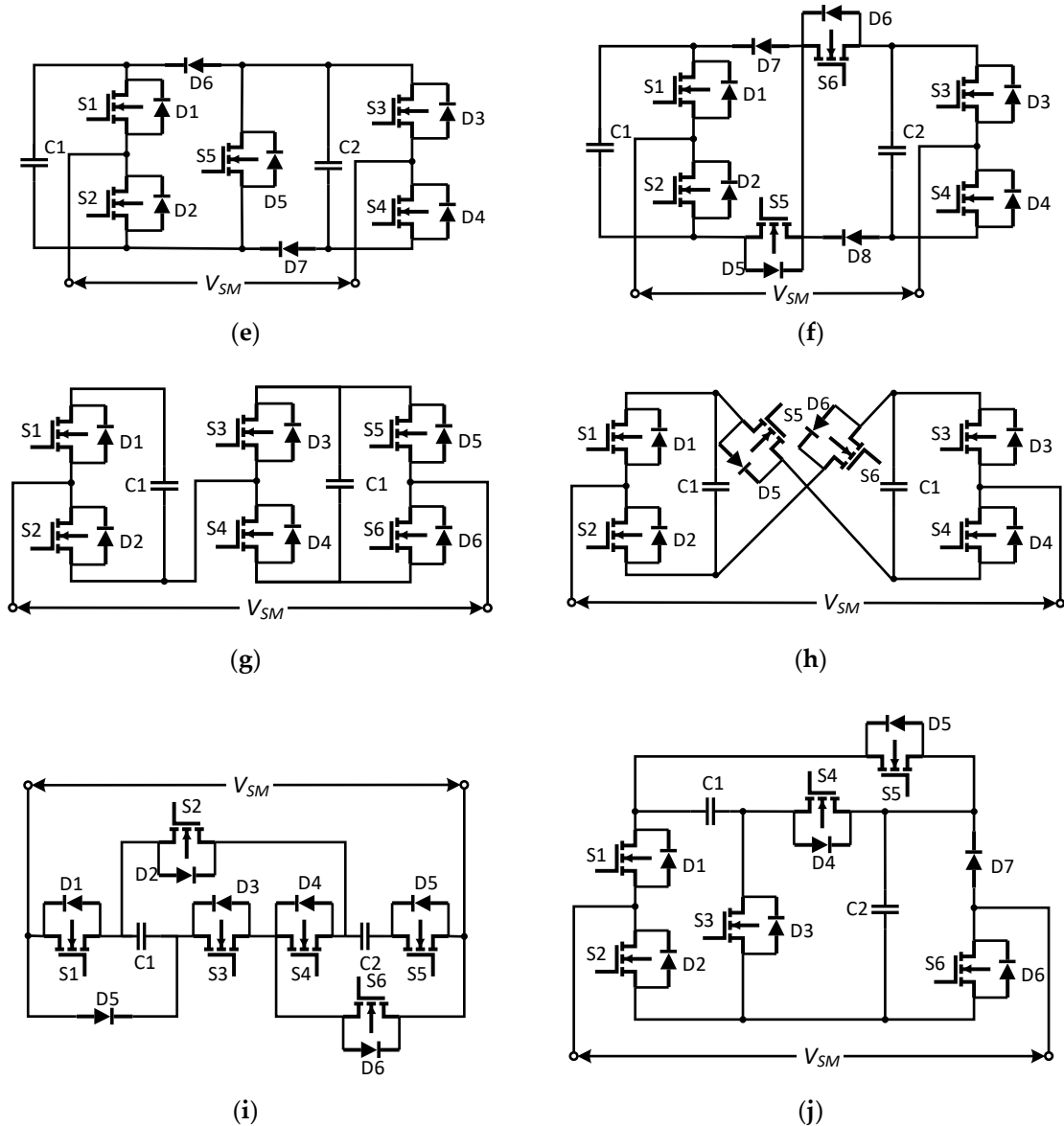

(**a**)

(**b**)

(**c**)

(**d**)

Figure 3. Multilevel submodule topologies: (**a**) neutral point clamped submodule (NPCSM); (**b**) flying capacitor submodule (FCSM); (**c**) cascaded half-bridge submodule (CHBSM); (d) stacked switched capacitor submodule (SSCSM); (**e**) clamp-double submodule (CDSM) type-I; (**f**) CDSM type-II; (**g**) hybrid submodules (HSM); (**h**) cross-connected submodule (CCSM); (**i**) switched capacitor submodule (SCSM); (**j**) composite three-level submodule (CSM).

With respect to submodule weight and size, the storage capacitor has a large influence. To reduce its volume, a compact submodule topology [46] was proposed with a stacked switched capacitor (SSC) energy buffer, as shown in Figure 3d. The SSC energy buffer refers to C1, C2, C3, and S3 along with S5. C3 is the main voltage source. C1 and C2 act as active supporting capacitors to compensate C3 voltage. Compared with HBSM, the total volume of SSCSM capacitors can be decreased by 40% at least.

A clamp-double submodule (CDSM) [47] (Figure 3e) consists of two identical HBSMs connected by two extra diodes and an IGBT, which is always on during normal operation. A clamp-double cell can generate a three-level voltage: $v_{c1} + v_{c2}$, v_{c1}/v_{c2}, and zero. In the case of DC fault, all the power devices are set off to resist the DC short-circuit current. A CDSM has only half utilization of the capacitor voltages ($-v_{c1}$ or $-v_{c2}$) in blocking mode. Therefore, using one extra IGBT is advised to be involved in the CDSM [48] (Figure 3f) to output $-2v_{c1}$ as blocking voltage. One apparent

weakness of a CDSM is the increased power losses, since all the switches work during normal operation.

Hybrid submodules (HSM) are generally based on the HBSM, as their primary purpose is to enable it to withstand DC fault with less components [49,50]. As shown in Figure 3g, a hybrid cell is comprised of series-connected HBSM and FBSM. It is tolerant of DC failure with three quarters of semiconductors compared with involving FBSMs alone. Similarly, [51] proposes a mixed submodule based on HBSM and CDSM. It is suggested to achieve fast DC fault current clearing and capacitor uniform distribution at the cost of adding an extra diode between the submodules.

Figure 3h shows a cross-connected submodule (CCSM) [52] that consists of two HBSMs connected back to back via two IGBTs with anti-parallel diodes. The CCSM can output five symmetric voltage levels: $\pm(v_{c1} + v_{c2})$, $\pm v_{c1}/\pm v_{c2}$, and zero. This topology is tolerant of DC fault current by turning off crossed IGBTs S5 and S6. Crossed IGBTs conduct alternately during normal operation, which increases power losses.

The researchers proposed a new switched capacitor submodule (SCSM) [53][OBJ,OBJ], as shown in Figure 3i. It is composed of two capacitors and six IGBTs with anti-parallel diodes. The two capacitors are connected in series to output a voltage $2v_c$, whereas they are connected in parallel to output a voltage v_c, which enables SCSM to achieve voltage balancing with only half of the voltage sensors utilized in the other submodules. The SCSM is able to ride through a DC-link short circuit by turning off all the IGBTs.

A composite three-level submodule (CSM) was designed in [54] containing two capacitors, six power switches, and one diode, as presented in Figure 3j. The main feature of a CSM is that it offers alternative DC fault blocking solutions including all-blocked, partly blocked, or staged blocking. All IGBTs are set off in blocked mode to avoid over-current. In partly blocked mode, S3 and S5 are switched on to connect C1 and C2 in parallel, which balance the capacitor voltages effectively. Staged blocking is the combination of all-blocked and partly blocked. With DC fault blocking schemes, especially the latter two, a CSM is capable of addressing DC fault current together with capacitor unbalanced charging.

A comparative summary of the aforementioned submodule topologies is presented in Table 1 [25,55,56]. The comparison shows the performances of different submodule configurations associated with the number of sources and switching devices, output voltage levels, bipolar operation, DC fault blocking capability, power losses and cost, together with control complexity. The HBSM, due to its simple construction, has the lowest power losses and cost, which are related to the count of devices. However, it is not able to deal with bidirectional power flow and is sensitive to DC short failure. Other topologies, e.g., FBSM, CDSM, or HSM, have a bipolar operation and DC fault blocking capability at a price of increasing structural complexity. It is desired to carry out a submodule construction that is capable of bipolar operation, short circuit blocking, as well as symmetrical voltage levels at a minimum cost. The main challenge for the optimal submodule blocking topology is to make a tradeoff between the construction complexity and its performances.

Table 1. Comparison between different SM topologies.

Performance Index	HBSM	FBSM	SCSM	NPCSM	FCSM	CDSM	HSM	CCSM
No. of sources	1	1	1	2	2	2	2	2
No. of transistors	2	4	3	4	4	5	6	6
No. of diodes	2	4	4	6	4	7	6	6
Max. voltage	v_c	v_c	v_c	$2v_c$	$2v_c$	$2v_c$	$2v_c$	$2v_c$
Bipolar operation	No	Yes	Yes	No	No	Yes	Yes	Yes

DC fault blocking	No	Yes	Yes	No	No	Yes	Yes	Yes
Power losses	Low	High	Low	Moderate	Low	Moderate	Moderate	Moderate
Cost	Low	Moderate	Moderate	High	High	High	High	High
Control complexity	Low	Low	Low	High	High	Low	Low	High

2.2. Overall Topologies

In terms of MMC overall topologies, the phase-leg or arm structure is one of the research points to improve the performance of MMCs. The hybrid arm/leg architecture is a key factor to trade off the system cost, power losses, and DC fault blocking capacity. Hybrid MMCs usually contain two different submodules. A symmetric hybrid MMC in [57] is based on HBSMs and FBSMs. The single-phase structure is demonstrated in Figure 4a. Each arm is composed of an identical number of HBSMs and FBSMs. Likewise, an asymmetric hybrid MMC is discussed in [58], where HBSMs and FBSMs are separated in the upper and lower arms. Simulation and experimental results indicate that the asymmetric hybrid MMC is more advantageous to regulate DC bus voltage smoothly with well-controlled submodule capacitor voltages. Similarly to the former symmetric hybrid MMC, a hybrid MMC referred to as MCH-MMC is investigated in [59] and is composed of both HBSMs and CDSMs. The authors develop a repetitive predictive control strategy to suppress the circulating current and balance the submodule capacitor voltage for the proposed MCH-MMC.

A new family of MMC referred to as bifurcate MMCs is investigated in [60–62]. Figure 4b shows the single-phase circuit configuration including two single-bifurcate arms. Each arm consists of three branches, and two branches are connected to different phases of the AC port. The single-bifurcate arm can deduce the multi-bifurcate arm with a multi-layer of submodules. Control schemes are given for single- and multi-bifurcate structures. Theoretical analysis and simulation results indicate that bifurcate MMCs are suitable for low-modulation-ratio applications.

Du et al. propose a passive cross-connected MMC (PC-MMC) [10] and an active cross-connected MMC (AC-MMC) [11] whose single-phase configurations are shown in Figure 4c and 4d, respectively. The PC-MMC is also referred to as the flying-capacitor MMC. PC-MMC and AC-MMC have similar circuit configurations. The difference is that the flying capacitor in the PC-MMC is replaced by a series of additional submodules in the AC-MMC. Control strategies are also proposed by Du et al. in [10,11]. For the PC-MMC, the flying capacitor is capable of balancing power between upper and lower arms, suppressing voltage ripples on submodule capacitors at low/zero frequency operation. This is achieved by active controlled submodules in terms of AC-MMC. Both PC-MMC and AC-MMC are applicable in medium-voltage motor drive.
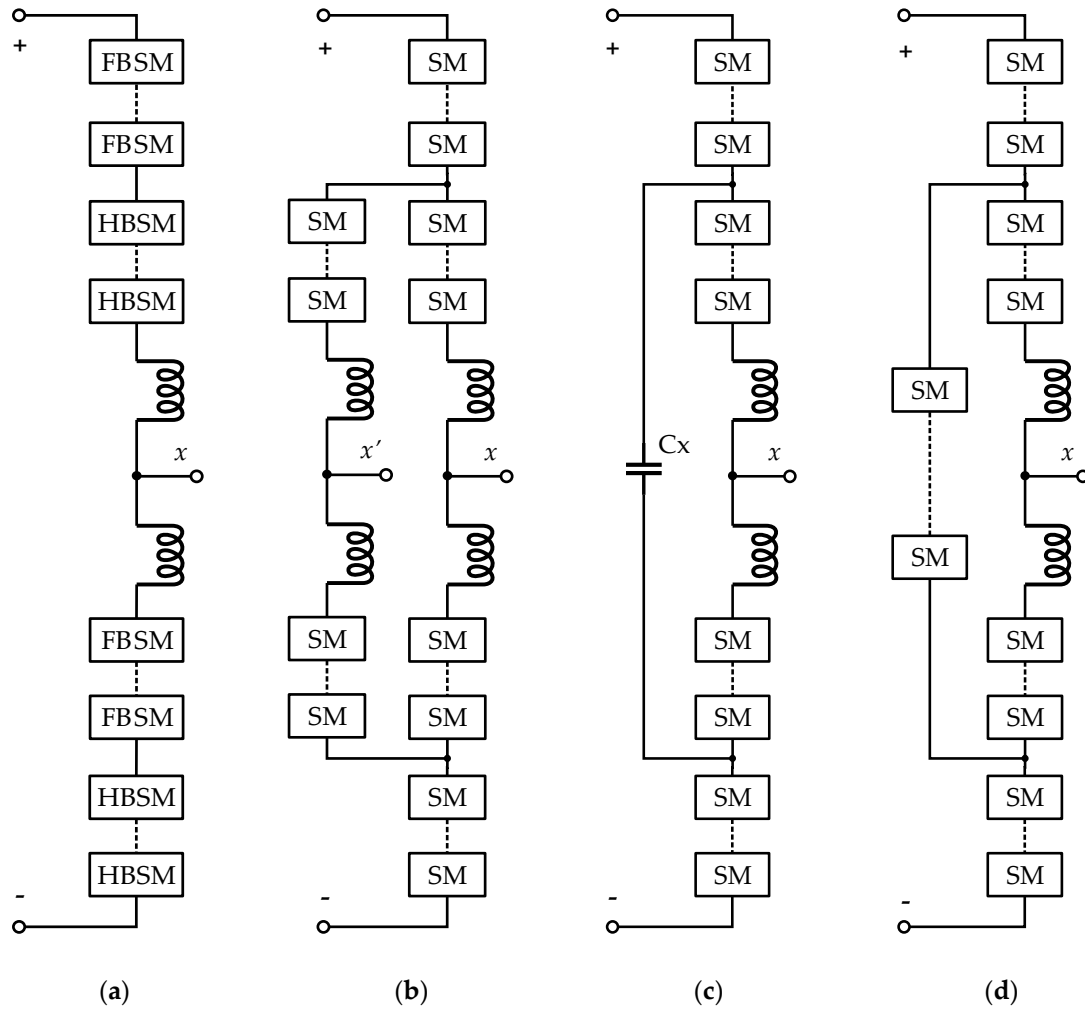
Figure 4. Overall single-phase configurations topologies: (**a**) Symmetric hybrid MMC; (**b**) Bifurcate MMC; (**c**) PC-MMC; (d) AC-MMC.

Apart from PC-MMC and AC-MMC, Du et al. also contribute to a star-channel MMC (SC-MMC) [63] and a delta-channel MMC (DC-MMC) [64] together with control schemes. Each arm of the SC-MMC and DC-MMC is divided into two parts, which are interconnected by additional submodules in either star or delta configuration. The upper and lower arms are usually composed of HBSMs for cost-saving and power efficiency matters, and the star-channel or delta-channel branches are realized by FBSMs to regulate the bidirectional current. Both SC-MMC and DC-MMC are capable of operating at zero/low-fundamental frequency with minimized submodule capacitor voltage ripples.

According to the connection schemes of the MMC arms, the overall architectures can be classified as star-configured MMCs and delta-configured MMCs [65,66]. These two types are classified as either chopper cells or bridge cells on account of the selection of submodules. They can be further split into single-star, single-delta, double-star, double-delta, and triple-star based on star and delta count. The configuration circuits are shown in Figure 5.
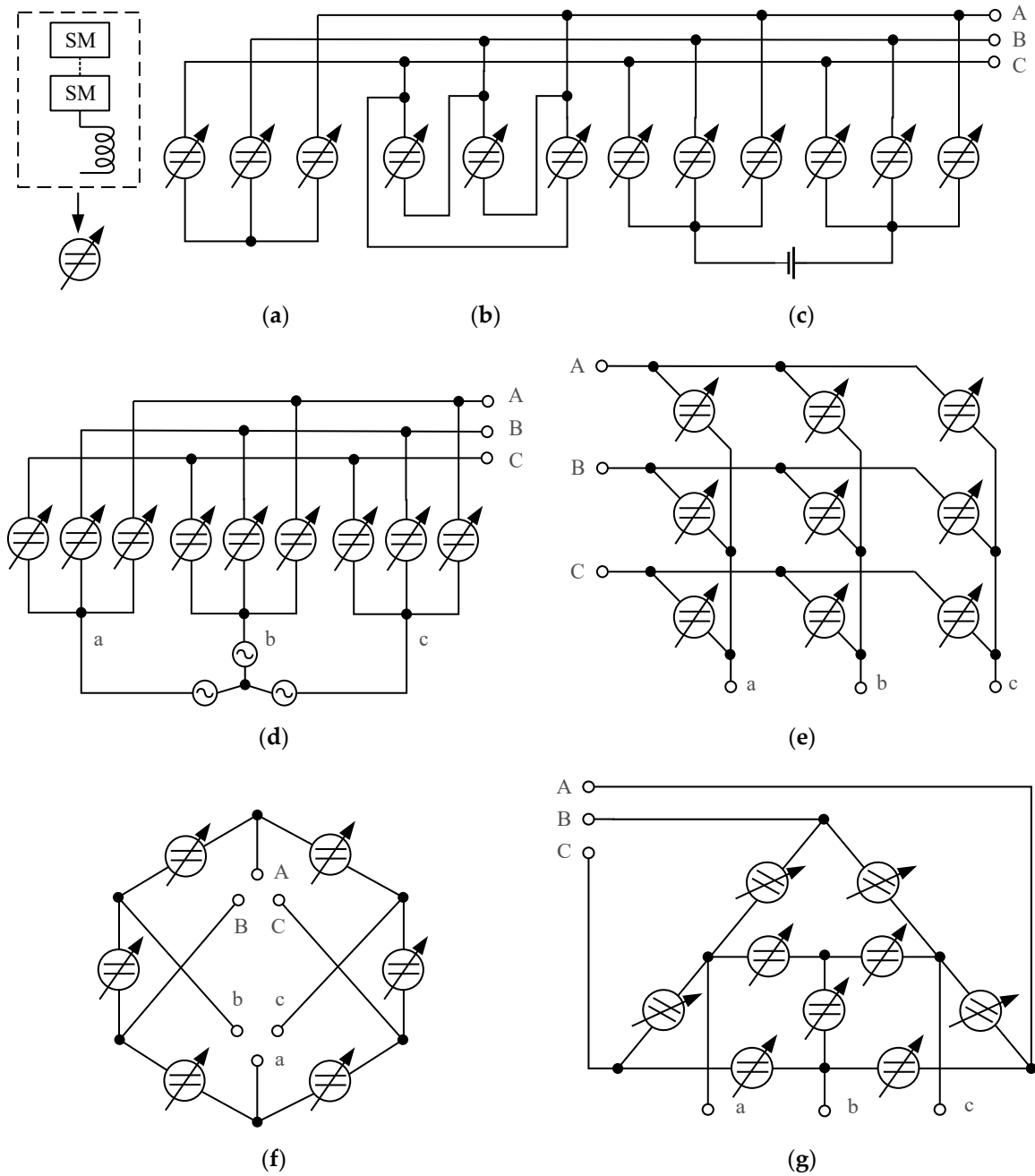
Figure 5. MMC arm configurations: (**a**) Single-star MMC; (**b**) Single-delta MMC; (**c**) Double-star MMC; (**d**) Triple-star MMC; (**e**) M3C; (**f**) Hexverter; (**g**) Hex-Y;.

Single-star and single-delta are the basic structures in the subfamily of star/delta-configured MMCs. They have three strings of submodules connected in either star or delta configuration. A single-star MMC is preferred in applications such as power compensators (STATCOM) and battery energy storage systems. Double-star and double-delta include two-star or delta-configured clusters connected by a DC source/load. They can realize the bidirectional current conversion of DC-AC or AC-DC. A double-star is widely used in MMC industries such as HVDC transmission and motor drive systems. A triple-star MMC [67] is comprised of three star-connected clusters, i.e., nine branches. It is well-known as a "modular multilevel matrix converter" (M3C) [68–70]. Figure 4d and Figure 4e are the two same presentations for triple-star MMC or M3C. It is capable of converting AC to AC directly between the bidirectional three-phase power system confronted with traditional AC-DC-AC indirect conversion, which is similar to back-to-back configuration [71] and involves two

three-phase MMCs including twelve branches. It has superior performance for the medium-voltage and high-power motor drive system with regenerative braking.

In recent years, researchers developed a new topology for MMC referred to hexagonal MMC or Hexverter [72]. The Hexverter consists of six arms connected in a hexagonal circuit, and each arm is alternatively connected to one phase of two three-phase AC networks, as shown in Figure 5f. This novel topology can achieve direct AC-AC conversion with a further reduced number of branches and components when compared with triple-star MMC or M3C. This converter is advantageous when applied in applications such as low-frequency wind turbines.

However, the Hexverter has limited reactive power provision capability at some operation points, together with injected common-mode voltage, which is not expected in some applications such as motor drives. Therefore, another hexagonal topology called Hex-Y [73,74] is proposed based on the Hexverter. Except for the retaining hexagon circuit, three star-connected branches are added within the hexagon, as shown in Figure 5g. A comparison for low-frequency mode was carried out between the Hex-Y and the M3C due to their identical number of branches. Simulation results indicate that the Hex-Y has a lower peak and RMS currents for low frequency below 5 Hz, and beyond 5 Hz, these turn to be higher than the M3C. The Hex-Y has flat torque-speed characteristics with low frequency. It is applicable for both fields which operate at low frequency and require full power capability in a wide frequency spectrum.

3. Mathematical Modeling and Control of Three-Phase MMC

3.1. Mathematical Modeling

Assuming that the arm and leg structures of three-phase MMC are perfectly symmetrical, the mathematical model [3,55,75–78] can be established based on a widely accepted equivalent circuit depicted in Figure 6.
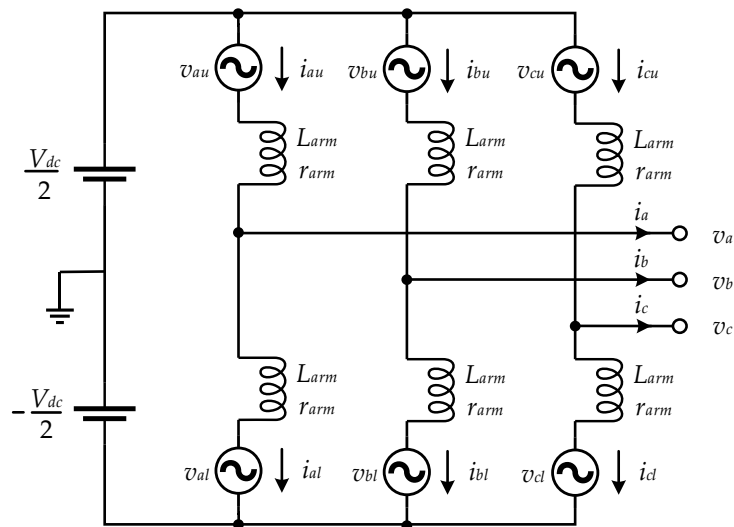

Figure 6. Equivalent circuit of three-phase MMC.

The equivalent AC electromotive force (EMF) is symmetrical in the upper and lower arm, resulting in equally distributed output AC current in the arms. The upper and lower currents can be expressed by

$$i_{xu} = \frac{i_x}{2} + i_{cirx} \tag{1}$$

$$i_{xl} = -\frac{i_x}{2} + i_{cirx} \tag{2}$$

where i_{xu} and i_{xl} represent the upper and lower currents of phase x $(x = a, b, c)$, i_{cirx} is the circulating current in each phase, and i_x represents the phase-x output AC current. From Equations (1) and (2), the output and circulating currents can be deduced as:

$$i_x = i_{xu} - i_{xl} \tag{3}$$

$$i_{cirx} = \frac{i_{xu} + i_{xl}}{2} \tag{4}$$

The circulating current contains DC and harmonic components. Due to the three-phase symmetrical structure, the equivalent DC EMF is equal for each leg, leading to an evenly distributed direct current in each phase. Thus, the DC component of the circulating current can be expressed by

$$i_{cirxu\_dc} = i_{cirxl\_dc} = i_{cirx\_dc} = \frac{i_{dc}}{3} \tag{5}$$

where i_{cirxu_dc}, i_{cirxl_dc}, and i_{cirxu_dc} are the DC components of cirrulating currents in the upper/lower arm and phase-x. The DC component of circulating currents is naturally eliminated when the DC link voltage is not practically employed such as operating in the motor drive mode in the battery-based MMC. In this case, the circulating currents consist of only harmonic components.

According to Kirchoff's voltage law, the upper and lower voltages can be given by

$$v_{xu} = \frac{V_{dc}}{2} - v_x - L_{arm} \frac{di_{xu}}{dt} - r_{arm} i_{xu} \tag{6}$$

$$v_{xl} = \frac{V_{dc}}{2} + v_x - L_{arm} \frac{di_{xl}}{dt} - r_{arm} i_{xl} \tag{7}$$

where v_{xu} and v_{xl} are the upper and lower voltages of phase x, v_x is the output voltage, L_{arm} and r_{arm} give the inductance and resistance of the arm inductor, and V_{DC} is the DC-link voltage. By separately adding and subtracting Equations (6) and (7), and using the relationship in Equations (1) and (2), the outer and inner dynamic equations of MMC can be expressed as

$$\frac{L_{arm}}{2} \frac{di_x}{dt} = -\frac{r_{arm}}{2} i_x + \frac{v_{xl} - v_{xu}}{2} \tag{8}$$

$$L_{arm} \frac{di_{cirx}}{dt} = -r_{arm} i_{cirx} - \frac{r_{arm}}{3} i_{dc} + \frac{V_{dc}}{2} - \frac{v_{xu} + v_{xl}}{2} \tag{9}$$

According to Equations (8) and (9), the output current i_x can be regulated by adjusting the voltage difference between the upper arm and the lower arm, and the circulating current i_{cirx} can be controlled by changing the sum of the upper arm and the lower arm voltages. These two driving voltages of the output current and circulating current can be defined as

$$v_x = \frac{v_{xl} - v_{xu}}{2} \tag{10}$$

$$v_{cirx} = \frac{V_{dc} - v_{xu} - v_{xl}}{2} \tag{11}$$

In addition, the dynamic equations of the submodule capacitor voltages are given by

$$C_{SM} \frac{dv_{SMuk}}{dt} = i_{xu} S_{SMuk} \tag{12}$$

$$C_{SM} \frac{dv_{SMlk}}{dt} = i_{xl} S_{SMlk} \tag{13}$$

where C_{SM} is the capacitor capacitance, v_{SMuk} and v_{SMlk} are the submodule voltages in the upper and lower arms, and S_{SMuk} and S_{SMlk} represent the submodule gating signals, respectively. When S_{SMk}=1, the submodule is inserted, and the charging or discharging is realized according to the direction of current. When S_{SMk}=0, the submodule is bypassed, and the capacitor voltage remains the same.

Equations (8), (9), (12), and (13) provide a generalized dynamic model of the MMC. The specific dynamic modeling principle can be based on the perspective of either voltage-based control or energy-based control [79]. When the submodule capacitors are substituted by batteries as the energy source, the state of charge (SoC) management turns to the key factor correspondingly [80,81]. Researchers have contributed a range of approaches for SoC estimation, where the most popular SoC tracking method is the Coulomb counting method [82] given by:

$$SoC(t) = SoC(0) - \frac{\int_0^t i(t)dt}{3600Q_{max}} \times 100\% \tag{14}$$

where Q_{max} is the battery maximum capacity. The relationships between battery current, capacity, and SoC are given by [18, 80,83]

$$i_{uxk} = Q_{max} \frac{dSoC_{uxk}}{dt} \tag{15}$$

$$i_{lxk} = Q_{max} \frac{dSoC_{lxk}}{dt} \tag{16}$$

where i_{uxk} and i_{lxk} are the battery current, and SoC_{xk} and SoC_{lk} donate individual SoC at the upper and lower arm. The average SoC of each phase arm is defined as

$$\overline{SoC}_{ux} = \frac{1}{N} \sum_{k=1}^{N} SoC_{xk} \tag{17}$$

$$\overline{SoC}_{lx} = \frac{1}{N} \sum_{k=1}^{N} SoC_{lk} \tag{18}$$

where $\overline{SoC}_{ux}$ and $\overline{SoC}_{lx}$ represent the average SoC of the upper arm and lower arm. Assuming the switching losses are neglected, the input and output power at the AC side and DC side of the submodule are equal.

$$P_{uxk} = V_{bat} i_{uxk} = v_{uxk} i_{ux} \tag{19}$$

$$P_{lxk} = V_{bat} i_{lxk} = v_{lxk} i_{lx} \tag{20}$$

where P_{uxk} and P_{Lxk} represent the individual power in the upper and lower arm, and V_{bat} is the battery voltage. The arm power is the sum of total submodules given by

$$P_{ux} = i_{ux} \sum_{k=1}^{N} v_{uxk} = (Q_{max} \sum_{k=1}^{N} \frac{dSoC_{uxk}}{dt}) V_{bat} \tag{21}$$

$$P_{lx} = i_{lx} \sum_{k=1}^{N} v_{lxk} = (Q_{max} \sum_{k=1}^{N} \frac{dSoC_{lxk}}{dt}) V_{bat} \tag{22}$$

where P_{ux} and P_{Lx} represent the upper and lower arm power. According to Equations (17) and (18) and using the representation in Equations (21) and (22), the sum and difference of arm power (P^Σ and P^Δ) are yielded,

$$P^\Sigma = P_{ux} + P_{ux} = NV_{bat}Q_{max}\frac{d(\overline{SoC}_{ux} + \overline{SoC}_{lx})}{dt} = -v_x i_x + NV_{bat}i_{cirx} - L_{arm}(i_{ux}\frac{di_{ux}}{dt} + i_{lx}\frac{di_{lx}}{dt}) \quad (23)$$

$$P^\Delta = P_{ux} - P_{ux} = NV_{bat}Q_{max}\frac{d(\overline{SoC}_{ux} - \overline{SoC}_{lx})}{dt} = -\frac{N}{2}V_{bat}i_x - 2v_x i_{cirx} - L_{arm}\frac{di_x i_{cirx}}{dt} \quad (24)$$

Neglecting the alternating term, the upper equation can be simplified as [83]:

$$NV_{bat}\frac{d(\overline{SoC}_{ux} + \overline{SoC}_{lx})}{dt} \cong NV_{bat}I_{cirx\_dc} - \frac{1}{2}V_x I_x \cos\varphi \quad (25)$$

$$NV_{bat}\frac{d(\overline{SoC}_{ux} - \overline{SoC}_{lx})}{dt} \cong -V_x I_{cirx\_1}\cos\varphi_1 \quad (26)$$

From Equations (25) and (26), the leg SoC balancing can be realized by controlling the DC component of the circulating currents; the arm SoC balancing can be achieved by regulating the fundamental component of circulating currents.

3.2. Output Voltage and Current Control

The MMC control strategies enable its high performance associated with superior safety, reliability, and efficiency. The control is challenging and sophisticated as involving substantial submodules and multiple control objectives related to the output voltage and current control, submodule voltage or SoC balancing control, and circulating current control. The MMC AC terminal can be connected to a renewable energy system, e.g., a wind turbine farm, or a high-voltage transport grid or medium-voltage distribution grid. Assuming the MMC is connected to the grid, as shown in Figure 7, the control of its output voltage and current vary under different grid conditions such as a balanced grid, unbalanced grid, and distorted grid [4].
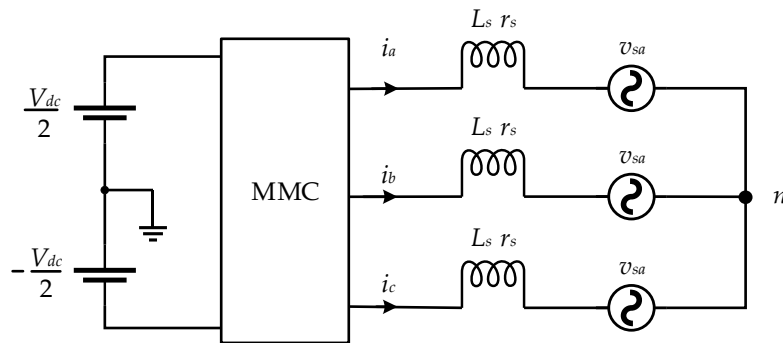
Figure 7. Grid-connected MMC.

In most cases, the AC side is assumed to interface a balanced utility only involving a fundamental component. The MMC output voltage and current control can be achieved by using the outer voltage control and inner current control. The inner current control is required to satisfy the command of active and reactive power based on the instantaneous power theory coordinated in a reference frame [84,85]. Generally, in the synchronous rotating *dq*-frame, assuming the *d* axis is completely aligned with the rotating vector of source voltage, the active power and reactive power can be expressed by

$$P = \frac{3}{2} v_{sd} i_d \tag{27}$$

$$Q = -\frac{3}{2} v_{sq} i_q \tag{28}$$

where P and Q are the active and reactive power, respectively, v_{sd} and v_{sq} represent the d component and q component of the source voltage, and i_d and i_q give the reference currents i_d^* and i_q^* in dq axes. Using Equations (27) and (28), the active and reactive power can be managed by regulating i_d and i_q independently. The output voltage in dq-axes can be expressed as

$$v_d = v_{sd} + L_s \frac{di_d}{dt} + r_s i_d - \omega L_s i_q \tag{29}$$

$$v_q = v_{sq} + L_s \frac{di_q}{dt} + r_s i_q + \omega L_s i_d \tag{30}$$

where v_d and v_q represent the d and q components of the MMC AC-side voltage, L_s and r_s donate the inductance and resistance at the grid side, and ω is the fundamental angular frequency.

In addition, the DC-link voltage should maintain at the setpoint, which can be realized by the power balance between the AC terminal and DC terminal.

$$P = \frac{3}{2} v_{sd} i_d = V_{dc} i_{dc} \tag{31}$$

From Equation (31), the DC voltage can be used to produce the reference current in the d component. Therefore, the control block of the output voltage and current is demonstrated in Figure 8.
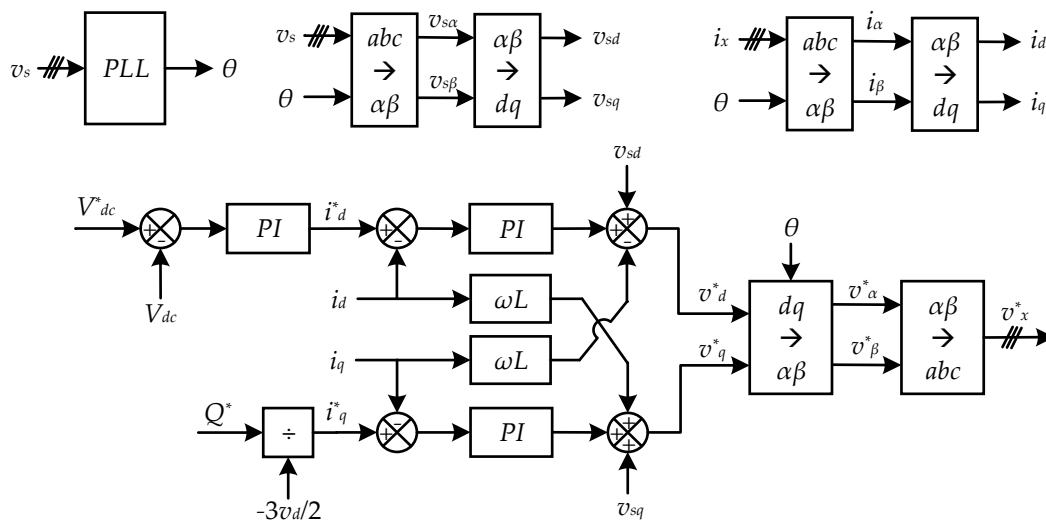

Figure 8. Output voltage and current control under balanced grid condition.

When unbalanced loads are connected or main failures occur in the grid, the grid voltage is unbalanced, resulting in an invalid injection of active power and limited restoration of reactive power. The output voltage and current must be controlled with independent control loops regarding positive and negative sequence grid components. A method is referred to as Delayed Signal Cancellation (DSC) [86]; it facilitates the calculation of the positive and negative sequence components. The control scheme of the output voltage and current control under unbalance grid conditions is depicted in Figure 9 [87]. The positive and negative sequence currents in d components are regulated with the effect of active power, and the command values are set to zero, as the active power ought to be zero. The positive and negative sequence voltages are controlled in the manner of reactive power by using PI controllers. The voltage references for positive and negative sequence are set to the grid voltage nominal value and zero, respectively.
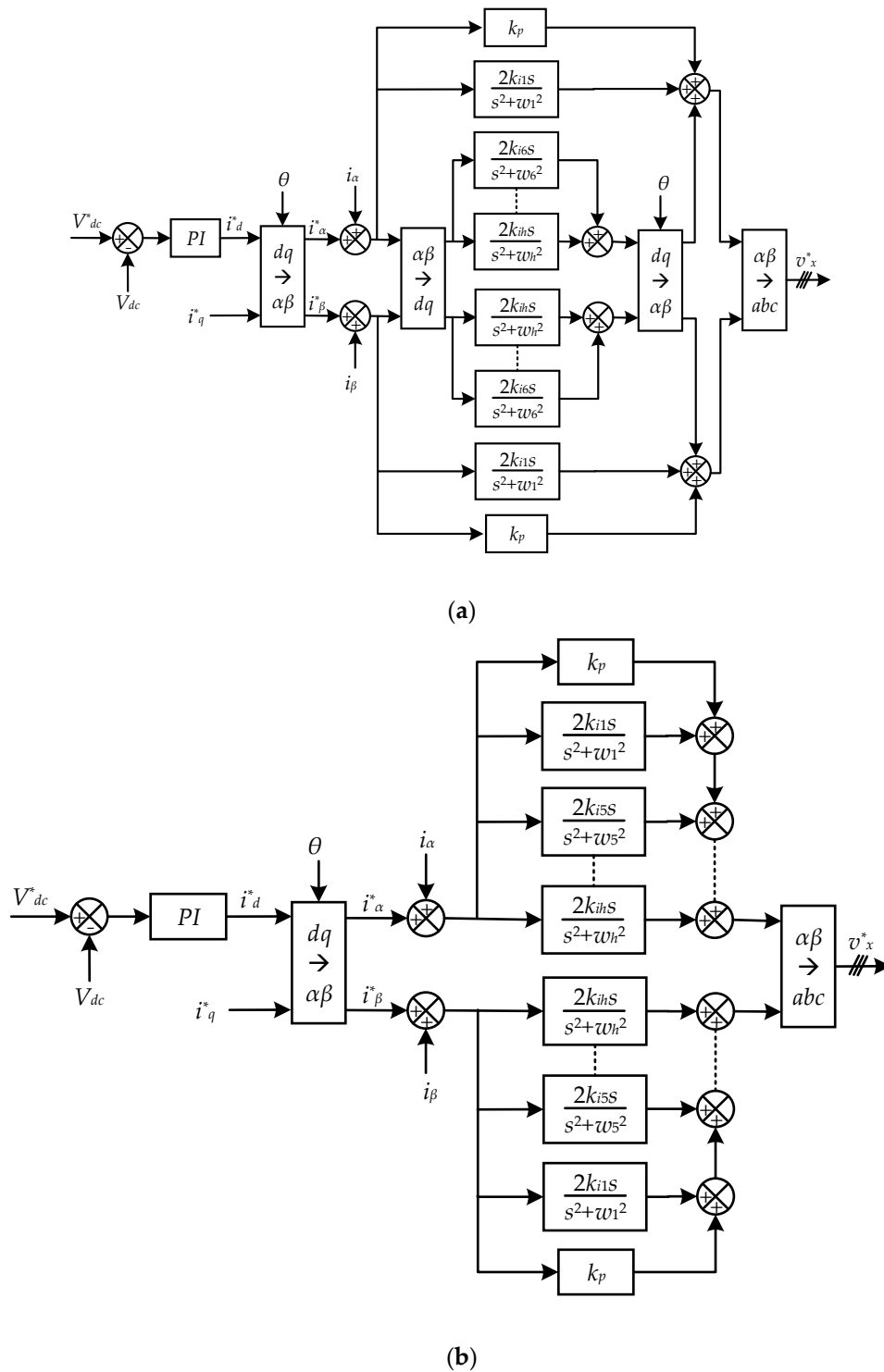
Distorted grid is another abnormal condition of the grid system in which the grid voltage involves fundamental component and multiple harmonics. These harmonics cause voltage distortion, additional power losses in converters, and the malfunction of sensitive electronic devices. Therefore, it is necessary to apply a control method to eliminate multiple harmonics for the distorted grid. The harmonic components are normally at $(6n \pm 1)\omega_1$, n = 1,2,3,..., in the three-phase system where the even-order and triple-order harmonics are naturally eliminated. The sequence of $(6n - 1)\omega_1$ harmonics are consistent with the sequence of a fundament component (positive/negative), whereas $(6n + 1)\omega_1$ harmonics are opposite to the fundamental sequence (negative/positive) [88].

Figure 9. Output voltage and current control under unbalanced grid condition.

It is argued that the PI controller is not suitable for harmonics elimination in the distorted grid due to its limited performance when dealing with sinusoidal reference signals and periodic disturbances [89]. The preferred control schemes [90] are based on selective harmonic compensation by using proportional resonant (PR) controllers or nonlinear and predictive approaches and repetitive control. Among them, the PR controller is widely used to eradicate the harmonics in the specific order. Figure 10 illustrates two control approaches based on PR controllers in the $\alpha\beta$ and *dq*-frame [91] and $\alpha\beta$ frame under distorted grid condition [92].

(**a**)

(**b**)

Figure 10. Output voltage and current control under distorted grid condition: (**a**) in $\alpha\beta$-dq frame; (**b**) in $\alpha\beta$ frame.

3.3. Submodule Balancing Control

The submodule balancing control in the MMC mainly involves leg/arm voltage balancing control, submodule capacitor voltage balancing control, or SoC balancing control if based on a battery submodule. Various submodule balancing schemes have been discussed and presented in the literature. These approaches are mainly based on individual voltage/SoC control or a sorting algorithm to equilibrate between submodules. Generally, when a small number of submodules are explored in the converter, the individual voltage/SoC control can be applied to realize the individual voltage/SoC regulation; otherwise, the sorting algorithm is preferred in the application with

increased submodules by selecting the inserted/bypassed submodules in order of priority [4]. The individual balancing control and sorting control are also well-known as distributed balancing control and centralized balancing control [5,93].

Due to the inconsistency of actual submodule parameters and the charging and discharging influence, the submodule capacitor voltage is likely to deviate from the setpoint. In addition, the frequent switching states also contribute to the capacitor voltage ripple. The inconsistent submodule capacitor voltage results in unequal arm and leg voltage, which will further lead to a circulating current increasing the power losses and worsening the submodule voltage balancing [3,75]. The individual submodule balancing can be achieved by using a closed-loop controller for each cell [94,95]. The leg voltage balancing can be achieved by involving PI controllers as depicted in Figure 11a. The average submodule voltage is compared with the setpoint and manipulated by a PI controller outputting the DC component of circulating currents reference. The actual DC component of circulating currents can be obtained through a low-pass filter (LPF) or by averaging the upper arm and lower arm current. The individual voltage balancing algorithm regulates each submodule voltage with a PI controller separately (Figure 11b), and thus, the value of the individual control signal is relatively small. The signed block donates the direction of the current.
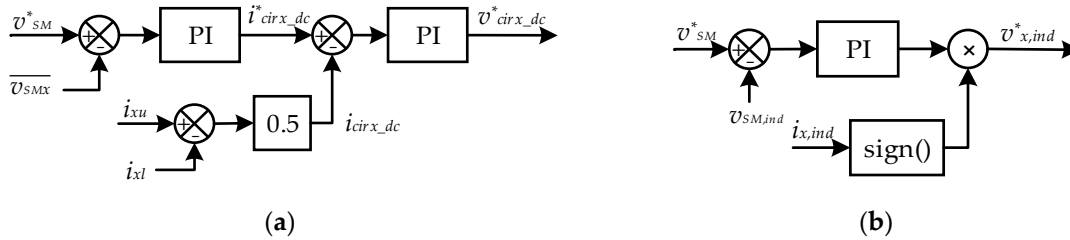

Figure 11. Voltage balancing control: (**a**) Leg voltage balancing; (**b**) Individual voltage balancing.

The submodule balancing control can be realized by using either the above-mentioned methods referred to as voltage-based control or the approaches involving energy-based control [79]. When the submodule capacitors are substituted by batteries as the energy source, the control objective changes to SoC balancing control, correspondingly. SoC balancing control involves SoC balancing between legs, arms, and individuals [80,81]. The control algorithm of SoC balancing resembles that of capacitor voltage control except for the SoC calculation. The arm SoC balancing control is realized by controlling the fundamental component of circulating currents shown in Figure 12b. The average SoCs of the upper and lower arms are compared and regulated by a PI controller yielding the amplitude of the fundamental component. The fundamental component is in-step phase with the reference and controlled by a proportional resonant (PR) controller to generate the arm SoC balancing control signal. On the basis of leg SoC and arm SoC balancing, a further individual SoC balancing control is conducted on each submodule battery, as demonstrated in Figure 12c.
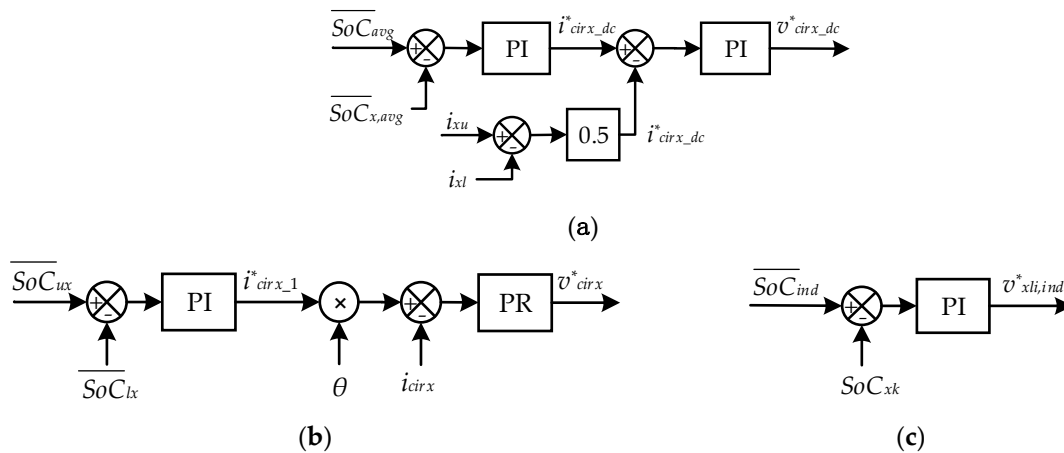

Figure 12. SoC balancing control: (**a**) Leg SoC balancing control; (**b**) Arm SoC balancing control; (**c**) Individual SoC balancing control.
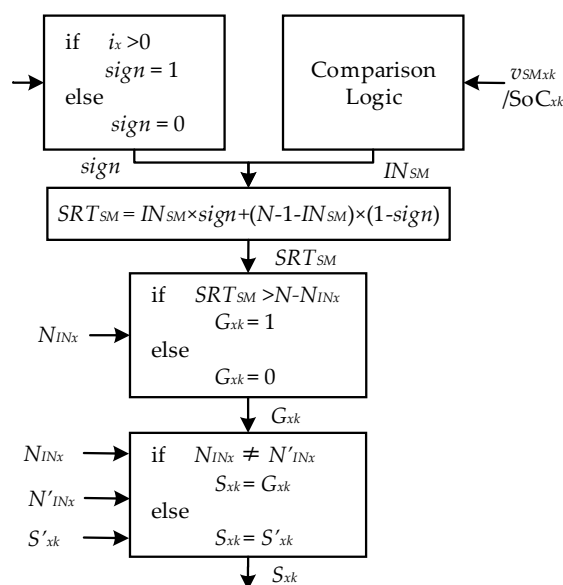
if　　i_x >0
　　　$sign$ = 1
else
　　　$sign$ = 0

Comparison
Logic

v_{SMxk}
/SoC$_{xk}$

$sign$　　　　　　　　　　　　　　IN_{SM}

$SRT_{SM} = IN_{SM} \times sign + (N-1-IN_{SM}) \times (1-sign)$

SRT_{SM}

N_{INx} →

if　　SRT_{SM} >N-N_{INx}
　　　G_{xk} = 1
else
　　　G_{xk} = 0

G_{xk}

N_{INx} →
N'_{INx} →
S'_{xk} →

if　　N_{INx} ≠ N'_{INx}
　　　S_{xk} = G_{xk}
else
　　　S_{xk} = S'_{xk}

S_{xk}

Figure 13. Flow chart of sorting balancing control.

Apart from employing PI controllers to realize the voltage balancing control or SoC balancing control, another widely used method refers to sorting balancing control [75,77], as illustrated in Figure 13. In the first step, the instantaneous value of the submodule capacitor voltage/battery SoC is measured, and the current direction is defined. According to the actual value, the submodule capacitor voltage/battery SoC is compared in a logic comparator to acquire an index number and further arranged in ascending or descending order depending on the current direction. Then, the final index number is compared with the reference index number, and submodules with the lowest voltages/SoC are selected and inserted if the current direction is positive and vice versa. The switching signal remains constant if it remains the same as in the previous cycle. Generally, the submodule balancing control using PI regulators produces a reference signal forming the modulation index and is arranged before PWM schemes, while the sorting balancing control is set after PWM methods to generate the final switching pulse.

3.4. Circulating Current Control

The voltage difference between the upper and lower arms of the MMC legs results in the circulating current. The circulating current has little influence on the output voltages and currents at the AC side. However, it distorts the arm current, leading to extra power losses, a higher rating of devices, and submodule voltage ripples [96]. Therefore, the circulating current is expected to be eliminated. The arm inductors can suppress the circulating current to some extent [97]. Furthermore, the elimination controller is required to be employed. Since the circulating current is dominated by even-order harmonic components, especially second-order harmonics, the control objective of the elimination controller mainly focuses on the elimination of second-order harmonics [98]. The circulating current elimination approaches are based on decoupling control in the rotating *dq*-frame or resonant control in the stationary *abc*-frame. In terms of decoupling control, the second-order circulating current is converted into a *d*-axis and *q*-axis as DC components, which can be controlled easily and independently by PI regulators, as shown in Figure 14a [99,100]. In the case of unbalanced conditions where the circulating currents have positive, negative, and zero sequence components, the repetitive controller [101,102] can be applied to regulate multiple circulating current harmonics. Compared to decoupling methods, the proportional resonant controller has some advantages under unbalanced conditions with an easier implementation of multiple resonant controllers to eliminate a wider bandwidth of circulating current harmonics [103,104]. The resonant control structure to eliminate second-order, fourth-order, and sixth-order harmonics is described in Figure 14b [92,104]. In addition, for the sake of control robustness, the improved quasi proportional resonant controller

is adopted to eliminate the circulating current, as shown in Figure 14c [105,106]. Except for eliminating the circulating current, the circulating current injection method is developed to reduce the submodule voltage ripple. Circulating current injection can be realized by the lookup table method [107] or the online calculation method based on instantaneous data [108].
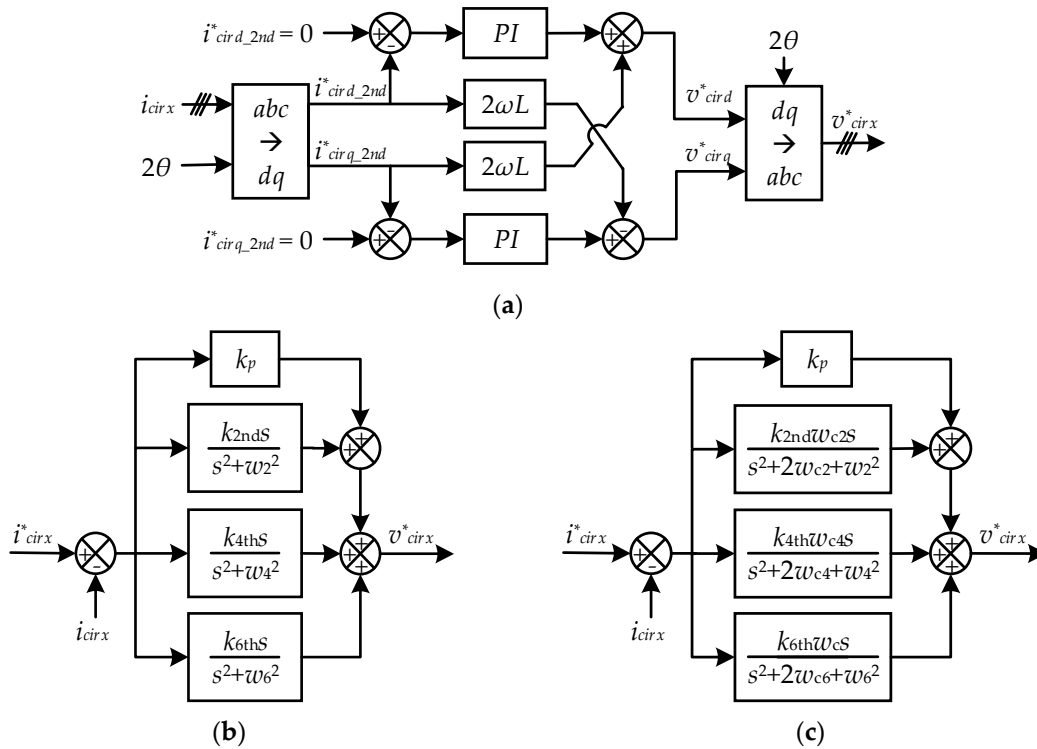

(a)

(b)

(c)

Figure 14. Circulating current control: (**a**) Decoupling control in the *dq*-frame; (**b**) Proportional resonant control; (**c**) Quasi proportional resonant control.

3.5. Nonlinear and Predictive control

The MMC as a switching converter is a nonlinear system associated with multiple coupled variables. The conventional control methods are easy to implement in digital controllers by using linear techniques. However, these methods have a limitation on the dynamic response in terms of multiple control objectives such as AC current and voltage, leg/arm voltage, and circulating currents. To achieve simultaneous control and dynamic response, nonlinear and predictive control strategies are promising alternatives for MMC applications.

A nonlinear decoupling control based on feedback linearization [109] is proposed for MMC converters with the remaining linearized variables and linear controller to achieve desired transient responses and stability. Another nonlinear control method based on sliding mode control [110] is investigated with the faster dynamic response by splitting the state space into several subspaces, which are further controlled in an individual control structure. Passivity-based control [111,112], belonging to the nonlinear control strategies is applied to the MMC system based on an energy function to acquire a better dynamic and steady-state performance. The passivity-based control and sliding mode control are further combined in the MMC control system to improve the transient performance and robustness to system changes [113]. A nonlinear back-stepping control scheme [114], based on energy equations, is explored for single- and three-phase MMC by using Lyapunov theory with a simplified control structure in the *abc* frame. The back-stepping method is armed with the inherent feature of circulating current suppression and validated in simulation and experiments showing good dynamic response and robustness.

Predictive control, often referred to as model predictive control (MPC), is a preferable choice for power converters as it is a nonlinear control method. The MPC method can deal with multiple constraints in a single cost function and provide fast dynamic response and robustness against

parameter variation and external disturbance. The finite control set MPC (FCS-MPC), also known as direct MPC, is a popular predictive approach used in MMC control. The implementation of FCS-MPC requires a discrete-time model of the MMC system which can be obtained from the discretization of the continuous-time model. The conversion from continuous-time to discrete-time can be achieved by using the forward Euler approximation or backward Euler approximation. A flow chart of the FCS-MPC [115] is depicted in Figure 15. One disadvantage of the FSC-MPC is the computational burden to obtain the optimal switching states, which worsens with increasing voltage levels. To deal with this issue, a fast FCS control scheme is investigated. Fast FCS-MPC [116], also known as indirect MPC, remains the submodule balancing strategy along with the predictive control. The predictive control is employed as the primary controller to control the output and circulating currents. Meanwhile, the submodule balancing strategy is applied as the secondary controller to equalize the submodule voltages or SoCs within the arm. The computational effort of the indirect FCS-MPC is minimized to a large extent, as only N+1 switching states are required to be evaluated for the optimal cost function.
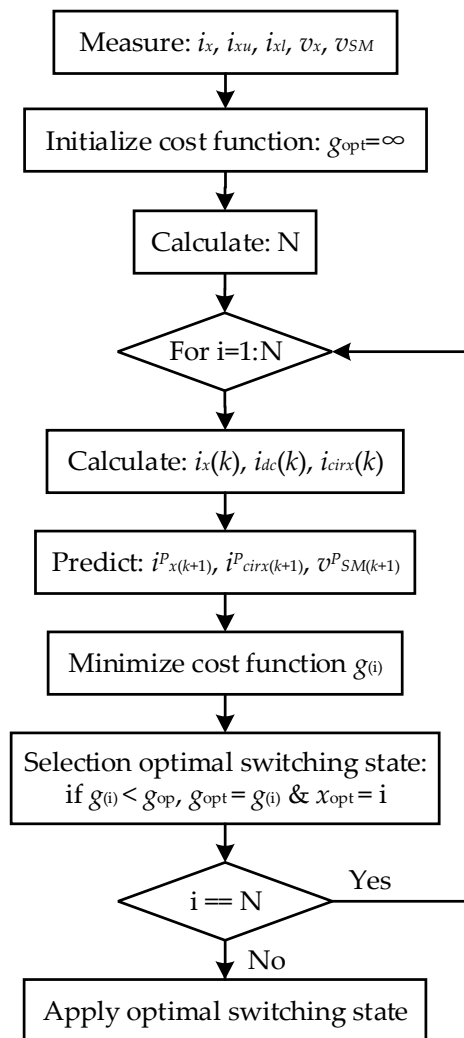

Figure 15. Flowchart of finite control set model predictive control.

4. MMC Modulation Techniques

Various pulse width modulation (PWM) techniques have been developed to generate a desired output voltage for the MMC. These modulation techniques, depending on the switching frequency, can be classified as high switching frequency PWM (HSF-PWM), low switching frequency (LSF-PWM), and fundamental switching frequency (FSF-PWM) modulation scenarios [3,5]. The

semiconductor switching losses increase with the switching frequency. As a result, the high switching frequency method is generally utilized when a small number of submodules are employed, whereas low switching frequency and fundamental switching frequency schemes are preferred when substantial submodules are involved [4].
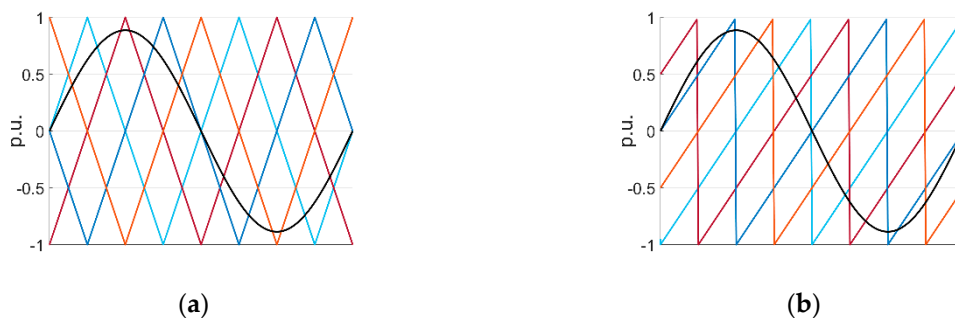
Carrier-based PWM is a typical HSF-PWM method in which, for multilevel converters, the modulation reference of each phase is compared with multiple carrier waveforms to create the gating signals [34]. Triangular or sawtooth waveforms are prevalently applied as the compared carrier signals. The reference signals are produced by involving application-oriented control strategies, for example, voltage-oriented control (VOC) and field-oriented control (FOC), and they can be given as [77]

$$v_x = m \times \frac{V_{dc}}{2} \sin(\omega t + \varphi_x) \tag{32}$$

where v_x is the phase modulation reference, m is the amplitude of modulation index in the range [0, 1], ω is the fundamental angular frequency, and φ_x is the phase angle of {0, $2\pi/3$, $4\pi/3$}.

Carrier-based modulation schemes, based on the arrangement of multiple carriers, are categorically divided as phase-shifted carrier-based (PSC-PWM) and level-shifted carrier-based (LSC-PWM) techniques [117], as seen in Figure 15. In PSC-PWM, N identical triangular carrier waveforms are employed and displaced horizontally with a phase shift $2\pi/N$. By comparing the modulation signals with the N carrier signals, the MMC can produce an output voltage with $N+1$ levels. The carrier waveforms in the upper and lower arm can be arranged with an interval angle π/N, with which the power converter can generate ($2N+1$)-level output voltage [43,118]. The latter approach reduces the harmonic distortion of the output voltage with approximately double voltage levels at the cost of additional computation burden. Thanks to the independent modulation signal for each submodule, the PSC-PWM method imposes equal-distributed power stresses and switching losses on the semiconductors and contributes to the submodule capacitor voltage balancing [119]. The PSC-PWM approach is widely used in the multilevel power conversion system.

Using LSC-PWM, it produces ($N+1$)-level output voltage at the AC side involving N carrier signals with uniform magnitude and frequency disposed sequentially in line with zero axis [120,121]. The LSC-PWM strategy has three subfamily members including phase-disposition (PD-PWM), phase-opposition-disposition (POD-PWM), together with alternate phase-opposition-disposition (APOD-PWM). The different modulation techniques are illustrated in Figure 16. Although the LSC-PWM approach can be easily implemented to produce multilevel voltage, it is less preferred in the MMC application, since it causes uneven voltage distribution across the submodule capacitors, which results in a higher harmonic distortion of output voltage and leads to an increase of circulating currents. To overcome this situation, a series of rotation techniques regarding carrier or reference signals, e.g., a carrier rotation technique [122], a modified carrier rotation technique [123], or a signal rotation technique [120], are proposed to equally arrange submodule capacitor voltage. Furthermore, the optimized PD-PWM are developed with a selective loop bias mapping technique [124] or interleaving angle method [125] to reduce total harmonic distortion and balance submodule capacitor voltage naturally.
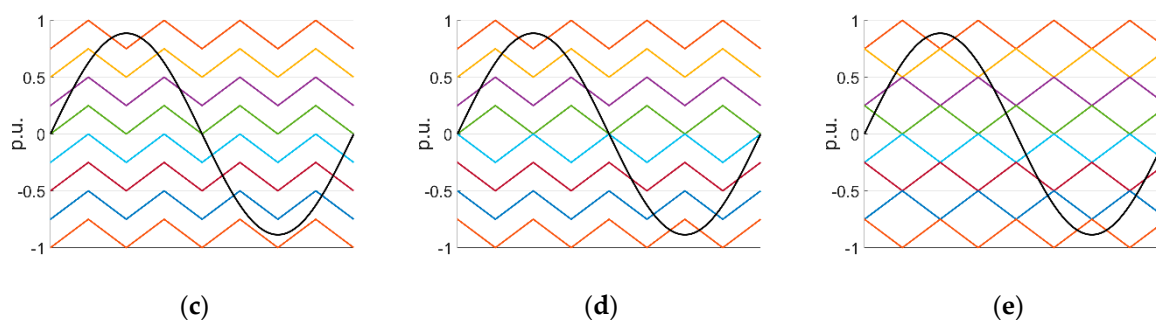
(**a**)

(**b**)

Figure 16. High switching frequency pulse width modulation (PWM) techniques: (**a**) phase-shifted carrier-based pulse width modulation (PSC-PWM) with triangular carriers; (**b**) PSC-PWM with sawtooth carriers; (**c**) phase-disposition pulse width modulation (PD-PWM); (**d**) phase-opposition-disposition pulse width modulation (POD-PWM); (**e**) POD-PWM.

The switching frequency of space vector modulation (SVM) falls into the category of the LSF-PWM scheme. It is advantageous to select the switching vectors and arrange the switching sequences with more freedom in SVM-PWM. SVM-PWM has demonstrated good performance with superior harmonic features and DC-link utilization in the two-level converter [126]. However, when it comes to multilevel modulation, the SVM-PWM algorithm is challenging to implement with the significantly increased computational burden and complexity [1]. For the case of N levels, the figures of switching vectors and triangles soar to N^3 and $6(N-1)^2$, respectively [3]. To simplify multilevel SVM-PWM applied in the MMC, an improved scheme is proposed by decomposing the multilevel space vector into several two-level space vectors [127]. This method can easily be extended to multilevel converters with a reduced computational cost. Another low switching frequency modulation approach referred to sampled average modulation (SAM) has a similar process to SVM-PWM but with less computation complexity and simple implementation to multilevel converters with any number of submodules [128]. In SAM-PWM, the command voltage is produced by averaging the two nearest voltage levels and avoiding zero vectors in each sampling interval.

In terms of fundamental switching frequency modulation, a quite popular method is nearest level modulation (NLM) [129,130]. In this approach, the switching states and dwell time are directly derived from the command voltage eliminating the use of carrier signals. It is easy and practical to implement, especially in the case of MMC involving a large number of submodules. Selective harmonic elimination (SHE) also belongs to the category of FSF-PWM. SHE-PWM [131] can provide a high performance of output voltages. However, this method is difficult to implement due to the heavy calculation of substantial switching angles with multilevel voltages. An overview and comparison of different modulation techniques regarding modulation categories, switching frequency, application with the employed number of submodules, output harmonic performance, and implementation effort are presented in Table 2.

Table 2. Pulse width modulation techniques.

PWM	Category	Switching frequency	SM count	Performance	Effort
PSC-PWM	HSF-PWM	$f_{sw} > 2000$ Hz	Small/Large	High	Complex
LSC-PWM	HSF-PWM	$f_{sw} > 2000$ Hz	Small/Large	Moderate	Moderate
SVM-PWM	LSF-PWM	100 Hz $< f_{sw} < 2000$ Hz	Small	High	Complex
SAM-PWM	LSF-PWM	100 Hz $< f_{sw} < 2000$ Hz	Small/Large	Moderate	Easy
NLM-PWM	LSF-PWM	$f_{sw} = 50/60$ Hz	Large	Low	Easy
SHE-PWM	LSF-PWM	$f_{sw} = 50/60$ Hz	Small	High	Complex

5. Power Losses and WBG Technology

Wideband gap (WBG) semiconductors, made on silicon carbide (SiC) and gallium nitride (GaN) provide advantages of increased energy efficiency, high power density, and cooling density thanks

to improved electrical and thermal conductivities [132,133]. WBG transistors are expected to occupy a wide range of power conversion applications which are dominated by the traditional Si-based power devices over the past decades. Figure 17 [134,135] accounts for the competitive advantages for WBG power modules over classical Si-based switches in the condition of high voltage, high frequency, and high-temperature operation. For low-voltage applications, GaN power modules, where all the electrodes are arranged on the top layer due to the lateral structure, are preferred as a result of significantly reduced on-state resistance with high switching frequency. In contrast, SiC switches are much more competitive for higher voltage applications because of the easily scalable voltage and current with a vertical conduction path [136].
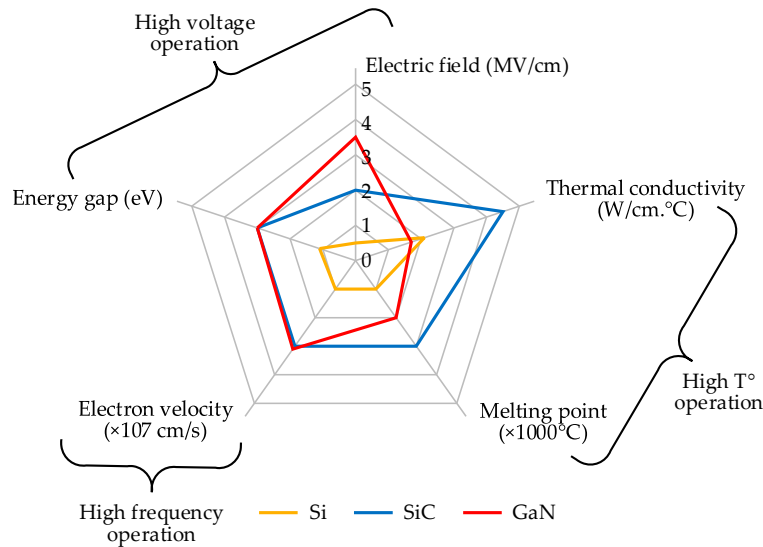

Figure 17. Comparison between Si, silicon carbide (SiC) and gallium nitride (GaN) power modules.

Power loss calculation is critical for thermal management and cooling in terms of applications with high power density. Power losses for WBG and Si-based semiconductors consist of conduction and switching losses. The low on-state resistance of WBG power devices contributes to a reduced conduction loss compared with Si-based modules. Generally, a freewheeling diode is connected to the semiconductor to ensure current continuity, which contributes additional power losses during reverse recovery behavior.

During the power losses calculation, the effect of temperature on the switching devices is neglected to simplify the loss model. The conduction loss for power switches is calculated within one fundamental period [137, 138] which is obtained by

$$P_{conT} = \frac{1}{T}\int_{t_0}^{t_0+T} i_T(t)v_T(t)dt = \frac{1}{T}\int_{t_0}^{t_0+T} i_T(t)(V_{T0} + R_T i_T(t))dt \tag{33}$$

$$P_{conD} = \frac{1}{T}\int_{t_0}^{t_0+T} i_F(t)v_F(t)dt = \frac{1}{T}\int_{t_0}^{t_0+T} i_F(t)(V_{D0} + R_D i_F(t))dt \tag{34}$$

where P_{conT} and P_{conD} stand for the conduction loss of the transistors and diodes, i_T and i_F are the conduction current, V_{T0} and V_{D0} donate the saturation voltage, and R_T and R_D represent the slope resistance, respectively.

Switching loss is related to the count of all the switching actions during each fundamental period, since energy is charged and discharged by the inherent capacitor during each transition of turning on and turning off period. The switching loss is calculated by using a look-up table technique, and the calculation model is expressed by [137,138]

$$P_{onT} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_T(t)}{v_{T\_ref}}E_{on}(i_T(t))\right\} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_T(t)}{v_{T\_ref}}\frac{i_T(t)}{i_{T\_ref}}E_{on}(i_{T\_ref})\right\} \tag{35}$$

$$P_{offT} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_T(t)}{v_{T\_ref}}E_{off}(i_T(t))\right\} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_T(t)}{v_{T\_ref}}\frac{i_T(t)}{i_{T\_ref}}E_{off}(i_{T\_ref})\right\} \tag{36}$$

$$P_{recD} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_D(t)}{v_{D\_ref}}E_{rec}(i_D(t))\right\} = \frac{1}{T}\sum_{i=1}^{N_i}\left\{\frac{v_D(t)}{v_{D\_ref}}\frac{i_F(t)}{i_{F\_ref}}E_{rec}(i_{F\_ref})\right\} \tag{37}$$

where P_{onT} and P_{offT} donate the turn-on and turn-off switching loss of the transistors and diodes, P_{recD} donates the diode reverse recovery loss, E_{on} and E_{off} stand for the turn-on and turn-off energies of power switches, and E_{rec} is the diode reverse recovery energy. The switching energies are proportional to the ratios of the occurring blocking voltage (v_T and v_D) to the reference blocking voltage (v_{T_ref} and v_{D_ref}) and the switching current (i_T and i_F) to the reference current (i_{T_ref} and i_{F_ref}). Therefore, the total power losses P_{tot} can be calculated by the sum of the conduction and switching losses of transistors and diode, as

$$P_{tot} = P_{con} + P_{sw} = P_{conT} + P_{conD} + P_{onT} + P_{offT} + P_{recD}. \tag{38}$$

The MMC efficiency is given by

$$\eta = (1 - \frac{P_{tot}}{P_{MMC}}) \times 100\% \tag{39}$$

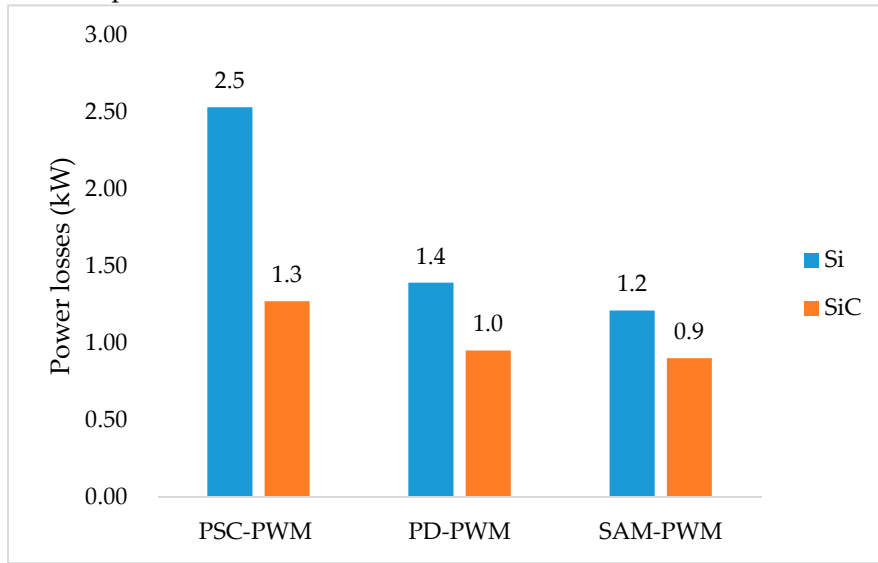where η is the MMC efficiency and P_{MMC} is the MMC power.

In order to assess the thermal performance of conventional Si-based semiconductors and WBG switching modules modulated by different modulation techniques for the MMC, the power losses calculation model is carried out with the simulation model in MATLAB by using the simulation parameters in Table 3. The comparative evaluation indexes include power losses and MMC efficiency. In addition, the total harmonic distortion (THD) of the output voltage is also investigated regarding different modulation methods. The modulation methods applied in the comparative study include PSC-PWM, PD-PWM, and SAM-PWM. PD-PWM is selected as a representative of LSC-PWM. SVM-PWM and SHE-PWM are excluded owing to their implementation complexity and calculation burden. In addition, the reason for not selecting NLM-PWM is that it is not suitable in application with a relatively small number of submodules, which leads to serious harmonic distortion. The switching frequency for both PSC-PWM and PD-PWM is set to 20 kHz, and the sampling rate for SAM-PWM is 2000 Hz. The semiconductor characteristics are extracted from the device datasheets CAS120M12BM2 and 2MBI150U2A-060.
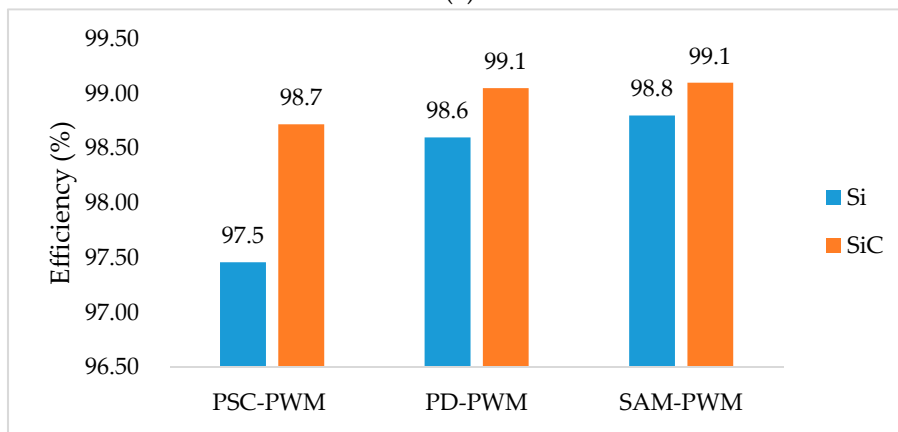
Table 3. MMC parameters for performance testing.

Parameters	Values
No. of submodules per leg	5
Nominal SM voltage	300 V
DC-link voltage	1500 V
RMS grid voltage	380 V
Grid frequency	50 Hz
Nominal power level	100 kW
Modulation technique	PSC-PWM, PD-PWM, SAM-PWM
Switching frequency rang	20 kHz; 20-100 kHz

The simulation results are demonstrated graphically as in Figures 18. Figure 18 illustrates the comparative performance based on semiconductor power losses, MMC efficiency, and output voltage THD by using different modulation methods. From Figure 18a and 18b, it is noticed that SiC modules, compared to Si devices, yield lower power losses and higher power efficiency for all the three modulation techniques. It is also indicated that the PSC-PWM has higher power losses following with the PD-PWM and SAM-PWM for both Si and SiC switches in Figure 18a, which leads
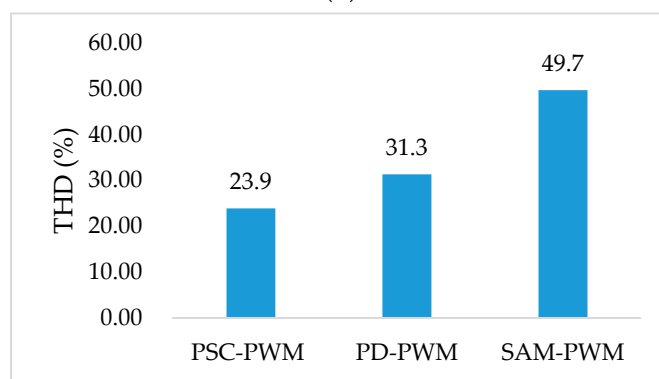
to a reduced MMC efficiency, as shown in Figure 18b. In spite of lower performance in power losses and efficiency, Figure 18c manifests that PSC-PWM is prominent in providing good voltage quality with lower THD compared to the other two methods.
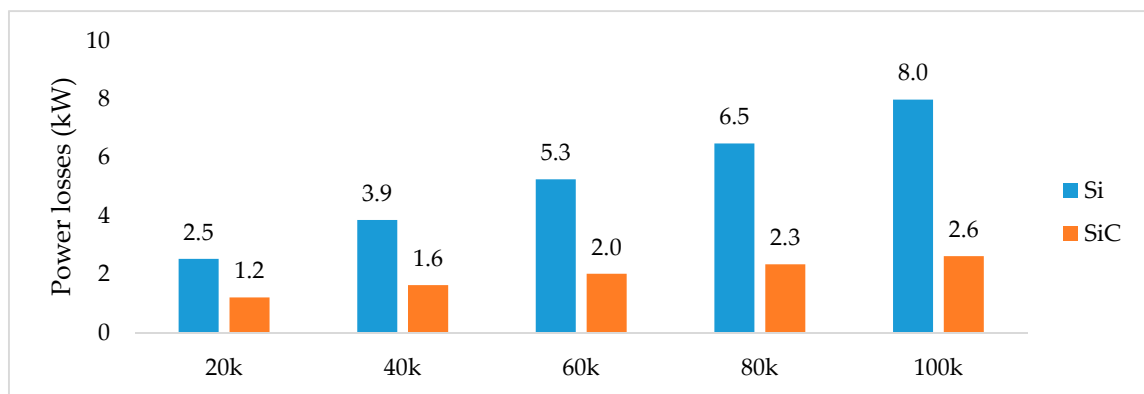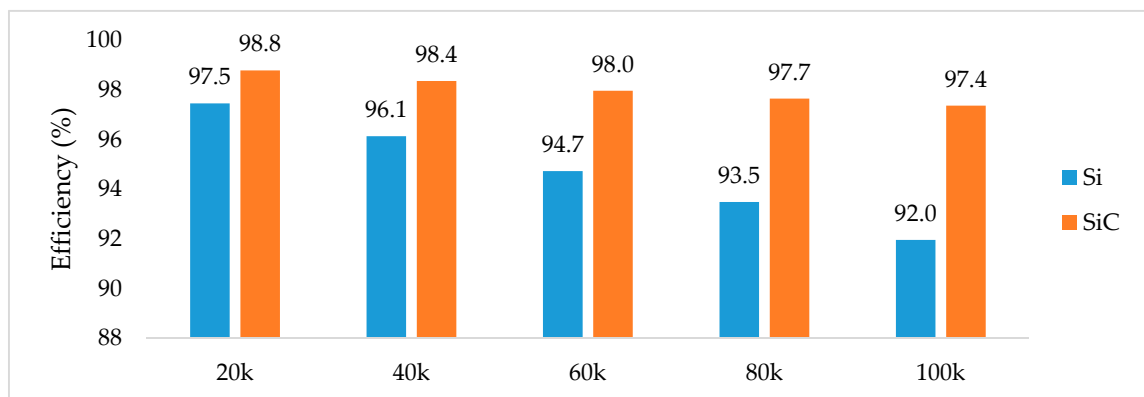

(**a**)

(**b**)

(**c**)

Figure 18. Comparative performance of using Si and SiC semiconductors with different modulation methods and load (100 kW) and input voltage per MMC HBSM (300 V): (**a**) Semiconductor power losses; (**b**) MMC efficiency; (**c**) Output voltage total harmonic distortion (THD).

Furthermore, to investigate the influence of switching frequency on Si and SiC semiconductors concerning power losses and MMC efficiency, the switching frequency is set from 20 to 100 kHz. PSC-PWM is selected as the modulation scenario in this comparative study. The simulation results are given in Figure 19. It is observed that power losses are reduced considerably by employing SiC

semiconductors compared to Si modules in Figure 19a. In particular, the power losses of Si power modules rise rapidly as the switching frequency increases, while those of the SiC devices increase much slower. This leads to a difference in terms of MMC efficiency, as shown in Figure 19b. It is noted that the MMC efficiency is capable of maintaining above 97% by using SiC switches at the switching frequency span of 20–100 kHz in this case, whereas the efficiency of Si-based MMC decreases to around 92% at the switching frequency of 100 kHz. The comparison of performance indicates that the differences in the material properties of switching devices lead to the fact that the WBG components have superior performance regarding reduced power losses and higher power efficiency, especially at the high switching frequency. The advantages of WBG power transistors can further substantially reduce the size of whole power conversion systems with strong robustness. It is expectable that WBG power switches will play a prominent role together with the MMC in the power conversion applications in the near future.

(**a**)

(**b**)

Figure 19. Comparative performance of using Si and SiC semiconductors at different switching frequencies and load (100 kW) and input voltage per MMC HBSM (300 V): (**a**) Semiconductor power losses; (**b**) MMC efficiency.

6. Conclusions

The MMC is expected to be a preferable choice in the medium and high-voltage power applications with intrinsic advantages such as scalable multilevel output voltage, low harmonic content of output voltage and output current, modular and flexible design, improved efficiency, and redundancy. As an application-oriented topology, it is predictable that the MMC will be guided to be more customized and well-adapted in the specific application area in terms of power transmission and quality improvement. This paper reviews the MMC with respect to the submodule and overall topologies, mathematical modeling and control methods, modulation techniques, and power losses with the incorporation of WBG technology. For submodule topology, the HBSM, owing to its simple architecture and low cost, maintains the domination in commercial utilization among a variety of

submodule configurations. Newly developed submodule circuits could be investigated along with a comparative study to compete and balance between module size and cost as well as switching losses and fault tolerance. New advanced topologies could be explored to output better performance and meet different load requirements with the overall structure of the MMC, especially under fluctuating or unbalanced load. With respect to MMC control, the output voltage and current control under different grid conditions, submodule balancing control, and circulating current control are discussed. The challenging issues include the submodule balancing control, circulating current control, multiple variables' simultaneous control, and the complexity of consequent control. Nonlinear and predictive control strategies could be promising alternatives compared to conventional control methods. Modulation techniques are reviewed and classified according to switching frequency with decent application area and implementation effort. Power losses are investigated with the incorporation of WBG technology by using different modulation methods and with different switching frequencies. The comparison of performance indicates that PSC-PWM has better output performance while generating higher power losses compared to PD-PWM and SAM-PWM, and the WBG semiconductors have superior performance regarding reduced power losses and higher power efficiency, especially at the high switching frequency. The incorporation of WBG technology will facilitate the MMC application with further advantages of high-voltage and high-power operations, low power losses, high efficiency, improved reliability, and reduced module size and cooling system. Finally, this review research focuses on the topology, modeling, control, and modulation techniques of the MMC for stationary applications, and future work will survey the MMC for vehicular applications.

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