Design of a Cooperative Voltage Harmonic Compensation Strategy for Islanded Microgrids Combining Virtual Admittance and Repetitive Controller

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Abstract—Non-linear loads (NLLs) in three-phase systems are known to produce current harmonics at -5, 7, -11, 13… times the fundamental frequency; harmonics of the same frequencies are induced in microgrid voltage, reducing therefore the power quality. Dedicated equipment like active power filters can be used to compensate the microgrid harmonics; alternatively, each distributed generation (DG) unit present in the microgrid can be potentially used to compensate for those harmonics. The use of the virtual admittance concept combined with a PI-RES control structure has been previously proposed as a harmonic compensation sharing strategy when multiple DGs operate in parallel. The drawback of this methodology is that a large number of RES controllers might be required to compensate for all harmonic components induced by NLLs, increasing the tuning complexity as well as the execution time. This paper proposes the combined use of virtual admittance control loop and repetitive controller (RC) for harmonic compensation. The main advantage of the proposed method is that only one RC is required to compensate for all the harmonic components, significantly reducing the computational burden and the design complexity. The dynamic performance of the whole system is tested under variable NLL.

Keywords—central controller, harmonic compensation, nonlinear loads, repetitive controller, resonant controller, virtual admittance

I. INTRODUCTION

During the last decades, the power generation strategy has been shifted from a centralized to a distributed scenario [2]. In a centralized scenario the power is generated in large centralized power plants that transmit the electric power over long distances. Opposite to this, in the distributed generation (DG) scenario the generators typically have a smaller size and are connected to the utility grid near where the electric power is used. This reduces the transmission losses as well as the size and number of power lines needed [3]. DG scenarios can be islanded or grid connected [4]-[5]. Both scenarios can combine linear loads (LL)

and non-linear loads (NLL). NLLs in three-phase systems are known to produce current harmonics typically at -5, 7, -11, 13… times the fundamental frequency (i.e. 50/60 Hz). As a consequence, harmonic components of the same frequencies are induced at the point of common coupling (PCC) voltage [6]-[8] in islanded microgrids (or in weak grid connections), adversely impacting the power quality. To overcome these problems, dedicated equipment like active power filters (APFs) are designed to compensate for those unwanted harmonic current components [9]. However, these solution brigs an increase of cost, also selection of APF is not trivial. An alternative to the use of APFs is to use the DG units to improve the microgrid's power quality. DGs can be required to inject high frequency currents to the PCC to compensate for harmonic components due to e.g. NLLs. A relevant issue in this case is to determine how much harmonic current must be injected by each DG unit participating in the strategy. It is desired in this case that DG units closer to where the disturbance is produced inject a larger share of the harmonic current, as this will reduce the associated loses. Centralized and distributed control strategies have been already proposed to address this issue [10]-[12].

A simple solution to select the amount of harmonic current injected by each DG is to use an agent that statically assigns the harmonic current command for each DG [12]. However, this solution typically does not take into account the microgrid topology, meaning that this strategy might not minimize the transmission losses due to the harmonic current injection. An alternative solution is the use of the virtual admittance concept [11]. This method dynamically adapts the mode of operation of the inverter to the microgrid condition, such that inverters located nearer the PCC contribute in a greater degree to the compensation task. Very important, this is achieved without previous knowledge of the grid topology.

Nonetheless, the virtual admittance concept [11] requires the use of a PI-RES control structure to inject the inverter´s current harmonics. A resonant controller (RES) is used for each pair of harmonic components to be compensated for (a positive sequence harmonic and a negative sequence), therefore a large number of RES controllers might be required to compensate for all harmonic components induced by NLLs, which might result

in a significant increase of the computational burden and tuning difficulties.

To overcome this limitation, this paper proposes a virtual admittance control loop based on a repetitive controller (RC). [1]. The advantage of using a RC is that it can compensate all harmonic components with reduced computational burden and design and tuning complexity.

The paper is organized as follows: Section II presents the basics of the proposed harmonic compensation strategy. The repetitive controller design is analyzed in Section III. Simulation and experimental results validating the proposed methodology are presented in Sections IV and V respectively. Finally, the conclusions are presented in Section VI.

II. COOPERATIVE VOLTAGE HARMONIC COMPENSATION STRATEGY FOR ISLANDED MICROGRIDS

Fig. 1 shows a simplified microgrid configuration that will be used for analysis purposes. It includes two voltage source inverters (VSI) connected in parallel, the microgrid always working in island mode. Each VSI feeds a local linear load while a set of NLLs are connected at the PCC. One of the inverters is working in voltage control mode (VSI-VCM), and consists of an inner current control loop and an outer voltage control loop [11, 35-36]. This inverter sets the voltage magnitude and frequency at the PCC The other VSI is working in current control mode (VSI-CCM), and includes only the inner current control loop [11, 35-36].

A Central Controller measure the harmonic content at the PCC voltage and provides commands to the inverters for their cancellation. All the variables in the following block diagrams are referred to a reference synchronous with the harmonic h being controlled inv: inverter-side or out: LCL output). The cooperative harmonic compensation strategies, including using a central controller and local controllers and the virtual admittance concept are described following.

A. Central Controller

The objective of a cooperative harmonic compensation strategy is to make use of all inverters connected to the PCC to inject harmonic currents consumed by NLLs. The central controller shown in Fig. 1 receives the information of the PCC voltage harmonic components, a communication channel (industrial bus, WiFi, ZigBee, mobile communications …) being used for this purpose. The central controller implements a PI regulator for each harmonic component to be compensated for, its reference $u^{h*}_{out\ dqh}$ being typically set to zero, as PCC voltage harmonic components are normally desired to be fully compensated. The output of each harmonic PI controller, i^{h*}_{dqh}, is then transmitted, the reference being common to all inverters.

B. Local Controller with virtual admittance

The harmonic current sharing being implemented uses the virtual admittance concept, (1)-(3) and Fig. 1. A virtual admittance is connected between the inverter output and the LCL filter ($Y^h_{v\ 1}$ and $Y^h_{v\ 2}$ in Fig. 1 [11]). This Virtual Admittance is a control gain, and does not consume therefore any power. The *virtual current* consumed by the virtual admittance (2) depends on its value and the inverter output voltage. I.e. for the same harmonic voltage, the higher the value of the inverter virtual admittance is, the lower the current that the inverter injects to the PCC is. In case of selecting the same Virtual Admittance for both inverters, the inverter with the higher output impedance will inject less current [11]. This is a very interesting feature, since inverters closer to the PCC will naturally inject more current, hence minimizing the transmission losses.

$$i_{inv\ dqh} = i^{h*}_{out\ dqh} - Y_{v\ n} \cdot u_{inv_{dqh}} \tag{1}$$

$$\left| i_{Y_v} \right| = \left| Y_{v\ n} \right| \cdot \left| u_{inv_{dqh}} \right| \tag{2}$$
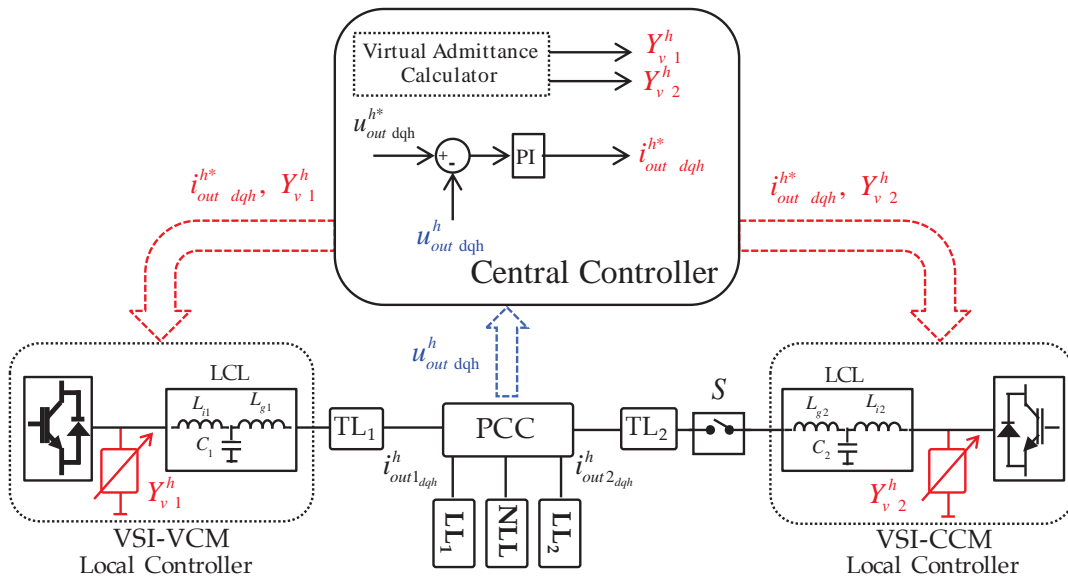

Fig. 1. Islanded scenario with two parallel-connected VSIs, operating in voltage control mode (VCM) and current control mode (CCM) respectively. "S" and "TL" block stand for static switches and transmission line respectively. Linear (LL) and nonlinear (NLL) loads are connected to the PCC.

The current injected by each inverter consist of a fundamental current and harmonic current components. A synchronous PI current regulator is typically used to control the fundamental current. Resonant controllers were proposed in [11] to control the harmonic currents. Use of repetitive current controller (RC) [13]-[15] for this purpose is proposed in the next section. Advantages of RCs include simultaneous control of multiple harmonic components and easiness of its design and tuning.

III. REPETITIVE CONTROLLER DESIGN

A. Repetitive Controller Background

The concept of repetitive control was originally developed in 1980 by Inoue et al. for a single input single output (SISO) plant in the continuous time domain to track a periodic repetitive signal with defined period, and was applied successfully to control a proton synchrotron magnet power supply in 1981 [25]. The concept was then further investigated by Hara et al. [13]. Based on the internal model principle proposed by Francis and Wonham in 1975, any periodic reference (disturbance) signal with known period can be tracked (rejected) by including their generator in the stable closed loop [26]. Therefore, RC is based on the idea of introducing the disturbance (signal) model in the system to track or reject it. Repetitive controllers have been widely used in applications including PWM inverters [27-30], PWM rectifiers [31], matrix converters [16], robotic manipulators [32], disk drive systems [33], four legs VSI [34]. The repetitive controller (RC), is a well know alternative to the use of a set of resonant controllers. The intrinsic characteristic of the RCs allows the automatic compensation of a defined set of multiple frequencies. The model can be introduced in both the continuous (Fig. 2) and discrete domain (Fig. 3), but the latter implementation, in digital system, has a more straightforward implementation by using (3). This results in a slow control action capable of cancelling the system steady state error to a periodic reference cycle by cycle (or rejecting periodic disturbances in the same way). To do so the RC requires to store some samples in the control system memory. It is noted however that memory requirements is negligible for most modern digital platform capabilities. RC can be used on its own only on an intrinsically stable system; for more general applications, it needs therefore to be used in conjunction with another controller (for example P or PI) which is designed with the aim of system stabilization and transient response performance.

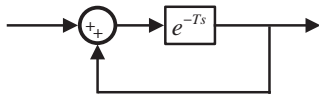$$G_{REP} = \frac{z^{-N}}{1-z^{-N}}; N = \frac{f_S}{f_{comp}} \qquad (3)$$
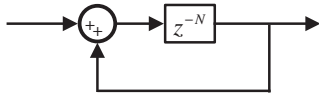
Fig. 2.- Continuous periodic model

Fig. 3. - Discrete periodic model

The delay N is an integer value that, which together with the sampling frequency f_s, and f_{comp} being the first target frequency to be compensated. Three different schemes of combined plant compensator and RC controllers have been proposed in the literature [14]: parallel, series and the plug-in. The plug-in structure (Fig. 4) is used in this work as it shows several advantages including the possibility to design separately the RC and the plant compensator. The plant compensator G_C is firstly design to stabilize the plant and later the parameters of the RC are chosen to achieve the target signal tracking. To ensure the stability of the overall system, the basic scheme has to be modified to obtain the RC shown in Fig. 5.
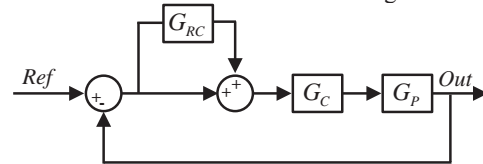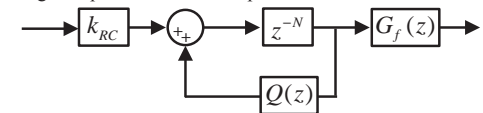
Fig. 4.- Plug-in repetitive Control loop.

Fig. 5- Repetitive controller structure

The structure of the RC is characterized by a learning gain k_{RC}, a robustness filter $Q(z)$ and a stability filter $G_f(z)$. The robustness filter is designed to increase the stability margin of the system while the learning gain together with the stability filter is used to stabilize the entire loop. As summarized in [19], if the two following conditions are satisfied, the stability of the system is ensured:

1. All the poles of the close loop without the RC must be within the unity circle.
2. The absolute value of the function $S(z)$ (4) is less than the unity for all the frequency below the Nyquist frequency.

$$S\left(e^{j\omega T_s}\right) = Q\left(e^{j\omega T_s}\right) - \frac{k_{RC}G_f\left(e^{j\omega T_s}\right)G_c\left(e^{j\omega T_s}\right)G_P\left(e^{j\omega T_s}\right)}{1+G_c\left(e^{j\omega T_s}\right)G_P\left(e^{j\omega T_s}\right)}$$

$$\forall \omega \le \omega_{NYQ} \qquad (4)$$

The second condition is obtained applying the small gain theorem [17] to the error transfer function of the control loop shown in Fig. 3. Several choices exist to define the RC controller. First of all the robustness filter $Q(z)$ can be either a close-to-unity gain constant [19] or a moving average filter [22]. Both solutions enhance the stability margin of the model; the close-to-unity choice is the simplest solution in terms of implementation, but it compensates all the poles in the same manner. This means poorer tracking/rejection at lower frequencies. The second solution considers the use of a low pass filter that moves the high frequency poles inside the unity circle, resulting in poorer performances only for the high frequency poles. This solution is an acceptable trade-off between reasonable stability margins and accurate tracking/rejection at lower frequencies. For what concerns the

stability filter $G_f(z)$ two different solutions can be adopted, as discussed in [16]. The first solution is a zero-phase-error-tracking-compensator [21]; however, the design is quite complicated and an accurate plant model is required. An alternative solution is the time-advanced-compensator that has the effect of balancing the phase shift introduced by the RC. The time-advanced compensator assumes the expression (5), where T_A is the time advanced step. The k_{RC} gain is adjusted to achieve the condition of the small gain theorem. In general the range of feasible values for the repetitive controller is $0 < k_{RC} < 2$.

$$G_f(z) = z^{T_A} \qquad (5)$$

B. Repetitive Controller Design

The proposed control is based on the plug-in configuration of the repetitive controller. PI gains have been selected to guarantee stability and achieve a current loop bandwidth of 100 Hz via a zero-pole cancellation technique [17].

Once the PI controller has been adjusted, the number of delays N is given by (3). The low pass filter Q(z), the stability filter G_f(z) and the learning gain k_{RC} are selected to satisfy the aforementioned stability conditions: $S(e^{j\omega T_S}) < 1, \forall \omega \le \omega_{NYQ}$ [19]. In particular, the low pass filter has been selected as a moving average filter whose transfer function is (6).

$$Q(z) = \frac{0.0625z^4 + 0.25z^3 + 0.375z^2 + 0.025z + 0.0625}{z^2} \qquad (6)$$

This solution allows a more accurate tracking of the low frequency components than the close-to-unity gain, and at the same time it enhances the stability reducing the gain at higher frequencies.

The stability filter $G_f(z)$ has been selected as a time-advanced compensator (5) in order to offset the phase lag of the system.

The proposed design uses a sampling frequency of 9.9 kHz and number of finite delays N equal to 33 (3). The learning gain k_{RC} has been adapted for the different network topologies; for doing so an initial learning gain $k_{RC\ init}$ has been defined to stabilize the system when the VSI-CCM inverter is not connected to the PCC (Fig. 1). The design parameters are summarized in Table I.

IV. SIMULATION RESULTS

Fig. 1 and Table I show the simulation scenario and the simulation parameters respectively. Fig. 6 shows the local controller block diagram that is implemented in each inverter (VSI-VCM and VSI-CCM, see Fig. 1); it includes the virtual admittance control loop (shown in red color, see Fig. 6; more details can be found in [11]) and the plug-in RC.

Fig. 7 shows the simulation results using both the proposed control strategy with a RC, and with RES controllers [11]. The central controller of Fig. 1 is configured to compensate the -5th, 7th, -11th and 13th harmonic voltage components at the PCC. Consequently, RES controllers [11] include the -5th, 7th, -11th and 13th harmonic components, implemented as two RES controllers in a fundamental frequency synchronous reference frame.

- For t=0.0 to 0.6 s: Only non-linear load NLL$_1$ is connected to the PCC. The THD at the PCC voltage is 8.7 %.

- For t=0.6 to 2.0 s: Cooperative harmonic compensation is enabled, the virtual admittance of both inverters is set to zero. Both PI-RC and PI-RES implementations are observed to reduce the voltage THD to 0.5%, the transient response being similar in both cases as well. Figs. 7c-7e show the magnitude of the harmonic current injected by each inverter for the PI-RC and PI-RES implementations, both VSI-VCM and VSI-CCM injecting the same amount of current for all of the controlled harmonics.

- For t=2.0 to 3.5 s: the VSI-VCM virtual admittance is set to 0.05 Ω^{-1} while the VSI-CCM virtual admittance is set to 0.01 Ω^{-1}. Independent of the control method, the higher the virtual admittance is (VSI-VCM), the lower the current injected is (see Fig. 7b-7e).

- For t=3.5 to 5 s a second NLL (NLL$_2$) identical to NLL$_1$ is connected to the PCC. The PCC voltage harmonic content, and thus its THD, temporarily increase until the central controller responds (Fig. 7b). The harmonic currents injected by the VSI-VCM and VSI-CCM follow the same trend as for the case of NLL$_1$ (t<3.5s). The VSI-CCM injects more harmonic current since its virtual admittance is smaller.

- For t>5s, the virtual admittances of both inverters are set to 0.1 Ω^{-1} (Fig. 7a). In this case, the VSI-CCM injects more harmonic current than the VSI-VCM (Figs. 7c-7e) since for the same virtual admittance value, the inverter with the smaller output impedance (Table I) compensates in a greater degree, therefore minimizing the transmission losses [11].
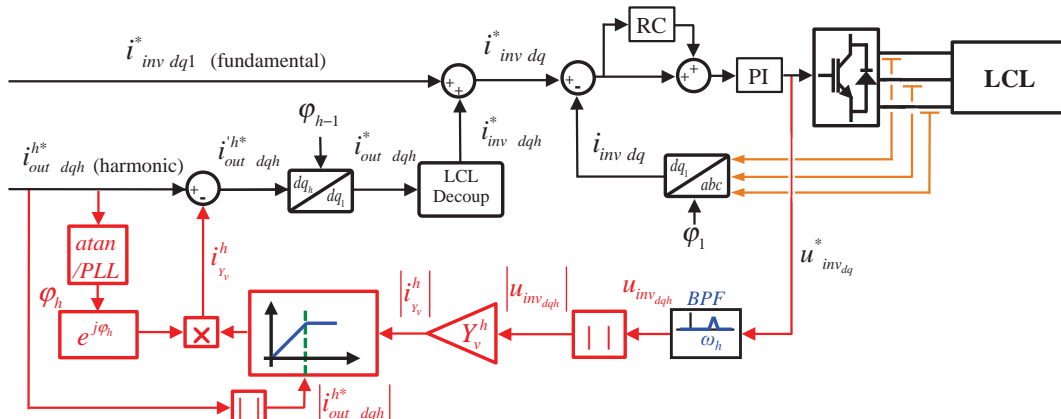

Fig. 6. Local controller block diagram including the virtual admittance and the RC.

a) Virtual admittances.

b) Magnitude of the voltage harmonics and THD.

c) Magnitude of the resulting -5th current harmonic.

d) Magnitude of the resulting 7th current harmonic.

e) Magnitude of the resulting -11th current harmonic.

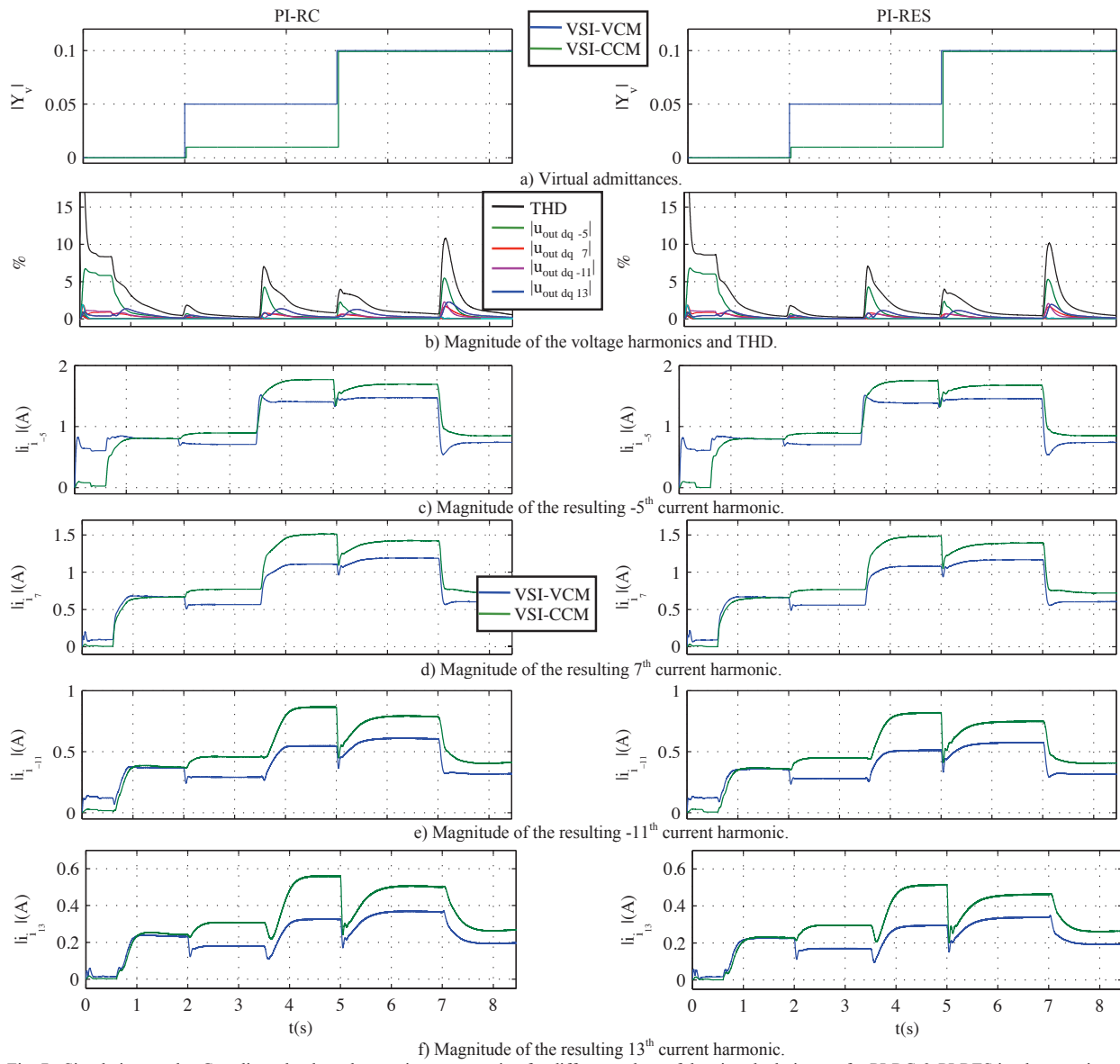f) Magnitude of the resulting 13th current harmonic.

Fig. 7.- Simulation results. Coordinated voltage harmonic compensation for different values of the virtual admittance for PI-RC & PI-RES implementations.
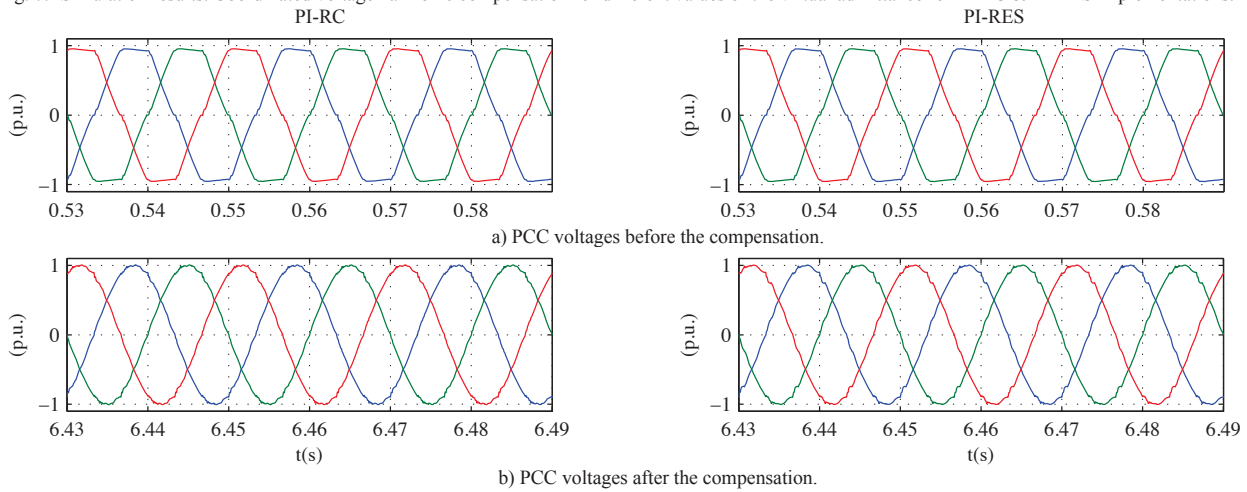

a) PCC voltages before the compensation.

b) PCC voltages after the compensation.

Fig. 8.- Simulation results. PCC voltages in *abc* quantities before and after harmonic compensation is enabled.

- For t>7 s, the NLL_2 is disconnected from the PCC. A large peak occurs in the PCC harmonic voltage components and consequently in its THD. This transient increase is compensated by the central controller in around 0.5s. In this case, the harmonic currents injected by the two inverters decrease (Figs. 7c-7e), the VSI-CCM injecting more current than the VSI-VCM. Fig. 8a and 8b the PCC voltages before and after the compensation.

Table I – Setup Parameters		VSI-VCM Inverter	VSI-CCM Inverter
Rated power		50kW	50kW
Rated voltage		380V	380V
Capacitor equivalent series resistance		0.052 Ω	0.052 Ω
Inductor equivalent series resistance		0.05 Ω	0.05 Ω
Inverter-side inductor		2.4 mH	2.196 mH
Capacitor filter		10 μF	10 μF
Grid-side inductor		1.6 mH	0.5 mH
Switching frequency		9.9 kHz	9.9 kHz
Local Linear Load		53 Ω	53 Ω
Centralized controller			
Kp_{-5}	0.07	Ki_{-5}	0.9
Kp_7	0.3	Ki_7	0.9
Local PI-RES			
Kp	8	Ki	3000
$Kp_{RES\,6}$	1	C	300
N	6	fs	9.9 kHz
Local PI-RC VSI-VCM Inverter			
k_{RCinit}	0.5	N	33
k_{RC}	1	fs	9.9 kHz
TA	2	$fcomp$	300Hz
Local PI-RC VSI-CCM Inverter			
k_{RCinit}	0.1	N	33
k_{RC}	1.2	fs	9.9 kHz
TA	2	$fcomp$	300Hz

V. EXPERIMENTAL RESULTS

This section shows the experimental verification of the proposed control strategy. The experimental setup is the same as in simulation (see Fig. 1), the main parameters being shown in Table I. The central controller, which is implemented in a computer. It receives the PCC voltage measurements, calculates and sends the required harmonic current references. The central controller also selects the virtual admittances for the VSI-VCM and VSI-CCM, which in the end determines the harmonic current sharing. Both inverters are connected to the PCC, the microgrid being disconnected from the main grid. Harmonics being compensated are the same as in simulation (see Fig. 7). A *WiFi* link is used to transfer measurements, current references and virtual admittances among inverters and the central controller. The sampling frequency of the central controller is 5 Hz.

Fig. 9 shows the response of both the PI-RC controller (Fig. 6) and the control strategy proposed in [11] using a PI-RES. The same virtual admittances are used for both control strategies (Fig. 9a). Fig. 9b shows the THDs for both type of controllers while Figs. 9c-9f show the -5th, 7th, -11th and 13th harmonic currents injected by the VSI-VCM and VSI-CCM respectively.

- For t=0.0 to 6.0 s: a non-linear load NLL_1 is connected to the PCC, producing voltage harmonics. The measured THD is 10.6%.
- For t=6.0 to 12.0 s the compensation strategy is activated, the virtual admittances of the VSI-VCM and VSI-CCM inverters being set to zero (Fig. 9a). The compensation strategy reduces to 1% both for PI-RC and PI-RES controllers, transient response being similar in both cases as well. These results are in good agreement with the simulation results (Fig. 7), both inverters injecting a similar amount of harmonic current, i.e. -5th, 7th, -11th, 13th.
- For t=12.0 to 18.0 s, VSI-VCM and VSI-CCM virtual admittances are set to 0.05 Ω-1 and 0.01 Ω-1 respectively (Fig. 9a). It is observed from Figs. 9c-9f that the inverter with the smaller virtual admittance injects more harmonic current, the corresponding transient lasts ≈1 s.
- For t=18.0 to 24.0 s, NLL_2, is connected to the PCC. Both methods show a transient increase of the THD after connection of the NLL_2 (Fig. 9b), until the central controller responds. The current injected by both inverters increase (see Figs. 9c-9f), harmonics at the PCC voltage being compensated after ≈1 s. Note that the inverter with the smaller virtual admittance injects a larger amount of harmonic current (VSI-VCM).
- For t> 24 s NLL_2 is disconnected from the PCC, and the virtual admittance of both inverters is set to 0.1 Ω⁻¹. The THD for both methods shows of a noticeable transient increase (t=24 s) until the central controller responds in ≈1 s. As already discusses in the previous section, using the same virtual admittance does not guarantee that both inverters will inject the same amount of harmonic current, as the LCL filter input voltage also affects ($u_{inv_{dqh}}$ in Fig. 6). In this case, VSI-CCM inverter uses smaller inductances (see Table I), therefore requiring less voltage to produce the same amount of harmonic current [11].

Figs. 10a show the PCC voltages when the harmonic compensation strategy is disabled, while Figs. 10b shows the PCC voltages both for PI-RC and PI-RES strategies. Experimental results shown in Figs. 9-10 are in good agreement with simulation results shown in Fig. 7-8, the differences being due to limited the accuracy of the current sensors, non-linear behavior of the inverters and the limited communications bandwidth.

It is finally noted that the increased complexity of the RES based solution has a direct impact on the computational burden. The number of clock cycles required by each controller can be used for comparison purposes. The control strategies discussed in this paper have been implemented in a Texas Instruments DSP (TMS320F28335). The RC control strategy requires 104 clock cycles while a single RES controller requires 116 clock cycles. Thus, for the particular configuration used for the experimental verification of the propose methods, the RES controllers require 232 cycles [11]. Furthermore, compensation of a larger number of harmonics would be straightforward and at no cost for the PI-RC based solution, while the PI-RES based solution will require additional RES controllers, consequently increasing the computational burden.

a) Virtual admittances.

b) Magnitude of the voltage harmonics and THD.

c) Magnitude of the resulting -5th current harmonic.

d) Magnitude of the resulting 7th current harmonic.

e) Magnitude of the resulting -11th current harmonic.
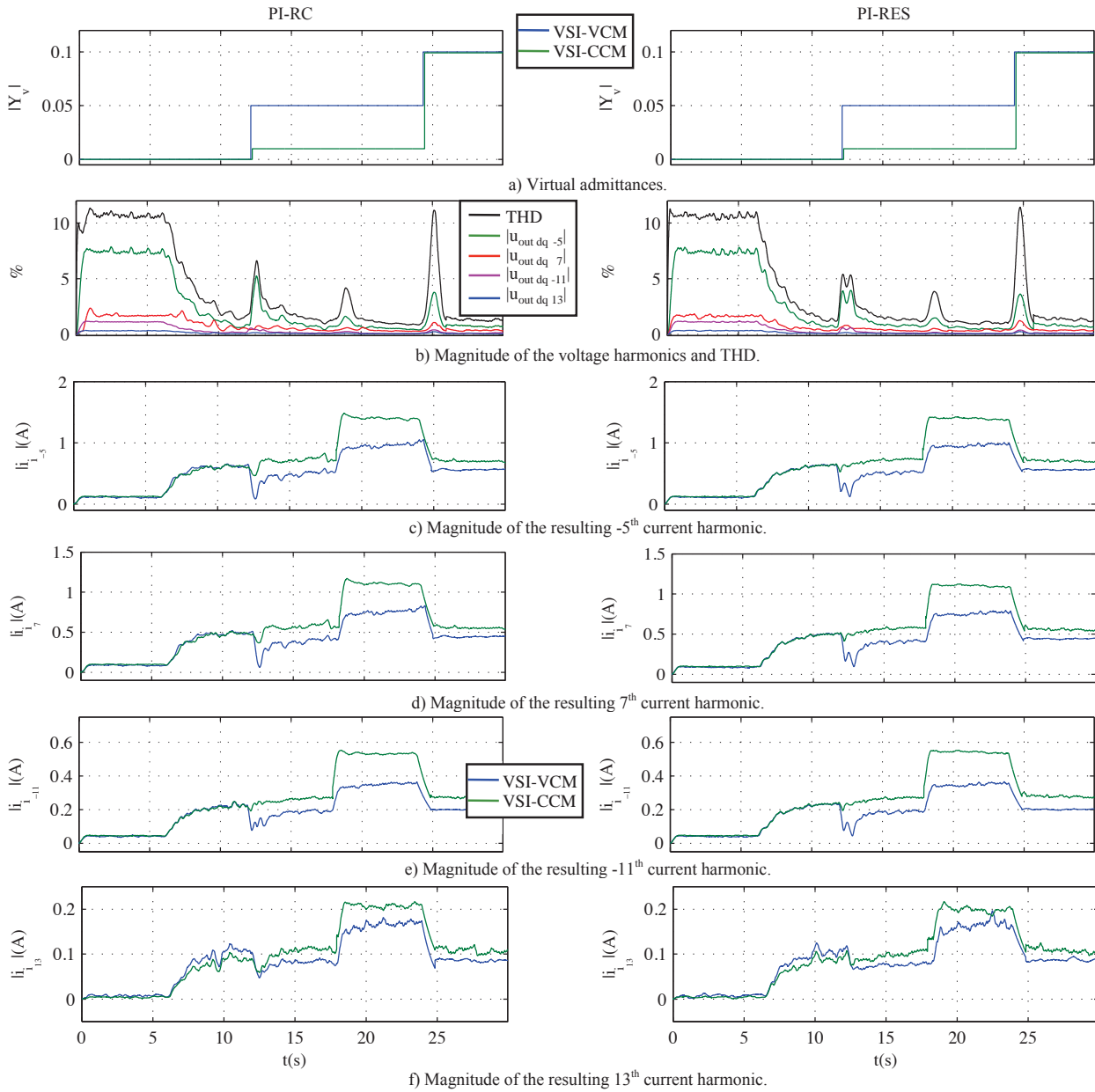
f) Magnitude of the resulting 13th current harmonic.

Fig. 9.- Experimental results. Coordinated voltage harmonic compensation for different values of the virtual admittance for PI-RC & PI-RES implementations

a) PCC voltages before the compensation.
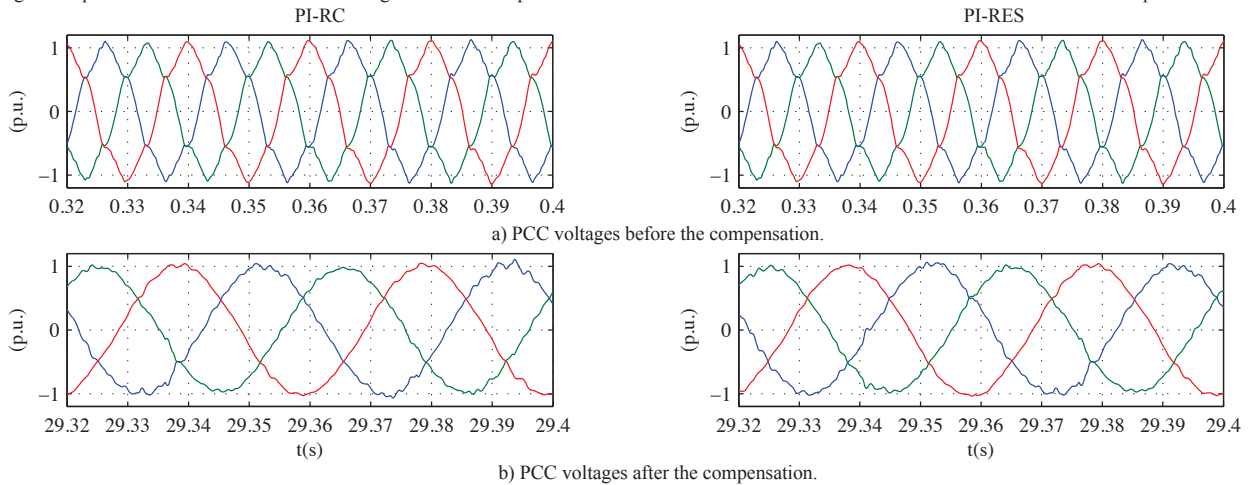
b) PCC voltages after the compensation.

Fig. 10.- Experimental results. PCC voltages in *abc* quantities before and after harmonic compensation is enabled.

I. CONCLUSIONS

In this paper, a cooperative voltage harmonic compensation strategy based on a centralized controller, combined with the virtual admittance concept was proposed. Two types of controller concepts for harmonic compensation have been evaluated, namely resonant and repetitive.

PI-RES controllers based solutions require multiple RES controllers, which increases the complexity and the computational burden proportionally to the number of harmonics to compensate. On the other hand, PI-RC can provide the same performance with significantly reduced computational burden and tuning difficulties. The proposed concepts have been confirmed by means of simulation and experimentally. The verification has included both static and dynamic NLL scenarios.

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