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This index covers all technical items—papers, correspondence, reviews, etc.—that appeared in this periodical during 2019, and items from previous years that were commented upon or corrected in 2019. Departments and other items may also be covered if they have been judged to have archival value.

The Author Index contains the primary entry for each item, listed under the first author's name. The primary entry includes the coauthors' names, the title of the paper or other item, and its location, specified by the publication abbreviation, year, month, and inclusive pagination. The Subject Index contains entries describing the item under all appropriate subject headings, plus the first author's name, the publication abbreviation, month, and year, and inclusive pages. Note that the item title is found only under the primary entry in the Author Index.

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A 65-nm Neuromorphic Image Classification Processor With Energy-Efficient Training Through Direct Spike-Only Feedback. *Park, J., +, JSSC Jan. 2020 108-119*

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A Smart Contact Lens Controller IC Supporting Dual-Mode Telemetry With Wireless-Powered Backscattering LSK and EM-Radiated RF Transmission Using a Single-Loop Antenna. *Jeon, C., +, JSSC April 2020 856-867*

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A 0.032-mm² 43.3-fJ/Step 100–200-MHz IF 2-MHz Bandwidth Bandpass DSM Based on Passive N -Path Filters. *Zhang, Y., +, JSSC Sept. 2020 2443-2455*

A Multiband FDD SAW-Less Transmitter for 5G-NR Featuring a BW-Extended N -Path Filter-Modulator, a Switched-BB Input, and a Wideband TIA-Based PA Driver. *Qi, G., +, JSSC Dec. 2020 3387-3399*

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A Low-Power VGA Vision Sensor With Embedded Event Detection for Outdoor Edge Applications. *Zou, Y., +, JSSC Nov. 2020 3112-3121*

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A 0.5-V Sub-10- μW 15.28-m $\Omega/\sqrt{\text{Hz}}$ Bio-Impedance Sensor IC With Sub-1° Phase Error. *Kim, K., +, JSSC Aug. 2020 2161-2173*

The Design of a CMOS Nanoelectrode Array With 4096 Current-Clamp/Voltage-Clamp Amplifiers for Intracellular Recording/Stimulation of Mammalian Neurons. *Abbott, J., +, JSSC Sept. 2020 2567-2582*

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Biomedical electrodes

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A 64-Channel Transmit Beamformer With ± 30 -V Bipolar High-Voltage Pulsers for Catheter-Based Ultrasound Probes. *Tan, M., +, JSSC July 2020 1796-1806*

A $7 \times 7 \times 2$ mm³ 8.6- μ W 500-kb/s Transmitter With Robust Injection-Locking-Based Frequency-to-Amplitude Conversion Receiver Targeting for Implantable Applications. *Xiong, B., +, JSSC June 2020 1698-1708*

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Biomedical equipment

A 0.5-V Sub-10- μ W 15.28-m Ω /Hz Bio-Impedance Sensor IC With Sub-1° Phase Error. *Kim, K., +, JSSC Aug. 2020 2161-2173*

Biomedical transducers

A 64-Channel Transmit Beamformer With ± 30 -V Bipolar High-Voltage Pulsers for Catheter-Based Ultrasound Probes. *Tan, M., +, JSSC July 2020 1796-1806*

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A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes. *Kang, E., +, JSSC Dec. 2020 3157-3168*

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The Design of a CMOS Nanoelectrode Array With 4096 Current-Clamp/Voltage-Clamp Amplifiers for Intracellular Recording/Stimulation of Mammalian Neurons. *Abbott, J., +, JSSC Sept. 2020 2567-2582*

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A Smart Hardware Security Engine Combining Entropy Sources of ECG, HRV, and SRAM PUF for Authentication and Secret Key Generation. *Cherupally, S.K., +, JSSC Oct. 2020 2680-2690*

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Bipolar MMIC

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Blood

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Blood vessels

A 1.8-GHz Near-Field Dielectric Plethysmography Heart-Rate Sensor With Time-Based Edge Sampling. *Chien, J., JSSC March 2020 615-628*

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A 0.5-V BLE Transceiver With a 1.9-mW RX Achieving -96.4 -dBm Sensitivity and -27 -dBm Tolerance for Intermodulation From Interferers at 6- and 12-MHz Offsets. *Tamura, M., +, JSSC Dec. 2020 3376-3386*

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A $7 \times 7 \times 2$ mm³ 8.6- μ W 500-kb/s Transmitter With Robust Injection-Locking-Based Frequency-to-Amplitude Conversion Receiver Targeting for Implantable Applications. *Xiong, B., +, JSSC June 2020 1698-1708*

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A 6.78-MHz Single-Stage Wireless Charger With Constant-Current Constant-Voltage Charging Technique. *Cheng, L., +, JSSC April 2020 999-1010*

Brain-computer interfaces

A Single-Chip Bidirectional Neural Interface With High-Voltage Stimulation and Adaptive Artifact Cancellation in Standard CMOS. *Uehlin, J.P., +, JSSC July 2020 1749-1761*

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A 2-in-1 Temperature and Humidity Sensor With a Single FLL Wheatstone-Bridge Front-End. *Jiang, H., +, JSSC Aug. 2020 2174-2185*

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A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC. *Song, Y., +, JSSC Feb. 2020 312-321*

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A Continuous-Time Zoom ADC for Low-Power Audio Applications. *Gonen, B., +, JSSC April 2020 1023-1031*

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A 20.5 TOPS Multicore SoC With DNN Accelerator and Image Signal Processor for Automotive Applications. *Yamada, Y., +, JSSC Jan. 2020 120-132*

A 28-nm Automotive Flash Microcontroller With Virtualization-Assisted Processor Supporting ISO26262 ASIL D. *Kondo, H., +, JSSC Jan. 2020 133-144*

C

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A 7.3 M Output Non-Zeros/J, 11.7 M Output Non-Zeros/GB Reconfigurable Sparse Matrix–Matrix Multiplication Accelerator. *Park, D., +, JSSC April 2020 933-944*

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A 1-nA 4.5-nW 289-ppm/°C Current Reference Using Automatic Calibration. *Lee, S., +, JSSC Sept. 2020 2498-2512*

- A 1.02-pJ/b 20.83-Gb/s/Wire USR Transceiver Using CNRZ-5 in 16-nm FinFET. *Tajalli, A., +, JSSC April 2020 1108-1123*
- A 1.6-GS/s 12.2-mW Seven-/Eight-Way Split Time-Interleaved SAR ADC Achieving 54.2-dB SNDR With Digital Background Timing Mismatch Calibration. *Guo, M., +, JSSC March 2020 693-705*
- A 12-b 18-GS/s RF Sampling ADC With an Integrated Wideband Track-and-Hold Amplifier and Background Calibration. *Ali, A.M.A., +, JSSC Dec. 2020 3210-3224*
- A 12.3- μ W 0.72-mm² Fully Integrated Front-End IC for Arterial Pulse Waveform and ExG Recording. *Hsu, Y., +, JSSC Oct. 2020 2756-2770*
- A 13.5-ENOB, 107- μ W Noise-Shaping SAR ADC With PVT-Robust Closed-Loop Dynamic Amplifier. *Tang, X., +, JSSC Dec. 2020 3248-3259*
- A 14-bit 4-MS/s VCO-Based SAR ADC With Deep Metastability Facilitated Mismatch Calibration. *Zhu, Z., +, JSSC June 2020 1565-1576*
- A 1770- μ m² Leakage-Based Digital Temperature Sensor With Supply Sensitivity Suppression in 55-nm CMOS. *Tang, Z., +, JSSC March 2020 781-793*
- A 39-GHz 64-Element Phased-Array Transceiver With Built-In Phase and Amplitude Calibrations for Large-Array 5G NR in 65-nm CMOS. *Wang, Y., +, JSSC May 2020 1249-1269*
- A 4-GHz Sub-Harmonically Injection-Locked Phase-Locked Loop With Self-Calibrated Injection Timing and Pulsewidth. *Jin, X., +, JSSC Oct. 2020 2724-2733*
- A 5-GS/s 158.6-mW 9.4-ENOB Passive-Sampling Time-Interleaved Three-Stage Pipelined-SAR ADC With Analog-Digital Corrections in 28-nm CMOS. *Ramkaj, A.T., +, JSSC June 2020 1553-1564*
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- A 7-bit 900-MS/s 2-Then-3-bit/cycle SAR ADC With Background Offset Calibration. *Li, D., +, JSSC Nov. 2020 3051-3063*
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- A CMOS Temperature Stabilized 2-D Mechanical Stress Sensor With 11-bit Resolution. *Nurmetov, U., +, JSSC April 2020 846-855*
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- A Wide-Range Variation-Resilient Physically Unclonable Function in 28 nm. *Liang, Z., +, JSSC March 2020 817-825*
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- Cameras**
- A 64-Pixel 0.42-THz Source SoC With Spatial Modulation Diversity for Computational Imaging. *Jain, R., +, JSSC Dec. 2020 3281-3293*
- Cancer**
- A Millimeter-Scale Single Charged Particle Dosimeter for Cancer Radiotherapy. *Lee, K., +, JSSC Nov. 2020 2947-2958*
- Capacitance**
- A 4-GS/s 39.9-dB SNDR 11.7-mW Hybrid Voltage-Time Two-Step ADC With Feedforward Ring Oscillator-Based TDCs. *Lyu, Y., +, JSSC July 2020 1807-1818*
- A Monolithic Resonant Switched-Capacitor Voltage Regulator With Dual-Phase Merged-LC Resonator. *McLaughlin, P.H., +, JSSC Dec. 2020 3179-3188*
- Capacitance measurement**
- A 2-in-1 Temperature and Humidity Sensor With a Single FLL Wheatstone-Bridge Front-End. *Jiang, H., +, JSSC Aug. 2020 2174-2185*
- Capacitive sensors**
- A 2-in-1 Temperature and Humidity Sensor With a Single FLL Wheatstone-Bridge Front-End. *Jiang, H., +, JSSC Aug. 2020 2174-2185*
- A 22- $\text{ng}/\sqrt{\text{Hz}}$ 17-mW Capacitive MEMS Accelerometer With Electrically Separated Mass Structure and Digital Noise-Reduction Techniques. *Furabayashi, Y., +, JSSC Sept. 2020 2539-2552*
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- Bandwidth-Enhanced Oversampling Successive Approximation Readout Technique for Low-Noise Power-Efficient MEMS Capacitive Accelerometer. *Zhong, L., +, JSSC Sept. 2020 2529-2538*
- Capacitive transducers**
- A 2-in-1 Temperature and Humidity Sensor With a Single FLL Wheatstone-Bridge Front-End. *Jiang, H., +, JSSC Aug. 2020 2174-2185*
- Capacitors**
- A 5.2-Mpixel 88.4-dB DR 12-in CMOS X-Ray Detector With 16-bit Column-Parallel Continuous-Time Incremental $\Delta\Sigma$ ADCs. *Lee, S., +, JSSC Nov. 2020 2878-2888*
- A 5.6 μ A Wide Bandwidth, High Power Supply Rejection Linear Low-Dropout Regulator With 68 dB of PSR Up To 2 MHz. *Joshi, K., +, JSSC Aug. 2020 2151-2160*
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- A Fully Integrated Multilevel Synchronized-Switch-Harvesting-on-Capacitors Interface for Generic PEHs. *Angelov, P., +, JSSC Aug. 2020 2118-2128*
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- A Three-Level Boost Converter With Full-Range Auto-Capacitor-Compensation Pulse Frequency Modulation. *Liu, W.C., +, JSSC March 2020 744-755*
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- Cardiology**
- A 0.5-V Sub-10- μ W 15.28-m $\Omega/\sqrt{\text{Hz}}$ Bio-Impedance Sensor IC With Sub-1° Phase Error. *Kim, K., +, JSSC Aug. 2020 2161-2173*
- Carrier transmission on power lines**
- A 161-mW 56-Gb/s ADC-Based Discrete Multitone Wireline Receiver Data-Path in 14-nm FinFET. *Kim, G., +, JSSC Jan. 2020 38-48*
- Catheters**
- A 64-Channel Transmit Beamformer With ±30-V Bipolar High-Voltage Pulses for Catheter-Based Ultrasound Probes. *Tan, M., +, JSSC July 2020 1796-1806*
- Cellular biophysics**
- The Design of a CMOS Nanoelectrode Array With 4096 Current-Clamp/Voltage-Clamp Amplifiers for Intracellular Recording/Stimulation of Mammalian Neurons. *Abbott, J., +, JSSC Sept. 2020 2567-2582*

Cellular radio

- A Cellular Multiband DTC-Based Digital Polar Transmitter With -153 -dBc/
Hz Noise in 14-nm FinFET. *Madoglio, P., +, JSSC July 2020 1830-1841*
NB-IoT and GNSS All-In-One System-On-Chip Integrating RF Transceiver,
23-dBm CMOS Power Amplifier, Power Management Unit, and Clock
Management System for Low Cost Solution. *Lee, J., +, JSSC Dec. 2020*
3400-3413

Channel coding

- An ISI-Resilient Data Encoding for Equalizer-Free Wireline Communication—
Decode Encoding and Error Correction for 24.2-dB Loss With 2.56
pJ/bit. *Chun, Y., +, JSSC March 2020 567-579*

Charge injection

- An All-Digital, V_{MAX} -Compliant, Stable, and Scalable Distributed Charge
Injection Scheme in 10-nm CMOS for Fast and Local Mitigation of Volt-
age Droop. *Bang, S., +, JSSC July 2020 1898-1908*

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- A 0.65-V 12–16-GHz Sub-Sampling PLL With 56.4-fs_{rms} Integrated Jitter and
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A 7-nm FinFET CMOS PLL With 388-fs Jitter and −80-dBc Reference Spur
Featuring a Track-and-Hold Charge Pump and Automatic Loop Gain Control. *Ko, C., +, JSSC April 2020 1043-1050*
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Spread-Spectrum Clock Generator. *Sun, H., +, JSSC Feb. 2020 426-438*
A Dynamically High-Impedance Charge-Pump-Based LDO With Digi-
tal-LDO-Like Properties Achieving a Sub-4-fs FoM. *Wang, X., +, JSSC*
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- A Self-Tuning IoT Processor Using Leakage-Ratio Measurement for Ener-
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- A Sub-mW 2.4-GHz Active-Mixer-Adopted Sub-Sampling PLL Achieving
an FoM of −256 dB. *Lee, D., +, JSSC June 2020 1542-1552*

- Distributed Network of LDO Microregulators Providing Submicrosecond
DVFS and IR Drop Compensation for a 24-Core Microprocessor in 14-nm
SOI CMOS. *Perez, M.E., +, JSSC March 2020 731-743*

Chemical variables measurement

- 50nW Opamp-Less $\Delta\Sigma$ -Modulated Bioimpedance Spectrum Analyzer for
Electrochemical Brain Interfacing. *ElAnsary, M., +, JSSC July 2020 1971-1983*

Chip scale packaging

- A 7-nm 4-GHz Arm¹-Core-Based CoWoS¹ Chiplet Design for High-Perfor-
mance Computing. *Lin, M., +, JSSC April 2020 956-966*

Chirp modulation

- A 4TX/4RX Pulsed Chirping Phased-Array Radar Transceiver in 65-nm
CMOS for X-Band Synthetic Aperture Radar Application. *Tang, K., +,*
JSSC Nov. 2020 2970-2983

Choppers (circuits)

- A 1.8-GHz Near-Field Dielectric Plethysmography Heart-Rate Sensor With
Time-Based Edge Sampling. *Chien, J., JSSC March 2020 615-628*

- A Code-Domain RF Signal Processing Front End With High Self-Inter-
ference Rejection and Power Handling for Simultaneous Transmit and
Receive. *Alshammary, H., +, JSSC May 2020 1199-1211*

Circuit feedback

- A 22.3-nW, 4.55 cm² Temperature-Robust Wake-Up Receiver Achieving a
Sensitivity of -69.5 dBm at 9 GHz. *Jiang, H., +, JSSC June 2020 1530-1541*

- A Multiband FDD SAW-Less Transmitter for 5G-NR Featuring a BW-Ex-
tended N -Path Filter-Modulator, a Switched-BB Input, and a Wideband
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- An OTA-Less Second-Order VCO-Based CT $\Sigma\Delta$ Modulator Using an Inher-
ent Passive Integrator and Capacitive Feedback. *Li, S., +, JSSC May 2020*
1337-1350

- Analysis and Design of a 260-MHz RF Bandwidth +22-dBm OOB-IIP3
Mixer-First Receiver With Third-Order Current-Mode Filtering TIA. *Pini,
G., +, JSSC July 2020 1819-1829*

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A Fully Passive RF Front End With 13-dB Gain Exploiting Implicit Capacitive Stacking in a Bottom-Plate N-Path Filter/Mixer. *Purushothaman, V.K., +, JSSC May 2020 1139-1150*

Mixer-First MIMO Receiver With Reconfigurable Multi-Port Decoupling and Matching. *Wilson, C., +, JSSC May 2020 1401-1410*

Microwave oscillators

A 12-mW 10-GHz FMCW PLL Based on an Integrating DAC With 28-kHz RMS-Frequency-Error for 23-MHz/ μ s Slope and 1.2-GHz Chirp-Bandwidth. *Renukaswamy, P.T., +, JSSC Dec. 2020 3294-3307*

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A Low-Noise Frequency Synthesizer Using Multiphase Generation and Combining Techniques. *Khashaba, A., +, JSSC March 2020 592-601*

An mm-Wave Synthesizer With Robust Locking Reference-Sampling PLL and Wide-Range Injection-Locked VCO. *Liao, D., +, JSSC March 2020 536-546*

Analysis and Design of a 17-GHz All-*n-pn* Push-Pull Class-C VCO. *Veni, S., +, JSSC Sept. 2020 2345-2355*

Design and Analysis of a Microwave-Optical Dual Modality Biomolecular Sensing Platform. *Zhang, L., +, JSSC March 2020 639-649*

Microwave photonics

A 0.46-THz 25-Element Scalable and Wideband Radiator Array With Optimized Lens Integration in 65-nm CMOS. *Jalili, H., +, JSSC Sept. 2020 2387-2400*

Microwave power amplifiers

A 28 GHz Single-Input Linear Chireix (SILC) Power Amplifier in 130 nm SiGe Technology. *Rabet, B., +, JSSC June 2020 1482-1490*

Microwave receivers

A 24.5–43.5-GHz Ultra-Compact CMOS Receiver Front End With Calibration-Free Instantaneous Full-Band Image Rejection for Multiband 5G Massive MIMO. *Huang, M., +, JSSC May 2020 1177-1186*

Microwave resonators

A 20-GHz 1.9-mW LNA Using g_m -Boost and Current-Reuse Techniques in 65-nm CMOS for Satellite Communications. *Zhang, J., +, JSSC Oct. 2020 2714-2723*

Microwave switches

A 24.5–43.5-GHz Ultra-Compact CMOS Receiver Front End With Calibration-Free Instantaneous Full-Band Image Rejection for Multiband 5G Massive MIMO. *Huang, M., +, JSSC May 2020 1177-1186*

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Millimeter wave antenna arrays

A 28-GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR. *Pang, J., +, JSSC Sept. 2020 2371-2386*

A 39-GHz 64-Element Phased-Array Transceiver With Built-In Phase and Amplitude Calibrations for Large-Array 5G NR in 65-nm CMOS. *Wang, Y., +, JSSC May 2020 1249-1269*

A 64-Pixel 0.42-THz Source SoC With Spatial Modulation Diversity for Computational Imaging. *Jain, R., +, JSSC Dec. 2020 3281-3293*

A CMOS Two-Element 170-GHz Fundamental-Frequency Transmitter With Direct RF-8PSK Modulation. *Nazari, P., +, JSSC Feb. 2020 282-297*

A Reconfigurable Hybrid Series/Parallel Doherty Power Amplifier With Antenna VSWR Resilient Performance for MIMO Arrays. *Mannem, N.S., +, JSSC Dec. 2020 3335-3348*

Antenna Preprocessing and Element-Pattern Shaping for Multi-Band mmWave Arrays: Multi-Port Transmitters and Antennas. *Chappidi, C.R., +, JSSC June 2020 1441-1454*

Code-Domain Multiplexing for Shared IF/LO Interfaces in Millimeter-Wave MIMO Arrays. *Johnson, M., +, JSSC May 2020 1270-1281*

Millimeter wave antennas

Multi-Feed Antenna and Electronics Co-Design: An E-Band Antenna-LNA Front End With On-Antenna Noise-Canceling and G_m -Boosting. *Li, S., +, JSSC Dec. 2020 3362-3375*

Millimeter wave bipolar transistors

3.2-mW Ultra-Low-Power 173–207-GHz Amplifier With 130-nm SiGe HBTs Operating in Saturation. *Zhang, Y., +, JSSC June 2020 1471-1481*

Millimeter wave communication

A 250-mW 60-GHz CMOS Transceiver SoC Integrated With a Four-Element AiP Providing Broad Angular Link Coverage. *Sadhu, B., +, JSSC June 2020 1516-1529*

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Analysis of a 28-nm CMOS Fast-Lock Bang-Bang Digital PLL With 220-fs RMS Jitter for Millimeter-Wave Communication. *Tsai, C., +, JSSC July 2020 1854-1863*

Code-Domain Multiplexing for Shared IF/LO Interfaces in Millimeter-Wave MIMO Arrays. *Johnson, M., +, JSSC May 2020 1270-1281*

Millimeter wave couplers

A Coupler-Based Differential mm-Wave Doherty Power Amplifier With Impedance Inverting and Scaling Baluns. *Nguyen, H.T., +, JSSC May 2020 1212-1223*

Millimeter wave frequency converters

A Fully Integrated 0.27-THz Injection-Locked Frequency Synthesizer With Frequency-Tracking Loop in 65-nm CMOS. *Liu, X., +, JSSC April 2020 1051-1063*

Millimeter wave imaging

A 24.5–43.5-GHz Ultra-Compact CMOS Receiver Front End With Calibration-Free Instantaneous Full-Band Image Rejection for Multiband 5G Massive MIMO. *Huang, M., +, JSSC May 2020 1177-1186*

Millimeter wave integrated circuits

A 230-GHz High-Power and Wideband Coupled Standing Wave VCO in 65-nm CMOS. *Jalili, H., +, JSSC March 2020 547-556*

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Millimeter wave mixers

300-GHz-Band 120-Gb/s Wireless Front-End Based on InP-HEMT PAs and Mixers. *Hamada, H., +, JSSC Sept. 2020 2316-2335*

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Millimeter wave oscillators

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Millimeter wave phase shifters

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A 30-GHz CMOS SOI Outphasing Power Amplifier With Current Mode Combining for High Backoff Efficiency and Constant Envelope Operation. *Ning, K., +, JSSC May 2020 1411-1421*

A 4TX/4RX Pulsed Chirping Phased-Array Radar Transceiver in 65-nm CMOS for X-Band Synthetic Aperture Radar Application. *Tang, K., +, JSSC Nov. 2020 2970-2983*

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MMIC

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Multi-Mode 60-GHz Radar Transmitter SoC in 45-nm SOI CMOS. *Lee, W., +, JSSC May 2020 1187–1198*

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A 2.92-Gb/s/W and 0.43-Gb/s/MG Flexible and Scalable CGRA-Based Baseband Processor for Massive MIMO Detection. *Peng, G., +, JSSC Feb. 2020 505–519*

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Integrated Self-Adaptive and Power-Scalable Wideband Interference Cancellation for Full-Duplex MIMO Wireless. *Cao, Y., +, JSSC Nov. 2020 2984–2996*

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MIMO radar

A CMOS 76–81-GHz 2-TX 3-RX FMCW Radar Transceiver Based on Mixed-Mode PLL Chirp Generator. *Ma, T., +, JSSC Feb. 2020 233–248*

Minimization

OPTIMO: A 65-nm 279-GOPS/W 16-b Programmable Spatial-Array Processor with On-Chip Network for Solving Distributed Optimizations via the Alternating Direction Method of Multipliers. *Chang, M., +, JSSC March 2020 629–638*

Mixed analog digital integrated circuits

A Fully Dynamic Multi-Mode CMOS Vision Sensor With Mixed-Signal Cooperative Motion Sensing and Object Segmentation for Adaptive Edge Computing. *Zhong, X., +, JSSC June 2020 1684–1697*

C3SRAM: An In-Memory-Computing SRAM Macro Based on Robust Capacitive Coupling Computing Mechanism. *Jiang, Z., +, JSSC July 2020 1888–1897*

XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks. *Yin, S., +, JSSC June 2020 1733–1743*

Mixers (circuits)

A Low-Power Backscatter Modulation System Communicating Across Tens of Meters With Standards-Compliant Wi-Fi Transceivers. *Wang, P.P., +, JSSC Nov. 2020 2959–2969*

Breaking the Performance Tradeoffs in N-Path Mixer-First Receivers Using a Second-Order Baseband Noise-Canceling TIA. *Sharma, P.K., +, JSSC Nov. 2020 3009–3023*

Design and Analysis of Enhanced Mixer-First Receivers Achieving 40-dB/decade RF Selectivity. *Krishnamurthy, S., +, JSSC May 2020 1165–1176*
Integrated Self-Adaptive and Power-Scalable Wideband Interference Cancellation for Full-Duplex MIMO Wireless. *Cao, Y., +, JSSC Nov. 2020 2984–2996*

MMIC

A 14-GHz Bang-Bang Digital PLL With Sub-150-fs Integrated Jitter for Wireline Applications in 7-nm FinFET CMOS. *Pfaff, D., +, JSSC March 2020 580–591*

A Wideband Low-Power Cryogenic CMOS Circulator for Quantum Applications. *Ruffino, A., +, JSSC May 2020 1224–1238*

MMIC amplifiers

A 1.7-dB Minimum NF, 22–32-GHz Low-Noise Feedback Amplifier With Multistage Noise Matching in 22-nm FD-SOI CMOS. *Cui, B., +, JSSC May 2020 1239–1248*

Baseband to 140-GHz SiGe HBT and 100-GHz InP DHBT Broadband Triple-Stacked Distributed Amplifiers With Active Bias Terminations. *Kobayashi, K.W., +, JSSC Sept. 2020 2336–2344*

MMIC mixers

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MMIC oscillators

A 4-GHz Sub-Harmonically Injection-Locked Phase-Locked Loop With Self-Calibrated Injection Timing and Pulsewidth. *Jin, X., +, JSSC Oct. 2020 2742–2743*

MMIC power amplifiers

A 21-dm_{OP1} dB 20.3%-Efficiency $-131.8\text{-dBm}/\text{Hz}$ -Noise X-Band Cartesian Error Feedback Transmitter With Fully Integrated Power Amplifier in 65-nm CMOS. *Li, J., +, JSSC June 2020 1491–1501*

A Broadband Switched-Transformer Digital Power Amplifier for Deep Back-Off Efficiency Enhancement. *Yin, Y., +, JSSC Nov. 2020 2997–3008*
Highly Linear High-Power 802.11ac/ax WLAN SiGe HBT Power Amplifiers With a Compact 2nd-Harmonic-Shorted Four-Way Transformer and a Thermally Compensating Dynamic Bias Circuit. *Ju, I., +, JSSC Sept. 2020 2356–2370*

Mobile computing

A 65-nm Neuromorphic Image Classification Processor With Energy-Efficient Training Through Direct Spike-Only Feedback. *Park, J., +, JSSC Jan. 2020 108–119*

Vocell: A 65-nm Speech-Triggered Wake-Up SoC for 10- μW Keyword Spotting and Speaker Verification. *Giraldo, J.S.P., +, JSSC April 2020 868–878*

Mobile radio

A 6.5–8.1-GHz Communication/Ranging VWB Transceiver for Secure Wireless Connectivity With Enhanced Bandwidth Efficiency and $\Sigma\Delta$ Energy Detection. *Song, H., +, JSSC Feb. 2020 219–232*

Catena: A Near-Threshold, Sub-0.4-mW, 16-Core Programmable Spatial Array Accelerator for the Ultralow-Power Mobile and Embedded Internet of Things. *Cerqueira, J.P., +, JSSC Aug. 2020 2270–2284*

Mobile robots

A 65-nm 8-to-3-b 1.0–0.36-V 9.1–1.1-TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Swarm Robotics. *Cao, N., +, JSSC Jan. 2020 49–59*

Modal analysis

Design and Analysis of a Microwave-Optical Dual Modality Biomolecular Sensing Platform. *Zhang, L., +, JSSC March 2020 639–649*

Modulation

Indirect Time-of-Flight CMOS Image Sensor With On-Chip Background Light Cancelling and Pseudo-Four-Tap/Two-Tap Hybrid Imaging for Motion Artifact Suppression. *Kim, D., +, JSSC Nov. 2020 2849–2865*

Modulators

A 0.032-mm² 43.3-fJ/Step 100–200-MHz IF 2-MHz Bandwidth Bandpass DSM Based on Passive N-Path Filters. *Zhang, Y., +, JSSC Sept. 2020 2443–2455*

A 50-Gb/s PAM4 Si-Photonic Transmitter With Digital-Assisted Distributed Driver and Integrated CDR in 40-nm CMOS. *Liao, Q., +, JSSC May 2020 1282-1296*

A Highly Linear OTA-Less 1-1 MASH VCO-Based $\Sigma\Delta$ ADC With an Efficient Phase Quantization Noise Extraction Technique. *Maghami, H., +, JSSC March 2020 706-718*

A Multiband FDD SAW-Less Transmitter for 5G-NR Featuring a BW-Extended N -Path Filter-Modulator, a Switched-BB Input, and a Wideband TIA-Based PA Driver. *Qi, G., +, JSSC Dec. 2020 3387-3399*

An Event-Driven Quasi-Level-Crossing Delta Modulator Based on Residue Quantization. *Wang, H., +, JSSC Feb. 2020 298-311*

Molecular biophysics

Design and Analysis of a Microwave-Optical Dual Modality Biomolecular Sensing Platform. *Zhang, L., +, JSSC March 2020 639-649*

Monopole antenna arrays

Mixer-First MIMO Receiver With Reconfigurable Multi-Port Decoupling and Matching. *Wilson, C., +, JSSC May 2020 1401-1410*

MOS integrated circuits

A 1.02-pJ/b 20.83-Gb/s/Wire USR Transceiver Using CNRZ-5 in 16-nm FinFET. *Tajalli, A., +, JSSC April 2020 1108-1123*

MOSFET

A 12-b 18-GS/s RF Sampling ADC With an Integrated Wideband Track-and-Hold Amplifier and Background Calibration. *Ali, A.M.A., +, JSSC Dec. 2020 3210-3224*

A 64-Channel Transmit Beamformer With ± 30 -V Bipolar High-Voltage Pulsers for Catheter-Based Ultrasound Probes. *Tan, M., +, JSSC July 2020 1796-1806*

High-Value Tunable Pseudo-Resistors Design. *Guglielmi, E., +, JSSC Aug. 2020 2094-2105*

MOSFET circuits

112-Gb/s PAM4 ADC-Based SERDES Receiver With Resonant AFE for Long-Reach Channels. *Krupnik, Y., +, JSSC April 2020 1077-1085*

A 243-mW 1.25–56-Gb/s Continuous Range PAM-4 42.5-dB IL ADC/DAC-Based Transceiver in 7-nm FinFET. *Pisati, M., +, JSSC Jan. 2020 6-18*

A 7-nm FinFET CMOS PLL With 388-fs Jitter and ~ 80 -dBc Reference Spur Featuring a Track-and-Hold Charge Pump and Automatic Loop Gain Control. *Ko, C., +, JSSC April 2020 1043-1050*

A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons. *Van Dijk, J.P.G., +, JSSC Nov. 2020 2930-2946*

Motion measurement

Indirect Time-of-Flight CMOS Image Sensor With On-Chip Background Light Cancelling and Pseudo-Four-Tap/Two-Tap Hybrid Imaging for Motion Artifact Suppression. *Kim, D., +, JSSC Nov. 2020 2849-2865*

Multi-robot systems

A 65-nm 8-to-3-b 1.0–0.36-V 9.1–1.1-TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Swarm Robotics. *Cao, N., +, JSSC Jan. 2020 49-59*

Multichip modules

A 0.32–128 TOPS, Scalable Multi-Chip-Module-Based Deep Neural Network Inference Accelerator With Ground-Referenced Signaling in 16 nm. *Zimmer, B., +, JSSC April 2020 920-932*

A 1.02-pJ/b 20.83-Gb/s/Wire USR Transceiver Using CNRZ-5 in 16-nm FinFET. *Tajalli, A., +, JSSC April 2020 1108-1123*

A 2×30 k-Spin Multi-Chip Scalable CMOS Annealing Processor Based on a Processing-in-Memory Approach for Solving Large-Scale Combinatorial Optimization Problems. *Takemoto, T., +, JSSC Jan. 2020 145-156*

Multilayer perceptrons

Tianjic: A Unified and Scalable Chip Bridging Spike-Based and Continuous Neural Computation. *Deng, L., +, JSSC Aug. 2020 2228-2246*

Multiplexing

A Beyond-1-Tb/s Coherent Optical Transmitter Front-End Based on 110-GHz-Bandwidth 2:1 Analog Multiplexer in 250-nm InP DHBT. *Nagatani, M., +, JSSC Sept. 2020 2301-2315*

Analysis and Design of a Robust, Low-Power, Inductively Coupled LSK Data Link. *Yousefi, A., +, JSSC Sept. 2020 2583-2596*

Wireless Body-Area-Network Transceiver and Low-Power Receiver With High Application Expandability. *Jang, J., +, JSSC Oct. 2020 2781-2789*

Multiplexing equipment

A 50–112-Gb/s PAM-4 Transmitter With a Fractional-Spaced FFE in 65-nm CMOS. *Zheng, X., +, JSSC July 2020 1864-1876*

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Multiplying circuits

A 28-nm Compute SRAM With Bit-Serial Logic/Arithmetic Operations for Programmable In-Memory Vector Computing. *Wang, J., +, JSSC Jan. 2020 76-86*

Multiprocessing systems

A 20.5 TOPS Multicore SoC With DNN Accelerator and Image Signal Processor for Automotive Applications. *Yamada, Y., +, JSSC Jan. 2020 120-132*

A 7.3 M Output Non-Zeros/J, 11.7 M Output Non-Zeros/GB Reconfigurable Sparse Matrix–Matrix Multiplication Accelerator. *Park, D., +, JSSC April 2020 933-944*

OPTIMO: A 65-nm 279-GOPS/W 16-b Programmable Spatial-Array Processor with On-Chip Network for Solving Distributed Optimizations via the Alternating Direction Method of Multipliers. *Chang, M., +, JSSC March 2020 629-638*

Muscles

A 1–10-MHz Frequency-Aware CMOS Active Rectifier With Dual-Loop Adaptive Delay Compensation and >230 -mW Output Power for Capacitively Powered Biomedical Implants. *Erfani, R., +, JSSC March 2020 756-766*

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NAND circuits

Privacy Protection NAND Flash System With Flexible Data-Lifetime Control by In-3-D Vertical Cell Processing. *Suzuki, S., +, JSSC Oct. 2020 2802-2809*

Nanogenerators

A High-Voltage Dual-Input Buck Converter Achieving 52.9% Maximum End-to-End Efficiency for Triboelectric Energy-Harvesting Applications. *Park, I., +, JSSC May 2020 1324-1336*

Nanowires

A 0.3 lx–1.4 Mlx Monolithic Silicon Nanowire Light-to-Digital Converter With Temperature-Independent Offset Cancellation. *Rhee, C., +, JSSC Feb. 2020 378-391*

Near-field communication

A Batteryless Padless Crystallless $116 \mu\text{m} \times 116 \mu\text{m}$ “Dielet” Near-Field Radio With On-Chip Coil Antenna. *Zhao, B., +, JSSC Feb. 2020 249-260*

Network routing

A 1.02-pJ/b 20.83-Gb/s/Wire USR Transceiver Using CNRZ-5 in 16-nm FinFET. *Tajalli, A., +, JSSC April 2020 1108-1123*

Network synthesis

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Network-on-chip

A 0.32–128 TOPS, Scalable Multi-Chip-Module-Based Deep Neural Network Inference Accelerator With Ground-Referenced Signaling in 16 nm. *Zimmer, B., +, JSSC April 2020 920-932*

Neural chips

A 0.32–128 TOPS, Scalable Multi-Chip-Module-Based Deep Neural Network Inference Accelerator With Ground-Referenced Signaling in 16 nm. *Zimmer, B., +, JSSC April 2020 920-932*

A 12.08-TOPS/W All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy Efficient Edge Computing. *Sayal, A., +, JSSC Jan. 2020 60-75*

A 65-nm Neuromorphic Image Classification Processor With Energy-Efficient Training Through Direct Spike-Only Feedback. *Park, J., +, JSSC Jan. 2020 108-119*

A Twin-8T SRAM Computation-in-Memory Unit-Macro for Multibit CNN-Based AI Edge Processors. *Si, X., +, JSSC Jan. 2020 189-202*

Embedded 1-Mb ReRAM-Based Computing-in-Memory Macro With Multibit Input and Weight for CNN-Based AI Edge Processors. *Xue, C., +, JSSC Jan. 2020 203-215*

Track-and-Zoom Neural Analog-to-Digital Converter With Blind Stimulation Artifact Rejection. *Reza Pazhouhandeh, M., +, JSSC July 2020 1984-1997*

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Neural networks

A 20.5 TOPS Multicore SoC With DNN Accelerator and Image Signal Processor for Automotive Applications. *Yamada, Y., +, JSSC Jan. 2020 120-132*

An Adaptive Clock Scheme Exploiting Instruction-Based Dynamic Timing Slack for a GPGPU Architecture. *Jia, T., +, JSSC Aug. 2020 2259-2269*

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- Photodetectors**
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- Piezoelectric transducers**
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- Tianjic: A Unified and Scalable Chip Bridging Spike-Based and Continuous Neural Computation. *Deng, L., +, JSSC Aug. 2020 2228-2246*
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A Three-Level Boost Converter With Full-Range Auto-Capacitor-Compensation Pulse Frequency Modulation. *Liu, W.C., +, JSSC March 2020 744-755*

Power dividers

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Power factor

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Power inductors

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Power transistors

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Quadrature phase shift keying

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Quantum optics

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Radar computing

A Time Domain Artificial Intelligence Radar System Using 33-GHz Direct Sampling for Hand Gesture Recognition. *Park, J., +, JSSC April 2020 879-888*

Radar detection

A 4-GS/s 80-dB DR Current-Domain Analog Frontend for Phase-Coded Pulse-Compression Direct Time-of-Flight Automotive Lidar. *Kashmiri, M., +, JSSC Dec. 2020 3131-3145*

Radar imaging

A 4TX/4RX Pulsed Chirping Phased-Array Radar Transceiver in 65-nm CMOS for X-Band Synthetic Aperture Radar Application. *Tang, K., +, JSSC Nov. 2020 2970-2983*

Radar receivers

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Radar resolution

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Radar signal processing

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Radar transmitters

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A 0.46-THz 25-Element Scalable and Wideband Radiator Array With Optimized Lens Integration in 65-nm CMOS. *Jalili, H., +, JSSC Sept. 2020 2387-2400*

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