

# 2019 Index

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This index covers all technical items—papers, correspondence, reviews, etc.—that appeared in this periodical during 2019, and items from previous years that were commented upon or corrected in 2019. Departments and other items may also be covered if they have been judged to have archival value.

The Author Index contains the primary entry for each item, listed under the first author's name. The primary entry includes the coauthors' names, the title of the paper or other item, and its location, specified by the publication abbreviation, year, month, and inclusive pagination. The Subject Index contains entries describing the item under all appropriate subject headings, plus the first author's name, the publication abbreviation, month, and year, and inclusive pages. Note that the item title is found only under the primary entry in the Author Index.

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Design of an Always-On Deep Neural Network-Based 1- $\mu$ W Voice Activity Detector Aided With a Customized Software Model for Analog Feature Extraction. *Yang, M.*, +, *JSSC June 2019 1764-1777*

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A 1-mW Class-AB Amplifier With  $-101$  dB THD+N for High-Fidelity 16  $\Omega$  Headphones in 65-nm CMOS. *Mehta, N.*, +, *JSSC April 2019 948-958*

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A 0.34-THz Wideband Wide-Angle 2-D Steering Phased Array in 0.13- $\mu$ m SiGe BiCMOS. *Jalili, H.*, +, *JSSC Sept. 2019 2449-2461*

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A 1-pJ/bit 80-Gb/s 2<sup>15</sup>-1 PRBS Generator With a Modified Cherry-Hooper Output Driver. *Khafaji, M.M.*, +, *JSSC July 2019 2059-2069*

**BiCMOS analog integrated circuits**

A 28-/37-/39-GHz Linear Doherty Power Amplifier in Silicon for 5G Applications. *Hu, S.*, +, *JSSC June 2019 1586-1599*

**BiCMOS integrated circuits**

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A Wireless Multi-Channel Peripheral Nerve Signal Acquisition System-on-Chip. *Ng, K.A.*, +, *JSSC Aug. 2019 2266-2280*

**Bioelectric potentials**

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**Biological techniques**

A CMOS Electrochemical Biochip With  $32 \times 32$  Three-Electrode Voltammetry Pixels. *Manickam, A.*, +, *JSSC Nov. 2019 2980-2990*

**Biological tissues**

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**Biomedical communication**

A Four-Camera VGA-Resolution Capsule Endoscope System With 80-Mb/s Body Channel Communication Transceiver and Sub-Centimeter Range Capsule Localization. *Jang, J.*, +, *JSSC Feb. 2019 538-549*

BodyWire: A 6.3-pJ/b 30-Mb/s  $-30$ -dB SIR-Tolerant Broadband Interference-Robust Human Body Communication Transceiver Using Time Domain Interference Rejection. *Maity, S.*, +, *JSSC Oct. 2019 2892-2906*

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A 0.8-V 82.9- $\mu\text{W}$  In-Ear BCI Controller IC With 8.8 PEF EEG Instrumentation Amplifier and Wireless BAN Transceiver. *Lee, J.*, +, *JSSC April 2019 1185-1195*

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A Wireless Multi-Channel Peripheral Nerve Signal Acquisition System-on-Chip. *Ng, K.A.*, +, *JSSC Aug. 2019 2266-2280*

**Biomedical optical imaging**

A  $192 \times 128$  Time Correlated SPAD Image Sensor in 40-nm CMOS Technology. *Henderson, R.K.*, +, *JSSC July 2019 1907-1916*

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A Sub- $\text{mm}^3$  Ultrasonic Free-Floating Implant for Multi-Mote Neural Recording. *Ghanbari, M.M.*, +, *JSSC Nov. 2019 3017-3030*

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A 1.06- $\mu\text{W}$  Smart ECG Processor in 65-nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring. *Yin, S.*, +, *JSSC Aug. 2019 2316-2326*

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A 232-1996-kS/s Robust Compressive Sensing Reconstruction Engine for Real-Time Physiological Signals Monitoring. *Chen, T.*, +, *JSSC Jan. 2019 307-317*

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- Boltzmann machines**
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- Broadband networks**
- Analysis and Design of Wideband I/Q CMOS 100–200 Gb/s Modulators. *Al-Rubaye, H., +, JSSC Sept. 2019 2361-2374*
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#### Capacitance measurement

A 0.1-nW–1- $\mu$ W Energy-Efficient All-Dynamic Versatile Capacitance-to-Digital Converter. *Xin, H.*, +, *JSSC July 2019 1841-1851*

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- 20-nm  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  MOSHEMT MMIC Technology on Silicon. *Tessmann, A., +, JSSC Sept. 2019 2411-2418*

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- A 232–1996-kS/s Robust Compressive Sensing Reconstruction Engine for Real-Time Physiological Signals Monitoring. *Chen, T., +, JSSC Jan. 2019 307-317*

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- An Energy-Efficient Graphics Processor in 14-nm Tri-Gate CMOS Featuring Integrated Voltage Regulators for Fine-Grain DVFS, Retentive Sleep, and  $V_{\text{MIN}}$  Optimization. *Meinerzhagen, P.A., +, JSSC Jan. 2019 144-157*

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- A 141- $\mu\text{W}$  High-Voltage MEMS Gyroscope Drive Interface Circuit Based on Flying Capacitors. *Marx, M., +, JSSC Feb. 2019 511-523*

**H****Hall effect transducers**

- A Fast T&H Overcurrent Detector for a Spinning Hall Current Sensor With Ping-Pong and Chopping Techniques. *Li, Y., +, JSSC July 2019 1852-1861*

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- A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range. *Kang, J., +, JSSC March 2019 865-873*

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- A General Theory of Injection Locking and Pulling in Electrical Oscillators—Part II: Amplitude Modulation in LC Oscillators, Transient Behavior, and Frequency Division. *Hong, B., +, JSSC Aug. 2019 2122-2139*

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- A 1-mW Class-AB Amplifier With  $-101$  dB THD+N for High-Fidelity 16  $\Omega$  Headphones in 65-nm CMOS. *Mehta, N., +, JSSC April 2019 948-958*

**HEMT integrated circuits**

- Broadband 240-GHz Radar for Non-Destructive Testing of Composite Materials. *Merkle, T., +, JSSC Sept. 2019 2388-2401*

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- A 1-mW Class-AB Amplifier With  $-101$  dB THD+N for High-Fidelity 16  $\Omega$  Headphones in 65-nm CMOS. *Mehta, N., +, JSSC April 2019 948-958*



**High electron mobility transistors**

20-nm In<sub>0.8</sub>Ga<sub>0.2</sub>As MOSHEMT MMIC Technology on Silicon. *Tessmann, A., +, JSSC Sept. 2019 2411-2418*

A Three-Stage 18.5–24-GHz GaN-on-SiC 4 W 40% Efficient MMIC PA. *Duffy, M.R., +, JSSC Sept. 2019 2402-2410*

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A Multi-Loop-Controlled AC-Coupling Supply Modulator With a Mode-Switching CMOS PA in an EER System With Envelope Shaping. *Liu, X., +, JSSC June 2019 1553-1563*

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**Humidity sensors**

A 2.92- $\mu$ W Capacitance-to-Digital Converter With Differential Bondwire Accelerometer, On-Chip Air Pressure, and Humidity Sensor in 0.18- $\mu$ m CMOS. *Park, S., +, JSSC Oct. 2019 2845-2856*

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A 135-mW 1.70TOPS Sparse Video Sequence Inference SoC for Action Classification. *Chen, T., +, JSSC July 2019 2081-2090*

An Always-On 3.8  $\mu$ J/86% CIFAR-10 Mixed-Signal Binary CNN Processor With All Memory on Chip in 28-nm CMOS. *Bankman, D., +, JSSC Jan. 2019 158-172*

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Dual-Tap Computational Photography Image Sensor With Per-Pixel Pipelined Digital Memory for Intra-Frame Coded Multi-Exposure. *Sarhangnejad, N., +, JSSC Nov. 2019 3191-3202*

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A 1920  $\times$  1080 25-Frames/s 2.4-TOPS/W Low-Power 6-D Vision Processor for Unified Optical Flow and Stereo Depth With Semi-Global Matching. *Li, Z., +, JSSC April 2019 1048-1058*

**Image motion analysis**

A 135-mW 1.70TOPS Sparse Video Sequence Inference SoC for Action Classification. *Chen, T., +, JSSC July 2019 2081-2090*

**Image recognition**

3-D NAND Flash Value-Aware SSD: Error-Tolerant SSD Without ECCs for Image Recognition. *Deguchi, Y., +, JSSC June 2019 1800-1811*

A Time-Domain Computing Accelerated Image Recognition Processor With Efficient Time Encoding and Non-Linear Logic Operation. *Chen, Z., +, JSSC Nov. 2019 3226-3237*

**Image reconstruction**

A 512-Pixel, 51-kHz-Frame-Rate, Dual-Shank, Lens-Less, Filter-Less Single-Photon Avalanche Diode CMOS Neural Imaging Probe. *Choi, J., +, JSSC Nov. 2019 2957-2968*

Dual-Tap Computational Photography Image Sensor With Per-Pixel Pipelined Digital Memory for Intra-Frame Coded Multi-Exposure. *Sarhangnejad, N., +, JSSC Nov. 2019 3191-3202*

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A 1920  $\times$  1080 25-Frames/s 2.4-TOPS/W Low-Power 6-D Vision Processor for Unified Optical Flow and Stereo Depth With Semi-Global Matching. *Li, Z., +, JSSC April 2019 1048-1058*

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**Image sampling**

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A Reconfigurable 3-D-Stacked SPAD Imager With In-Pixel Histogramming for Flash LIDAR or High-Speed Time-of-Flight Imaging. *Hutchings, S.W., +, JSSC Nov. 2019 2947-2956*

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A 135-mW 1.70TOPS Sparse Video Sequence Inference SoC for Action Classification. *Chen, T., +, JSSC July 2019 2081-2090*

A 1920  $\times$  1080 25-Frames/s 2.4-TOPS/W Low-Power 6-D Vision Processor for Unified Optical Flow and Stereo Depth With Semi-Global Matching. *Li, Z., +, JSSC April 2019 1048-1058*

**Impedance matching**

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20-nm In<sub>0.8</sub>Ga<sub>0.2</sub>As MOSHEMT MMIC Technology on Silicon. *Tessmann, A., +, JSSC Sept. 2019 2411-2418*

5–31-Hz 188- $\mu$ W Light-Sensing Oscillator With Two Active Inductors Fully Integrated on Plastic. *Meister, T., +, JSSC Aug. 2019 2195-2206*

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An Always-On 3.8  $\mu\text{J}/86\%$  CIFAR-10 Mixed-Signal Binary CNN Processor With All Memory on Chip in 28-nm CMOS. *Bankman, D.*, +, *JSSC Jan. 2019 158-172*

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A 0.53-THz Subharmonic Injection-Locked Phased Array With 63- $\mu\text{W}$  Radiated Power in 40-nm CMOS. *Guo, K.*, +, *JSSC Feb. 2019 380-391*

A 10-Gb/s, 0.03-mm<sup>2</sup>, 1.28-pJ/bit Half-Rate Injection-Locked CDR With Path Mismatch Tracking Loop in a 28-nm CMOS Technology. *Choo, M.*, +, *JSSC Oct. 2019 2812-2822*

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An Instruction-Driven Adaptive Clock Management Through Dynamic Phase Scaling and Compiler Assistance for a Low Power Microprocessor. *Jia, T.*, +, *JSSC Aug. 2019 2327-2338*

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A 7T-SRAM With Data-Write Technique by Capacitive Coupling. *Takashima, D.*, +, *JSSC Feb. 2019 596-605*

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#### Integrated circuit synthesis

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A 1–2 GHz Computational-Locking ADPLL With Sub-20-Cycle Locktime Across PVT Variation. *ur Rahman, F.*, +, *JSSC Sept. 2019 2487-2500*

A 1-mW Class-AB Amplifier With –101 dB THD+N for High-Fidelity 16  $\Omega$  Headphones in 65-nm CMOS. *Mehta, N.*, +, *JSSC April 2019 948-958*

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Self-Convergent Trimming SRAM True Random Number Generation With In-Cell Storage. *Yeh, P.*, +, *JSSC Sept. 2019 2614-2621*

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A 15-nW per Sensor Interference-Immune Readout IC for Capacitive Touch Sensors. *Hussaini, S.*, +, *JSSC July 2019 1874-1882*

#### Integrated memory circuits

Mr.Wolf: An Energy-Precision Scalable Parallel Ultra Low Power SoC for IoT Edge Processing. *Pullini, A.*, +, *JSSC July 2019 1970-1981*

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A 25-Gb/s, 2.1-pJ/bit, Fully Integrated Optical Receiver With a Baud-Rate Clock and Data Recovery. *Lee, Y.*, +, *JSSC Aug. 2019 2243-2254*

A Process and Temperature Insensitive CMOS Linear TIA for 100 Gb/s/  $\lambda$  PAM-4 Optical Links. *Lakshmi Kumar, K.R.*, +, *JSSC Nov. 2019 3180-3190*

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A 40-GHz Mirrored-Cascode Differential Transimpedance Amplifier in 65-nm CMOS. *Kim, S.G.*, +, *JSSC May 2019 1468-1474*

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A 47.14- $\mu$ W 200-MHz MOS/MTJ-Hybrid Nonvolatile Microcontroller Unit Embedding STT-MRAM and FPGA for IoT Applications. *Natsui, M.*, +, *JSSC Nov. 2019 2991-3004*

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A 0.6 V 1.63 fJ/c.-s. Detective Open-Loop Dynamic System Buffer for SAR ADC in Zero-Capacitor TDDI System. *Hu, Y.*, +, *JSSC Oct. 2019 2680-2690*

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A 0.1-nW–1- $\mu$ W Energy-Efficient All-Dynamic Versatile Capacitance-to-Digital Converter. *Xin, H.*, +, *JSSC July 2019 1841-1851*

A 16-nm Always-On DNN Processor With Adaptive Clocking and Multi-Cycle Banked SRAMs. *Lee, S.K.*, +, *JSSC July 2019 1982-1992*

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A Watt-Level Quadrature Class-G Switched-Capacitor Power Amplifier With Linearization Techniques. *Yoo, S.*, +, *JSSC May 2019 1274-1287*

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A 56-Gb/s PAM4 Receiver With Low-Overhead Techniques for Threshold and Edge-Based DFE FIR- and IIR-Tap Adaptation in 65-nm CMOS. *Roshan-Zamir, A.*, +, *JSSC March 2019 672-684*

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A 2.4-mm<sup>2</sup> 130-mW MMSE-Nonbinary LDPC Iterative Detector Decoder for  $4 \times 4$  256-QAM MIMO in 65-nm CMOS. *Tang, W.*, +, *JSSC July 2019 2070-2080*

**Iterative methods**

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**J****Jitter**

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**Optical fiber dispersion**

An Electronic Dispersion Compensation Transceiver for 10- and 28-Gb/s Directly Modulated Lasers-Based Optical Links. Kwon, K., +, *JSSC Jan. 2019 55-64*

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A 512-Pixel, 51-kHz-Frame-Rate, Dual-Shank, Lens-Less, Filter-Less Single-Photon Avalanche Diode CMOS Neural Imaging Probe. Choi, J., +, *JSSC Nov. 2019 2957-2968*

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34-Gb/s Linear Transimpedance Amplifier for 200-Gb/s DP-16-QAM Optical Coherent Receivers. Ahmed, M.G., +, *JSSC March 2019 834-844*

A 25-Gb/s Avalanche Photodetector-Based Burst-Mode Optical Receiver With 2.24-ns Reconfiguration Time in 28-nm CMOS. Chen, K.C., +, *JSSC June 2019 1682-1693*

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A Differential Optical Receiver With Monolithic Split-Microring Photodetector. *Mehta, N.*, +, *JSSC Aug. 2019 2230-2242*

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A 1.06- $\mu$ W Smart ECG Processor in 65-nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring. *Yin, S.*, +, *JSSC Aug. 2019 2316-2326*

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A CMOS MedRadio Transceiver With Supply-Modulated Power Saving Technique for an Implantable Brain-Machine Interface System. *Lee, M., +, JSSC June 2019 1541-1552*

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A 25-MHz Four-Phase SAW Hysteretic Control DC-DC Converter With 1-Cycle Active Phase Count. *Lee, B., +, JSSC June 2019 1755-1763*

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A 1.6-to-3.0-GHz Fractional- $N$  MDLL With a Digital-to-Time Converter Range-Reduction Technique Achieving 397-fs Jitter at 2.5-mW Power. *Santuccioli, A., +, JSSC Nov. 2019 3149-3160*

A 10-Gb/s, 0.03-mm<sup>2</sup>, 1.28-pJ/bit Half-Rate Injection-Locked CDR With Path Mismatch Tracking Loop in a 28-nm CMOS Technology. *Choo, M., +, JSSC Oct. 2019 2812-2822*

A 2.4-GHz Reference-Sampling Phase-Locked Loop That Simultaneously Achieves Low-Noise and Low-Spur Performance. *Sharma, J., +, JSSC May 2019 1407-1424*

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A 0.0056-mm<sup>2</sup>  $-249$ -dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs. *Yang, S., +, JSSC Jan. 2019 88-98*

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A 5.5-GHz Background-Calibrated Subsampling Polar Transmitter With  $-41.3$ -dB EVM at 1024 QAM in 28-nm CMOS. *Markulic, N., +, JSSC April 2019 1059-1073*

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A Self-Oscillating Boosting Amplifier With Adaptive Soft Switching Control for Piezoelectric Transducers. *Amir, S., +, JSSC Jan. 2019 253-265*

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An Instruction-Driven Adaptive Clock Management Through Dynamic Phase Scaling and Compiler Assistance for a Low Power Microprocessor. *Jia, T., +, JSSC Aug. 2019 2327-2338*

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A 2.92- $\mu\text{W}$  Capacitance-to-Digital Converter With Differential Bondwire Accelerometer, On-Chip Air Pressure, and Humidity Sensor in 0.18- $\mu\text{m}$  CMOS. *Park, S., +, JSSC Oct. 2019 2845-2856*

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A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS. *Yang, S., +, JSSC May 2019 1351-1362*

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**Power capacitors**

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A 14-nA, Highly Efficient Triple-Output Thermoelectric Energy Harvesting System Based on a Reconfigurable TEG Array. *Wan, Q., +, JSSC June 2019 1720-1732*

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An Energy Measurement Frontend With Integrated Adaptive Background Accuracy Monitoring of the Full System Including the Current and Voltage Sensors. *Danesh, S., +, JSSC Dec. 2019 3269-3280*

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#### Pressure measurement

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Improved Power/EM Side-Channel Attack Resistance of 128-Bit AES Engines With Random Fast Voltage Dithering. *Singh, A., +, JSSC Feb. 2019 569-583*

#### Program compilers

An Instruction-Driven Adaptive Clock Management Through Dynamic Phase Scaling and Compiler Assistance for a Low Power Microprocessor. *Jia, T., +, JSSC Aug. 2019 2327-2338*

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A 0.8-V 82.9- $\mu$ W In-Ear BCI Controller IC With 8.8 PEF EEG Instrumentation Amplifier and Wireless BAN Transceiver. *Lee, J., +, JSSC April 2019 1185-1195*

#### Prosthetics

A CMOS MedRadio Transceiver With Supply-Modulated Power Saving Technique for an Implantable Brain–Machine Interface System. *Lee, M., +, JSSC June 2019 1541-1552*

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**Public key cryptography**

An Energy-Efficient Reconfigurable DTLs Cryptographic Engine for Securing Internet-of-Things Applications. *Banerjee, U., +, JSSC Aug. 2019 2339-2352*

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A 112 Gb/s PAM-4 56 Gb/s NRZ Reconfigurable Transmitter With Three-Tap FFE in 10-nm FinFET. *Kim, J., +, JSSC Jan. 2019 29-42*

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