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Sub-100nm Non-planar 3D InGaAs MOSFETs: Fabrication and Characterization

Jiangjiang J. Gu, and Peide D. Ye

Department of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA

InGaAs MOSFETs have been considered promising candidate for post-Si logic devices beyond 14nm technology node. To meet the increasing demand in electrostatic control at sub-100nm channel lengths, non-planar 3D structures have been introduced to the fabrication of InGaAs MOSFETs. In this paper, the fabrication and characterization of various non-planar 3D InGaAs MOSFETs have been demonstrated and summarized, including InGaAs heterostructure FinFETs, InGaAs-on-nothing nanowire MOSFETs, and InGaAs gate-all-around nanowire MOSFETs. It is shown that the implementation of 3D structure greatly reduces short channel effect and improves scalability of InGaAs MOSFETs. The gate-all-around nanowire structure has been fabricated by a novel top-down approach for the first time and is found to offer great scalability down to at least 50nm channel length with good transport property, making InGaAs gate-all-around nanowire MOSFETs strong candidate for ultimately scaled III-V logic technology.

Introduction

InGaAs MOSFETs with encouraging device performance have been demonstrated, and are considered promising candidate to replace Si CMOS at 14nm technology node and beyond [1-3]. Much attention has been focused on the interface engineering between high-k dielectric and III-V channel to reduce the interface trap density (D_{it}), which is critical for realizing steep sub-threshold swing (SS) at off-state as well as large current drive at on-state. However, the effective control of short channel effect by utilizing advanced device structure such as non-planar 3D or ultra-thin body becomes equally important as device dimension reaches sub-100nm regime. As Si CMOS manufacturing enters a new era with the “tri-gate” design at 22 nm node [4], similar non-planar 3D approach is yet to be explored on its III-V counterpart [5]. In this paper, we summarize and review our recent development on several InGaAs non-planar 3D architecture, including, InGaAs heterostructure FinFET (HFinFET) [6], InGaAs-on-nothing nanowire MOSFETs (InGaAsON FET) [7], and InGaAs gate-all-around nanowire MOSFETs (InGaAs GAA FET) [8].

InGaAs HFinFETs

InGaAs surface-channel FinFETs have been demonstrated to suppress short channel effects and extend the scaling of InGaAs MOSFETs down to 100nm [5][9]. On the other hand, the buried-channel InGaAs MOSFETs with GaAs/AlGaAs, InAlAs or InP barrier [10-13] and quantum-well FETs (QWFETs) with thin InP barrier [2] have been shown to offer higher transconductance (g_m), higher effective mobility and lower SS compared to surface-channel III-V MOSFETs. Therefore, an InGaAs FinFET with wide bandgap

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barrier layers would benefit from both the good short channel effect control of the FinFET and the low voltage operation of the heterostructure design [14]. In this work, we demonstrated InGaAs HFinFETs with different Fin width (W_{Fin}) and two channel thickness of 10nm (type I) and 60nm (type II) shown in Figure 1 and 2.

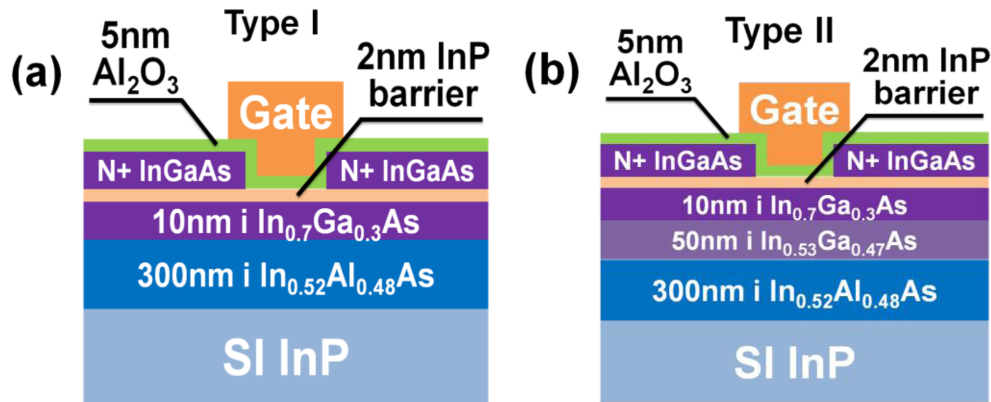

Figure 1. Schematic diagram of InGaAs HFinFETs with (a) 10nm channel (b) 60nm channel.

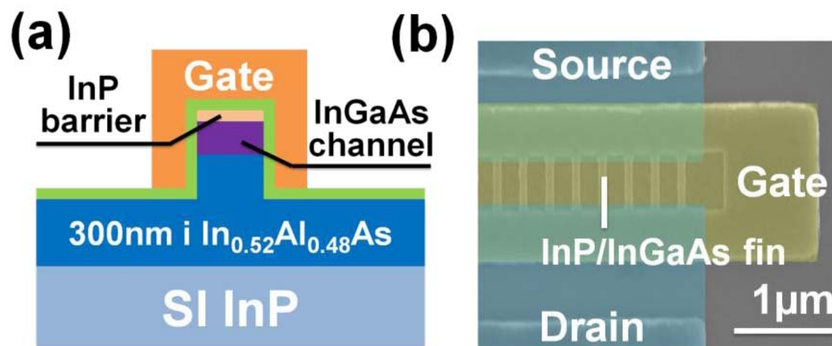

Figure 2. (a) Schematic cross section of InGaAs HFinFETs. (b) Top-view SEM image of a InGaAs HFinFET (type I) with W_{Fin}=30nm.

MOSFET fabrication started with a 2 inch semi-insulating InP substrate. A 300 nm undoped $In_{0.52}Al_{0.48}As$ buffer layer, 50 nm undoped $In_{0.53}Ga_{0.47}As$ channel layer (type I only), 10 nm undoped $In_{0.7}Ga_{0.3}As$ channel layer (type I and type II), 2 nm undoped InP barrier layer and 20 nm N+ doped InGaAs layer were sequentially grown by molecular beam epitaxy. Device isolation and gate recess etching were then performed using citric acid based solution. The gate lengths of the devices were varied from 0.5μm down to 100 nm. For non-planar devices, a fin etching process was done using BCl_3/Ar based reactive ion etching [5]. The smallest W_{Fin} defined was 30 nm. After short buffered oxide etch (BOE) dip, the samples were soaked in 10% $(NH_4)_2S$. The passivation time was fixed at 10 minutes. Previous Al_2O_3/InP capacitance-voltage studies revealed that 10 minute treatment was sufficient to achieve an effective passivation. The air exposure after sulfur treatment was minimized. The samples were then loaded into an ASM F-120 atomic-layer deposition (ALD) reactor for 5 nm Al_2O_3 deposition at 300 ^oC. Source/drain contacts were then formed by Au/Ge/Ni deposition and 350 ^oC rapid thermal annealing process (RTA). Finally, Ni/Au was electron beam evaporated as gate metal. Since sulfur passivation was found to be unstable after thermal treatment higher than 400 ^oC [15], no post deposition annealing (PDA) was performed after ALD gate dielectric deposition, and

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the thermal budget of the entire fabrication process was as low as 350 ^{o}C. All patterns were defined by a Vistec UHR electron beam lithography system.

Electrical characterization of InGaAs HFinFET with 10nm channel (Type I)

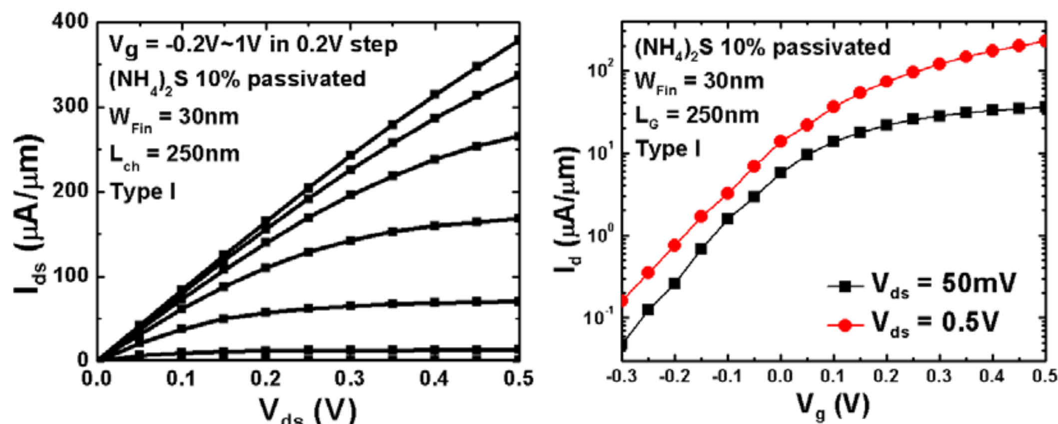

Figure 3. I_{ds}-V_{ds} and I_{ds}-V_{gs} of InGaAs HFinFET (Type I) with W_{Fin} =30nm and L_{ch}=250nm.

Figure 3 show the well-behaved output and transfer characteristics of a InGaAs HFinFET with L_{ch}= 250 nm, W_{Fin} = 30 nm and passivated with 10% $(NH_4)_2S$ before gate oxide deposition. A saturation drain current of 380 μA/μm and g_m of 557 μS/μm is obtained at a V_{ds} = 0.5 V. The threshold voltage (V_T) of the device is -0.05V from linear extrapolation at V_{ds} = 50 mV and -0.18V using 1μA/μm metric at V_{ds} = 0.5 V. A SS of 120 mV/dec and DIBL of 99 mV/V are also achieved. Compared to deep-submicron surface-channel InGaAs MOSFETs, a higher g_m is obtained at a lower drain voltage with the same gate oxide thickness [16], indicating the advantage of buried-channel devices for low-voltage operation.

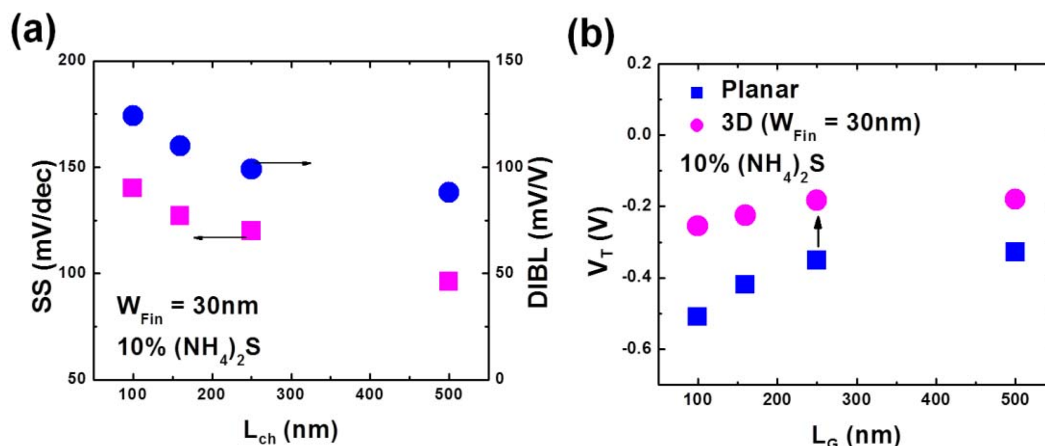

Figure 4. (a) SS and DIBL versus L_{ch} of 3D (W_{Fin} = 30 nm) InGaAs HFinFETs (Type I) (b) V_T versus L_G of planar and 3D (W_{Fin} = 30 nm) InGaAs HFinFET (Type I). V_T is determined by 1 μA/μm metric at V_{ds} = 0.5 V.

Furthermore, we investigate the scaling metrics of the InGaAs HFinFETs with 10% $(NH_4)_2S$ passivation and the gate lengths of the devices varied from 0.5 μm down to 100 nm. Figure 4 (a) shows the SS and DIBL versus L_{ch} for non-planar devices with W_{Fin} = 30 nm, where SS is obtained at a drain voltage of 0.5 V. It is found that SS and DIBL

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gradually increase with L_G shrinking due to the SCE. Further suppression of SCE can be achieved by reducing W_{Fin} [5], decreasing the equivalent oxide thickness, or implementing more advanced 3D structure such as gate-all-around structure [8]. Figure 4 (b) shows the V_T versus L_{ch} for planar and 3D devices with W_{Fin} = 30 nm. A 0.15V to 0.25V positive V_T shift has been observed for 3D devices, making the device operation more approaching enhancement-mode. Moreover, 3D devices show better threshold roll-off property due to a better electrostatic control of the channel. These results highlight the importance of introducing advanced 3D structure to the fabrication of III-V MOSFETs at deep submicron gate lengths.

Electrical characterization of InGaAs HFinFET with 60nm channel (Type II)

Figure 5 (a) show the transfer characteristics of planar and HFinFET with 60nm channel. Due to the thicker channel, type II planar devices show much worse off-state metrics than that of type I devices. Therefore, the non-planar 3D structure plays a more important role in this type of devices. Figure 5 (b) show the SS scaling metrics as a function of L_{ch}. The planar devices suffer from severe short channel effects, while the HFinFET is highly resistant to short channel effects. The SS of HFinFET with 60nm channel thickness is a constant regardless of the L_{ch}, showing good electrostatic control with L_{ch} down to at least 10nm. It is noted that the type II HFinFET show better gate control than type I due to the higher H_{Fin}/W_{Fin} ratio of the devices. To benefit fully from the 3D FinFET structure, fins of high aspect ratio is strongly needed.

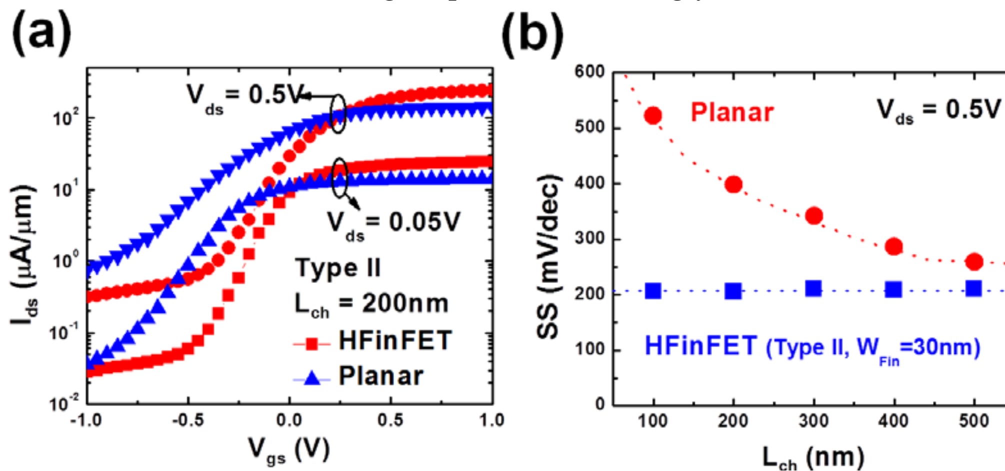

Figure 5. (a) Transfer characteristics of planar and HFinFET (Type II) with 60nm channel (b) SS as a function of L_{ch} for planar and HFinFET (Type II) at V_{ds}=0.5V.

InGaAs-On-Nothing nanowire MOSFETs

Silicon on nothing (SON) MOSFETs have been proposed [17] and experimentally demonstrated [18], providing a solution for quasi-total suppression of short channel effects and DIBL with L_{ch} down to 30 nm. The key fabrication processes for SON MOSFETs involve selective removal of the SiGe layer and formation of an air tunnel underneath the Si channel. Similarly, a SON counterpart on the III-V platform, namely III-V on nothing (III-VON), can also be realized if a selective etching process is developed to form an air gap underneath the III-V channel. We report the first experimental demonstration of III-VON MOSFETs with $In_{0.53}Ga_{0.47}As$ as the channel and atomic-layer-deposited (ALD) Al_2O_3 as the gate dielectric. The starting substrate is 30nm

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p- $In_{0.53}Ga_{0.47}As$ epitaxially grown on heavily p-doped InP substrate. The key fabrication has been enabled by well-controlled HCl based selective etching of InP over InGaAs. It is found that the InGaAs fins have to be patterned along [010] direction in order to achieve a successful channel release process, owing to the anisotropy of InP wet etching. III-VON MOSFETs with gate length down to 50 nm and fin width down to 40 nm were fabricated. A low DIBL of 45mV/V at 50 nm gate length is observed experimentally, which is consistent with the numerical simulation results from 3D Synopsys Sentaurus TCAD. This shows that the III-VON structure is effective at suppressing the SCE of III-V MOSFETs down to at least L_G = 50 nm.

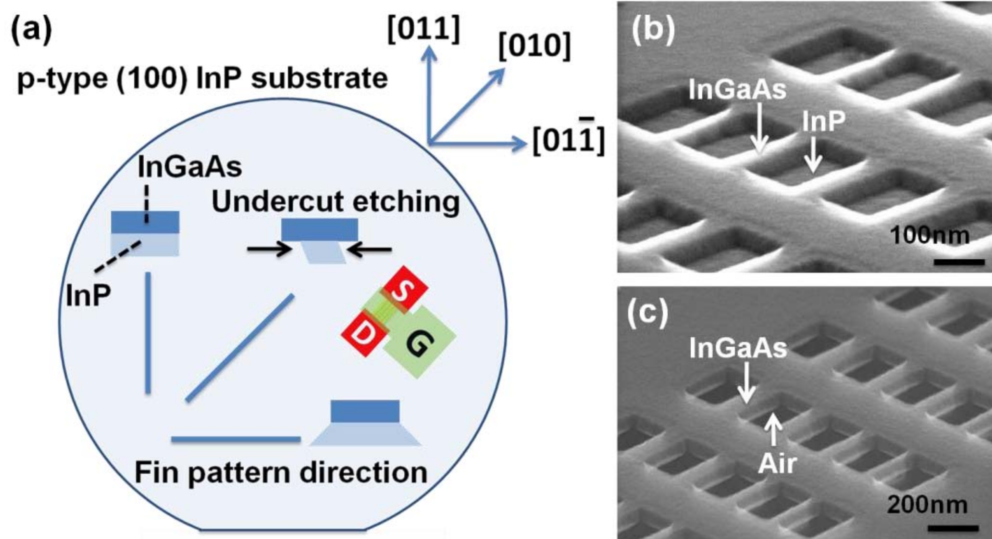

Figure 6 (a) Schematic diagram of fin patterning direction, release etching profile, device alignment to the substrate (b) Tilted SEM image of fin test structures after fin dry etching and before wire release (c) Tilted SEM image of fin testing structures after wire release.

MOSFET fabrication started with a 2 inch p+ InP wafer. A 30nm $In_{0.53}Ga_{0.47}As$ layer with p-doping of 2×10^{16} cm^{-3} was grown on InP substrate by molecular beam epitaxy as the channel layer. After surface treatment with $(NH_4)OH$ solution, a 10nm Al_2O_3 was grown by ALD as an encapsulation layer. Source/drain regions were then defined and Si ion implantation at energy of 20 keV and dose of 1×10^{14} cm^{-2} was performed. The shortest gate length of 50 nm was defined by the separation between source and drain regions. Dopant activation was done using rapid thermal annealing (RTA) at 600°C for 15 seconds in nitrogen ambient. Next, the InGaAs fins were patterned along [010] direction as shown in Figure 1 (a), using diluted ZEP520A electron-beam resist with a thickness of 200 nm. The fin etching was performed with BCl_3/Ar gas using a Panasonic high density plasma etcher. After removing the resist, the sample was treated sequentially with diluted buffered oxide etch (BOE) and diluted mixture of HCl and hydrogen peroxide (H_2O_2). Then the channel release process was performed using HCl:H_2O (1:2) solution. It is known that HCl based solution has high selectivity between InP and InGaAs. However, the InP etching is found to be highly anisotropic, and undercut etching is only possible along <100> directions [19]. Test fin structures along [011], [010] and [01-1] were patterned, followed by etching in diluted HCl. For different fin patterning directions, the etching profile varies as depicted in Figure 6 (a). Figure 6 (b) and (c) show the tilted scanning electron microscopy (SEM) images for fin test structures before and after channel release process respectively, where successful undercut etching was demonstrated. Patterning the fin along <100> directions is the key to realize the III-V

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channel release at the deep sub-micron scale. After channel release, a 5 nm Al_2O_3 was regrown using ALD as the gate dielectric. Note that for the purpose of process demonstration, no pre-gate surface passivation such as $(NH_4)_2S$ treatment was carried out here. The gate structure was formed by electron beam evaporation of Ni/Au and liftoff process. Due to the vertical directionality of the evaporation, the air gap naturally remains underneath the channel. Au/Ge/Ni source/drain metal was then evaporated and annealed at 350°C in nitrogen ambient. Finally, test pads were deposited which concluded the fabrication processes. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system.

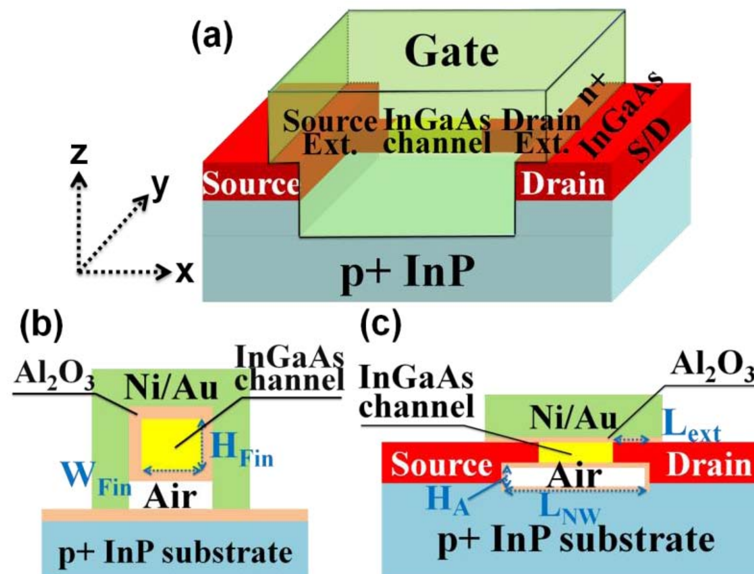

Figure 7 (a) Schematic diagram of a III-VON MOSFET with $In_{0.53}Ga_{0.47}As$ channel and Al_2O_3 gate dielectric from a bird's eye view (b) Cross sectional view of a III-VON MOSFET in x-y plane (c) Cross sectional view of a III-VON MOSFET in x-z plane.

Figure 7 (a) shows the schematic diagram of a finished III-VON device from a bird's eye view. Figure 7 (b) and (c) depict the schematic cross section of the device in the y-z plane and the x-z plane, respectively. The fin height (H_{Fin} = 30 nm) is determined by the initial InGaAs layer thickness. The smallest W_{Fin} achieved is 40 nm. The nanowire length (L_{NW}) in this work is fixed at 300 nm, yielding a source/drain extension length (L_{ext}) of around 125 nm for a 50 nm L_{ch} device. The smallest air gap height (H_A) is around 40 nm, controlled by the release etching time. The L_{ch} of the devices vary from 100 nm down to 50 nm. Figure 8 (a) and (b) shows the output, transfer characteristic and gate leakage current versus gate voltage of a typical III-VON MOSFET with L_{ch} of 50 nm, W_{Fin} of 40 nm, and four wires in parallel. To better evaluate the intrinsic device performance, source current is used to eliminate the effect from non-ideal source/drain junction leakage current. The device operates in enhancement mode, with a threshold voltage of 0.36 V from linear extrapolation at a drain voltage of 50 mV. A low DIBL of 45 mV/V is obtained at the shortest gate length of 50 nm, thanks to the III-VON structure. As a comparison, a 100 nm gate length InGaAs FinFET has a DIBL of around 180 mV/V [5]. The subthreshold swing (SS) is found to be around 200 mV/dec, indicating relatively large interface trap density (D_{it}). Surface treatment before the formation of ALD Al_2O_3 gate dielectric which could have improved the D_{it} was not performed since that was not our main purpose in this study. Gate leakage current is similar to that in Ref. [5] and stays very low at gate voltage less than 1V. The saturation current at a drain voltage of 1.6V

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and a gate voltage of 2V reaches 10μA/μm, normalized by the total width of the gated region, i.e. $W_{ch} = 2\times H_{Fin} + W_{Fin}$. The current can be further improved by applying $(NH_4)_2S$ pre-gate treatment and reducing source/drain series resistance.

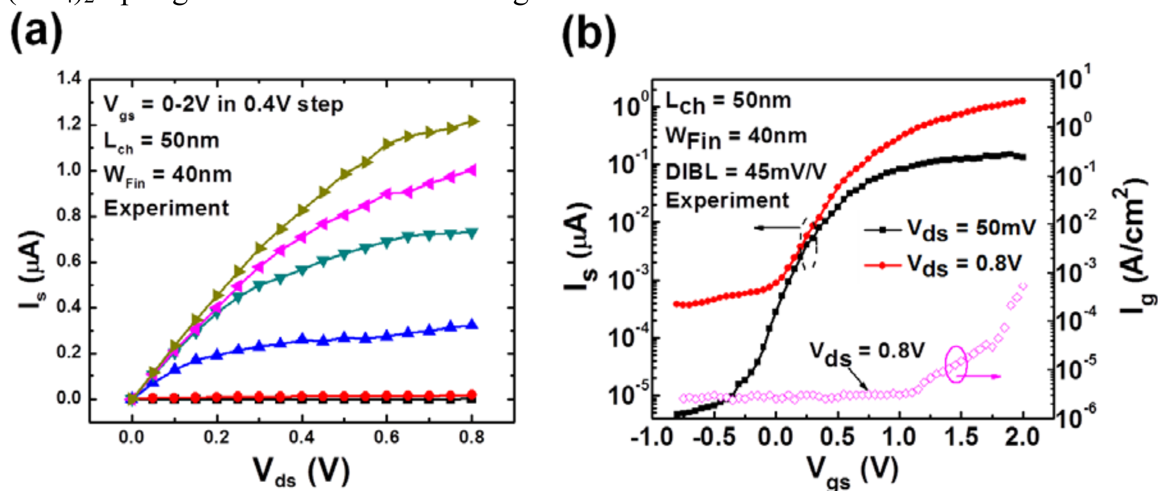

Figure 8 (a) Output and (b) transfer characteristics of InGaAs-ON MOSFETs with L_{ch}=50nm, W_{Fin}=40nm.

To further confirm the experimental data and examine the effects of various design parameters on device performance, 3-dimensonal TCAD simulation was performed using Synopsys Sentaurus. Device structures were first created according to the experimental parameters, i.e. W_{Fin} = 40 nm, H_{Fin} = 30 nm, etc. The Poisson's equation, electron and hole continuity equations were solved using a coupled solver at each mesh node to obtain various output parameters such as potential, electric field, electron and hole density, etc. No interface traps were incorporated in the simulation. From the simulated transfer characteristics, DIBL was extracted and compared with the experimental data as shown in Figure 9. The experimental data agrees well with the simulation results. Moreover, the DIBL obtained from InGaAs FinFETs in Ref. [5] is also plotted in the same figure. The III-VON structure shows significant improvement in DIBL reduction, confirming that the more advanced 3D structures are beneficial for the suppression of the SCE.

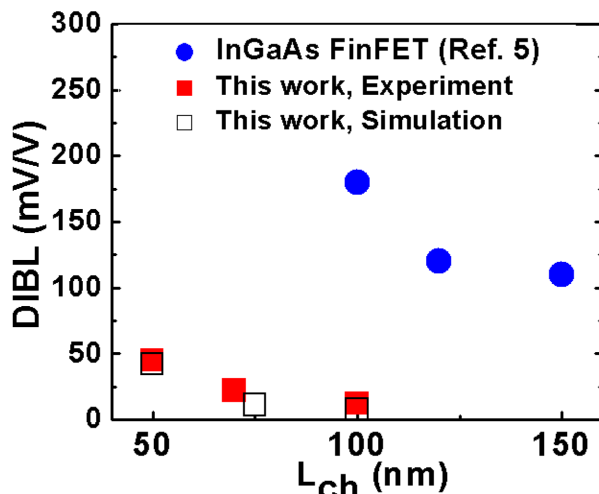

Figure 9 DIBL versus L_{ch} for III-VON MOSFETs from experiment (square) and simulation (hollow square) compared to that of InGaAs FinFET (circle).

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InGaAs Gate-all-around nanowire MOSFETs

The GAA structure has been proven on Si CMOS to be the most resistant to SCE, thanks to having the best gate electrostatic control [20-22]. Therefore, a III-V GAA FET is the most promising candidate for the ultimately scaled III-V FETs. We report the first experimental demonstration of inversion-mode $In_{0.53}Ga_{0.47}As$ GAA FETs by a top-down approach with ALD Al_2O_3/WN gate stacks. Benefiting from the GAA structure, we have demonstrated the shortest L_{ch} = 50nm III-V MOSFETs to date with well-behaved on- and off-state characteristics. A systematic scaling metrics study has been carried out for $In_{0.53}Ga_{0.47}As$ GAA FETs with L_{ch} from 110nm down to 50nm, W_{Fin} of 30nm and 50nm, fin height (H_{Fin}) of 30nm, and wire lengths L_{NW} of 150 to 200nm. The SCE has been effectively suppressed by the advanced 3D design.

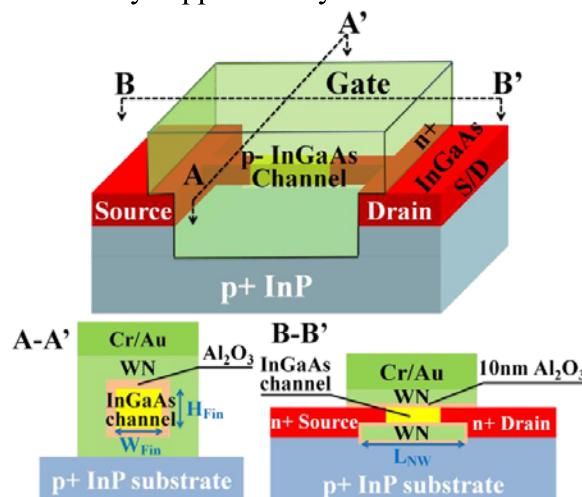

Figure 10 Schematic diagram of InGaAs GAA FETs from bird's eye view.

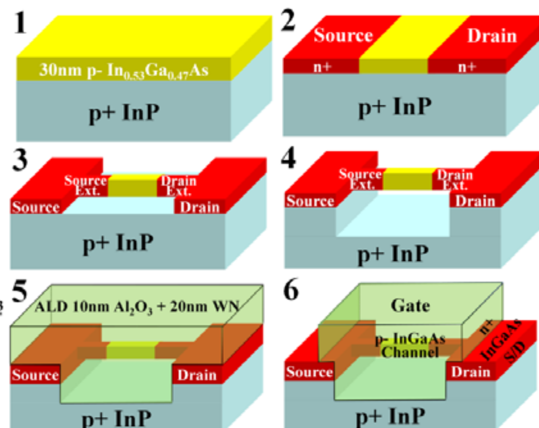

Figure 11 Key Fabricatin process of InGaAs GAA FETs.

Fig. 10 shows a schematic view of an $In_{0.53}Ga_{0.47}As$ GAA FET fabricated in this work. Fig. 11 depict the key fabrication processes for $In_{0.53}Ga_{0.47}As$ GAA FETs. A 30nm p-doped 2×10^{16} cm^{-3} $In_{0.53}Ga_{0.47}As$ channel layer was epitaxially grown on a p+ (100) InP substrate by MBE as the starting material (Fig. 11-1). After surface degrease and NH_4OH pretreatment, 10nm Al_2O_3 was grown by ALD as an encapsulation layer. Source/drain Si implantation was then performed at an energy of 20keV and a dose of 1×10^{14} cm^{-2} (Fig. 11-2). The dopant activation was carried out at 600 °C for 15 seconds in nitrogen ambient. The source/drain separation determines the final L_{ch} of the devices. After removing the encapsulation layer by buffered oxide etch (BOE), the InGaAs fin etching was done by BCl_3/Ar high density plasma etching (HDPE) (Fig. 11-3). The diluted ZEP520A electron-beam resist with a thickness of 100 nm was used as a hard mask for the fin etching and the smallest W_{Fin} defined was 30nm. After surface cleaning in BOE and diluted $HCl:H_2O_2$ solution, the InGaAs channel release process was carried out using $HCl:H_2O$ (1:2) solution (Fig. 11-4). HCl based solution can selectively etch InP over InGaAs. However, the etching is found to be highly anisotropic. Therefore the InGaAs fins have to be patterned along <100> directions for a successful release process. Fig. 12 (a) shows the cross-sectional STEM image of InGaAs nanowire test structures wrapped by 50nm ALD Al_2O_3 on InP substrate, confirming the nanowires are completely released. After channel release, the samples were soaked in 20% $(NH_4)_2S$ for pre-gate interface passivation. Then the samples were immediately transferred to an ASM F-120 ALD reactor via room ambient. 10nm Al_2O_3 was regrown as the gate dielectric at 300 °C.

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20nm WN metal gate was then deposited in a separate ALD reactor at 385 ^oC (Fig. 11-5), with a resistivity of ~4000μΩ·cm [23]. The conformal deposition of ALD Al_2O_3/WN surrounding the nanowire channel is the key fabrication process for realizing the GAA structure. After gate stack deposition, gate etch process was performed using CF_4/Ar HDPE, where Cr/Au gate pattern was defined as the hard mask (Fig. 11-6). The CF_4 based dry etching chemistry provides excellent selectivity between WN and Al_2O_3, resulting in a damage-free gate oxide. The source/drain contact was then formed by electron beam evaporation of Au/Ge/Ni, followed by 350 ^oC rapid thermal annealing in nitrogen ambient. Finally, the Ti/Au test pads were defined. The fabricated MOSFETs have a nominal L_{ch} varying from 50nm to 120nm, W_{Fin} from 30nm to 50nm, and different numbers of parallel channels (1 wire, 4 wires, 9 wires or 19 wires). Fig. 12 (b) shows the SEM image of a InGaAs GAA FET with 4 parallel wires.

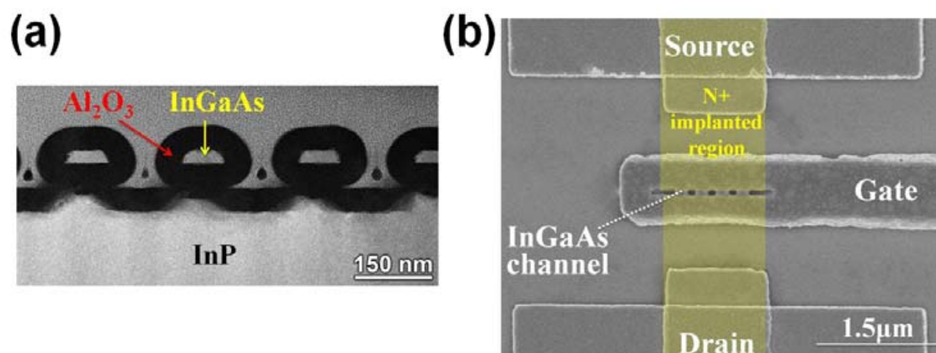

Figure 12 (a) Cross-sectional STEM image of InGaAs nanowire test structures wrapped by 50nm ALD Al_2O_3 on InP substrate (b) Top view SEM image of a finished InGaAs GAA FET with 4 parallel wires of W_{Fin} = 30nm , L_{NW} = 200nm and L_{ch} = 50nm.

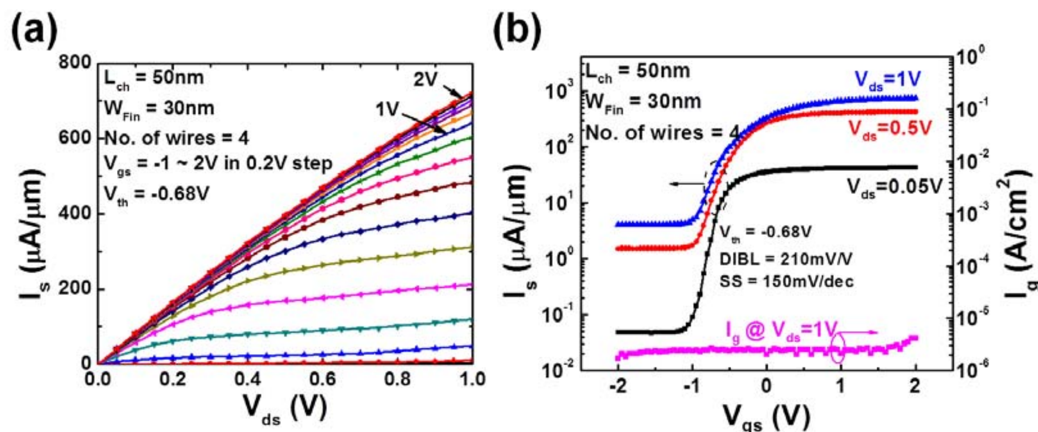

Figure 13 (a) output and (b) transfer characteristics of InGaAs GAA FET with L_{ch}=50nm, W_{NW}=30nm.

Fig. 13 (a) and (b) show the well-behaved output and transfer characteristics as well as I_g-V_g of a L_{ch} = 50nm GAA FET. The current here is normalized by the total perimeter of the $In_{0.53}Ga_{0.47}As$ channel, i.e. $W_G = (2W_{Fin} + 2H_{Fin}) \times$ (No. of wires). A representative 50nm L_{ch} device shows on-current of 720μA/μm, transconductance of 510μS/μm and reasonable off-state characteristics with subthreshold swing (SS) of 150mV/dec and drain-induced barrier lowering (DIBL) of 210mV/V. Although operating in inversion-mode, the threshold voltage of the device is -0.68V from linear extrapolation at V_{ds}=50mV due to the relatively low work function of ALD WN metal (~4.6eV). Due to

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the junction leakage current and a very large area ratio (>10^3) between implanted junction and GAA channels, the source current is used to obtain the intrinsic current in the channel. Gate leakage current is minimal in the entire gate voltage range, indicating 10nm Al_2O_3 is sufficient for GAA structure and further equivalent oxide thickness (EOT) scaling is achievable. It also shows that the WN gate etch process is damage-free.

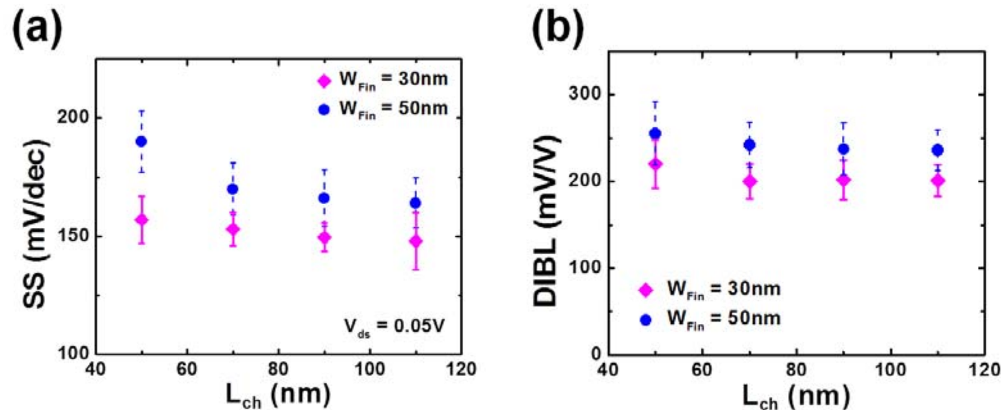

Figure 14 (a) SS and (b) DIBL scaling metrics of InGaAs GAA FETs with L_{ch} down to 50nm.

Fig. 14 show the off-state (SS and DIBL) scaling metrics for L_{ch} = 50 - 110nm with W_{Fin}=30nm and 50nm. The SS for 30nm W_{Fin} devices are almost unchanged at around 150mV/dec when scaling L_{ch} down to 50nm, indicating excellent control of SCE, whereas the 50nm W_{Fin} devices show larger SS, which increases with scaling of L_{ch}. It is noted here that the 100nm L_{ch} InGaAs FinFET with 5nm Al_2O_3 gate oxide shows similar SS [5] as the 50nm L_{ch} GAA FET with 10nm Al_2O_3 in this work. This translates to at least a factor of 2 improvement of midgap D_{it} (~5.6×10^{12}/cm^2·eV) achieved. The improved interface quality indicates that the newly-developed channel release process can provide a smooth damage-free InGaAs bottom surface. Fig. 11 shows that 30nm W_{Fin} devices have smaller DIBL and the DIBL is roughly independent of L_{ch}, confirming the effective SCE control. Further SS and DIBL reduction can be achieved by scaling down EOT and reducing the InGaAs nanowire dimension. Figure 15 compares g_m EOT product for InGaAs GAA FETs with InGaAs MOSFETs fabricated in our group recently. The InGaAs GAA FETs benefits from the continuous scaling of the L_{ch} down to 50nm.

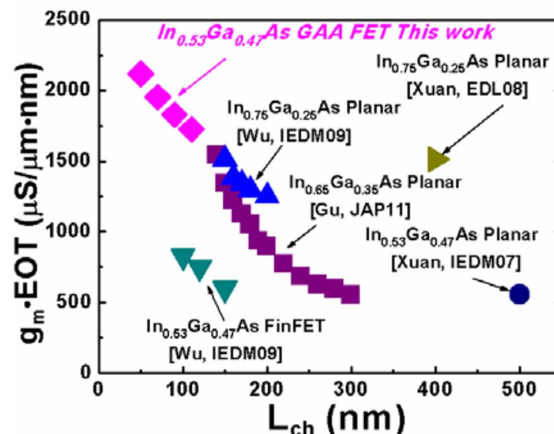

Figure 15 Benchmarking g_m·EOT of planar and non-planar InGaAs surface-channel MOSFETs.

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We have demonstrated for the first time inversion-mode $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with ALD Al_2O_3/WN gate stacks. The highest saturation current reaches 1.17mA/μm at L_{ch} = 50nm and V_{ds} = 1V with $g_{m,max}$ = 701μS/μm. Detailed scaling metrics study shows that the 3D GAA structure can effectively control the SCE with L_{ch} scaling down to at least 50nm, making III-V GAA FET a very promising candidate for ultimately scaled III-V logic device technology.

Summary

In this paper, we have demonstrated non-planar 3D InGaAs MOSFETs including InGaAs HFinFETs, InGaAs-on-nothing nanowire MOSFETs and InGaAs gate-all-around nanowire MOSFETs. InGaAs HFinFETs with high aspect ratio fins show better scalability and extend the scaling of InGaAs MOSFETs down to 100nm L_{ch}. The introduction of nanowire structure further increases the resistance to short channel effects and record-low DIBL of 45mV/V has been achieved at 50nm L_{ch} for InGaAs-ON MOSFETs. The InGaAs GAA FETs show the best electrostatic control and is the most promising candidate for future high-speed low-power logic applications. Further interface passivation, EOT scaling and source/drain engineering is needed to optimized the device performance of the InGaAs GAA FETs.

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