Design of a Software Defined Radio Using Soc Builder

Cristian Randieri[1], Valerio Francesco, Puglisi[2]

[1]eCampus University, Via Isimbardi, 10, Novedrate, 22060, Italy
[2]University of Catania, Dept. of Mathematics and Computer Science, Catania, Italy

Abstract

This paper deals with the development of SDR systems on XILINX RF-SOC devices using the MATHWORKS "SOC Builder" tool. RF-SOC are complex devices integrating microprocessors, FPGA, and RF converters (both ADC and DAC). This complexity requires engineers' transversal competence sweeping from software, hardware, and RTL coding capabilities. For this reason, although these devices are very powerful, the implementation of complex systems on them is very demanding work. The MATHWORKS SOC builder tool is a promising toolchain that allows designers to develop complex SDR systems on XILINX RF-SOC using the Simulink environment, without the necessity to write c/c++ code and without the knowledge of HDL language. This work analyzes this interesting environment underlining its potential in the development of SDR systems. Experimental results are presented in terms of hardware complexity, maximum frequency and power consumption.

Keywords

SDR, FPGA, RF SAMPLING

1. Introduction

In the last few years, the introduction of RF Analog to Digital Converters and Digital to Analog Converters made possible the development of Software Defined Radio (SDR) characterized by an always more reduced number of analog components,[1, 2]. SDR introduce several advantages as the ability to receive and transmit various modulation schemes, the ability to upgrade functionalities downloading and running new firmware, the possibility of adaptively choosing operating frequencies and the reduction of analog hardware. For all those reasons, in the last few years, electronic devices manufacturers proposed new microchips with RF ADC and RF DAC capabilities. Among these devices, XILINX RF-SOCS are very interesting because they integrate into a single chip a microprocessor, an FPGA, and several RF ADC/DAC [3, 4**?**]. The possibility to have all these elements in a single chip is very interesting for several reasons: the PCB design process is considerably simplified; modern communication systems are very complex integrating several functionalities such as communication algorithms [5, 6, 7, 8], machine learning [9, 10, 11, 12, 13], etc. that require different processing devices. In this scenario, the possibility of partitioning the processing between the microprocessor and FPGA is a very important aspect. The microprocessor can be used to manage peripherals and implement low throughput algorithms while FPGA can be used for custom datapaths [14]. For modern communication systems characterized by heterogeneity in terms of algorithms the use of FPGA is alwaysmore a necessity. FPGA allows to realize customizable datapaths characterized by high computation capabilities, reconfigurability and reduced power consumption. These feature are very important for the realization so new generation communication systems that integrates advanced DSP and machine learning requirement[15, 16, 17, 18, 19]. XILINX RF-SOCs offer these interesting feature integrating in the same chip also high speed Analog to digital converters and Digital to analog converters. In a single chip designer have all the devices necessary to implement complex software defined systems for what concerns the digital parts and the converters. Although RFSOCS are very interesting objects their use requires transversal knowledge sweeping from RTL design, to software design. The MATHWORKS SOC BUILDER tools is a very interesting design flow that allows the designer to configure RFADC/DAC, program microprocessor, and design FPGA systems directly in the MATLAB/SIMULINK environment without the necessity to write c/c++ code and without the necessity to know HDL languages like VHDL, Verilog/System Verilog. In this paper, we explore the SOC Builder tool capabilities. To do it we realized an SDR transmitter

2. The XILINX RF-SOC

Xilinx Zynq Ultrascale+ RFSoC integrate programmable logic,n ARM cortex system and RF ADC/DAC in the same SoC.

The integration of these components in a single die allows to save area and power and simplifies the design of the board being the RF signal is directly sampled without further analog up/down-conversions. The analog components are so reduced with a consequent reduction

ICYRIME 2022: International Conference of Yearly Reports on Informatics, Mathematics, and Engineering. Catania, August 26-29, 2022
cristian.randieri@unicampus.it (C. Randieri);
valeriopuglisi.vp@gmail.com (V. F. Puglisi)

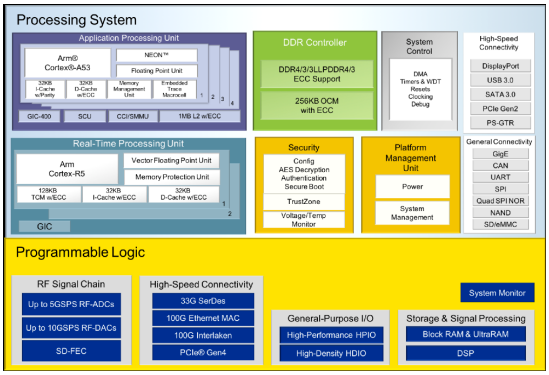

Figure 1: RFSoC block diagram

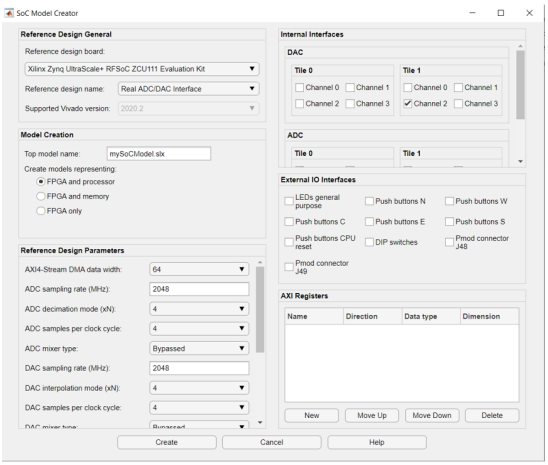

Figure 2: Reference design generator

of all the harware complexity and the design.

XILINX RFSoC devices allow to directly sample RF signals until 6 GHz. This aspect make these devices suitable for applications using bands L, S and C as for example:

- Multi-band 5G networks
- Massive MIMO
- Phased Array systems
- Space communications
- RADAR

The block diagram of the XILINX RFSoC is shown in Figure ??.

The RFSoC Analog-to-digital and Digital-to-analog converters,offer the possibility to manage real and complex signals (I/Q). The structure of ADCs is organized in *tiles*. Each tile is composed of 4 ADCs and 1 PLL with 12 or 14 bits operation mode. DAC are organized with 4 14 bits DACs and 1 PLL with a bandwidth of 4 GHz and output frequency until 5 GHz. The device is 40x40-mm in size, with a 1517-pin ball grid array (BGA) package and is manufactured with a 16-nm Fin field-effect transistor (FinFET) process [2]

3. SDR design with SOC builder

In order to simplify the design, the SOC Builder tool offers a script called SocModelCreator that can be used to generate reference designs of different tipology. The script launches a GUI that allows designers to set many parameters. Among these parameters the most important are:

- The possibility to choose among several reference design.
- The possibility to set ADC and DAC directly in matlab without the necessity of other tools
- The possibility to include in the project external I/O interfaces as for example the switched the LEDs.
- The possibility to include AXI register to read and write data from Simulink to the board
- The possibility to choose to realize a project for the ARM+ the FPGA or FPGA only
- The possibility to manage external DDR4 memory.

In Fig.?? is shown the Graphical User Interface for the SOC configuration ad system developement.

The most interesting feature is surely the possibility to set the ADCs and the DACs. Modern converters are in general very complex devices and their configuration is a very difficult operation. SocModelCreator allows configuring these devices using this simple GUI simplifying the configuration process.

There is the possibility to set sample frequencies and other parameters. For example, converters can operate in real mode or in complex IQ mode. In the case of IQ modes, it is also possible to configure mixers for the up and the down-conversion of the signal. In fact, XILINX RF-SOC has integrated mixers that allow the designer to perform up and down conversion without the necessity to waste FPGA hardware resources.

In addition to the mixers, XILINX RF-SOC provide also hardware interpolators and decimators in the proximity of DAC and ADC. The presence of these blocks simplifies the design. Another interesting feature regards the possibility to interface the converters in frame-based mode. In other words, it is possible to send and receive data through converters using more than one sample per clock cycle. This feature allows designers to create parallel datapaths characterized by a reduced clock frequency

[20],[21]. For example, let's consider setting 4 samples for clock cycles. If the sample rate of the converters is set for example to 1 GHz, the possibility to have 4 samples for the clock cycle makes it possible to split the datapath into 4 parallel datapath having a data rate of 250 MHz. In this way, it is easier to not violate the clock constraint during the STA phase.

The SocModelCreator tool, one configured for a reference design, create a Simulink model like the one shown in Fig?? This model is divided into two main part, a block for the FPGA and a block for the microprocessor. Different from the traditional SOC development environment where design has to use HDL languages to program the FPGA and C/C++ to program the microprocessor, using SOC builder designer has to use only Simulink with a consequent simplification of the flow design. Both the FPGA and microprocessor algorithm have to be described in terms of block diagram using Simulink

4. Experimental results

In order to evaluate the potential offered by SOC builder in the design of SDR systems we realize a QPSK modulator composed of a bit generator, a squared raised cosine filter with interpolation, and a DDS. We use the DDS for the operation of upconversion.

After the design of the Simulink block diagram, the system has been synthetized and implemented directly in the MATLAB environment. This is possible because the MATLAB callS, configure, and execute the XILINX VIVADO tool. In this way, designers can complete the design flow directly in MATLAB without the necessity to manually use VIVADO and other complex tools. In case of synthesis failure or STA violation the SOC BUILDER tool adverts the design with alerts in the TCL.

The use of SOC builder speeds up the design process making possible the realization of SDR systems in a very reduced time if compared with traditional design flows.

Advanced synthesis instruction allows designer to set important parameters directly in Simulink without the necessity to do it in VIVADO. For example, it is possible to manage the re-timing register in order to improve the performance in terms of throughput.

The implemented system has been tested using the XILINX ZCU111 board shown in Fig. ??

Implementation results underline a power consumption of about 8W, a maximum clock frequency of 100 MHz and a very reduced use of the hardware resources of the FPGA. The entire modulator has been realized using only:

- 14,531 LUT
- 19,233 Flip Flop
- 26 DSP
- 13 BRAM

The entire modulator has been developed maintaining 16-bit of accuracy in all the data path.

5. Conclusions

In this paper, we explored the capabilities of a new MATHWORKS tool called SOCBUILDER for the design of SDR based on XILINX RF-SOC devices.

A Q-PSK modulator has been realized and implemented on a XILINX ZCU111 board. The entire system has been designed entirely in Simulink without the necessity to use other software tools. SOCBUILDER allows the possibility to perform fixed-point analysis, simulations, and customization in the synthesis providing the possibility to manage hardware primitives and synthesis settings as the retiming. The possibility to simulate the DUT (Design Under Test) in the Simulink environment in addition to the other Simulink toolbox help designer in the verification stage of the design. DUT can be stimulated directly with real case data. Implementation results show that SOCBUILDER allows to implement communication system with reduced hardware complexity.

References

[1] T. Ulversoy, Software defined radio: Challenges and opportunities, IEEE Communications Surveys & Tutorials 12 (2010) 531–550.

[2] F. Di Francoa, C. Ramettab, M. Russoa, M. Vaccaroa, Rf sampling of wideband signals using xilinx ultrascale+ rfsoc (2020).

[3] Xilinx, Zynq UltraScale+ RFSoC, Technical Report, 2019. URL: https://www.xilinx.com/publications/product-briefs/rfsoc-product-brief.pdf.

[4] G. Magistris, C. Rametta, G. Capizzi, C. Napoli, Fpga implementation of a parallel dds for wide-band applications, in: CEUR Workshop Proceedings, volume 3092, 2021, pp. 12–16.

[5] G. Capizzi, C. Napoli, S. Russo, M. Woźniak, Lessening stress and anxiety-related behaviors by means of ai-driven drones for aromatherapy, in: CEUR Workshop Proceedings, volume 2594, 2020, pp. 7–12.

[6] G. De Magistris, S. Russo, P. Roma, J. Starczewski, C. Napoli, An explainable fake news detector based on named entity recognition and stance classification applied to covid-19, Information (Switzerland) 13 (2022). doi:10.3390/info13030137.

[7] C. Ciancarelli, G. De Magistris, S. Cognetta, D. Appetito, C. Napoli, D. Nardi, A gan approach for anomaly detection in spacecraft telemetries, Lecture Notes in Networks and Systems 531 LNNS (2023) 393–402. doi:10.1007/978-3-031-18050-7_38.

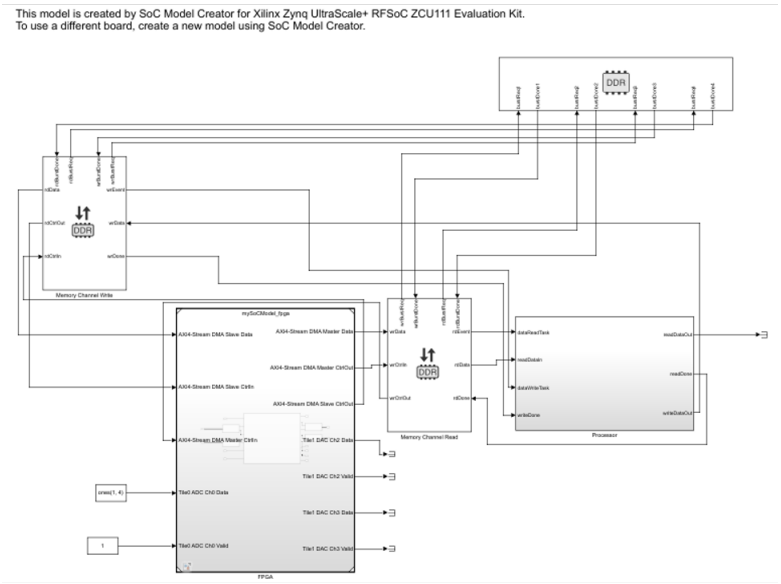

Figure 3: Reference design

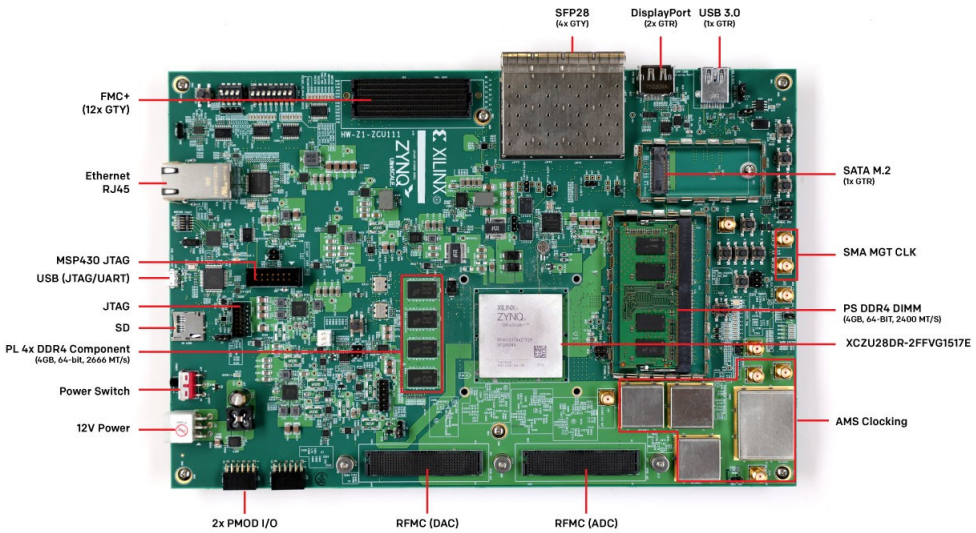

Figure 4: The ZCU111 board

[8] C. Napoli, G. De Magistris, C. Ciancarelli, F. Corallo, F. Russo, D. Nardi, Exploiting wavelet recurrent neural networks for satellite telemetry data modeling, prediction and control, Expert Systems with Applications 206 (2022). doi:10.1016/j.eswa.2022.117831.

[9] R. Giuliano, The next generation network in 2030: Applications, services, and enabling technologies, in: 2021 8th International Conference on Electrical Engineering, Computer Science and Informatics (EECSI), IEEE, 2021, pp. 294–298.

[10] F. Liao, S. Wei, S. Zou, Deep learning methods in communication systems: A review, in: Journal of Physics: Conference Series, volume 1617, IOP

Publishing, 2020, p. 012024.
[11] R. Brociek, G. Magistris, F. Cardia, F. Coppa, S. Russo, Contagion prevention of covid-19 by means of touch detection for retail stores, in: CEUR Workshop Proceedings, volume 3092, 2021, pp. 89–94.
[12] L. Canese, G. Cardarilli, L. Di Nunzio, R. Fazzolari, D. Giardino, M. Re, S. Spanò, Efficient digital implementation of a multirate-based variable fractional delay filter for wideband beamforming, IEEE Transactions on Circuits and Systems II: Express Briefs (2023).
[13] R. Aureli, N. Brandizzi, G. Magistris, R. Brociek, A customized approach to anomalies detection by using autoencoders, in: CEUR Workshop Proceedings, volume 3092, 2021, pp. 53–59.
[14] F. Silvestri, S. Acciarito, G. C. Cardarilli, G. M. Khanal, L. D. Nunzio, R. Fazzolari, M. Re, Fpga implementation of a low-power qrs extractor, in: International Conference on Applications in Electronics Pervading Industry, Environment and Society, Springer, 2017, pp. 9–15.
[15] G. Capizzi, G. Lo Sciuto, C. Napoli, R. Shikler, M. Woźniak, Optimizing the organic solar cell manufacturing process by means of afm measurements and neural networks, Energies 11 (2018) 1221.
[16] R. Avanzato, F. Beritelli, M. Russo, S. Russo, M. Vaccaro, Yolov3-based mask and face recognition algorithm for individual protection applications, in: CEUR Workshop Proceedings, volume 2768, 2020, pp. 41–45.
[17] F. Bonanno, G. Capizzi, G. L. Sciuto, A neuro wavelet-based approach for short-term load forecasting in integrated generation systems, in: 2013 International Conference on Clean Electrical Power (ICCEP), IEEE, 2013, pp. 772–776.
[18] F. Bonanno, G. Capizzi, G. Lo Sciuto, C. Napoli, G. Pappalardo, E. Tramontana, A cascade neural network architecture investigating surface plasmon polaritons propagation for thin metals in openmp, in: Artificial Intelligence and Soft Computing: 13th International Conference, ICAISC 2014, Zakopane, Poland, June 1-5, 2014, Proceedings, Part I 13, Springer, 2014, pp. 22–33.
[19] N. Brandizzi, V. Bianco, G. Castro, S. Russo, A. Wajda, Automatic rgb inference based on facial emotion recognition, in: CEUR Workshop Proceedings, volume 3092, 2021, pp. 66–74.
[20] A. Simonettaa, M. C. Paolettia, M. Muratorea, A new approach for designing of computer architectures using multi-value logic, Proceeding recursively 1 (2021) 7.
[21] A. Simonetta, M. C. Paoletti, Designing digital circuits in multi-valued logic, International Journal on Advanced Science, Engineering and Information Technology 8 (2018) 1166–1172.